**Conversion Register**

This 16-bit register contains the result of the last conversion in binary twos complement format. Following power-up, the Conversion Register is cleared to '0', and remains '0' until the first conversion is completed.

| BIT | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| NAME | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

**Data Format**

The ADS1118 provide 16 bits of data in binary twos complement format. The positive full-scale input produces an output code of 7FFFh and the negative full-scale input produces an output code of 8000h. The output clips at these codes for signals that exceed full-scale. The table below summarizes the ideal output codes for different input signals.

| Input Signal, $V_{IN}$ ($AIN_P$ - $AIN_N$) | Ideal Output Code |
|---|---|
| ≥ FS $(2^{15} – 1)/2^{15}$ | 7FFFh |
| $+FS/2^{15}$ | 0001h |
| 0 | 0001h |
| $–FS/2^{15}$ | FFFFh |
| ≤ –FS | 8000h |