Register 8—PGA Input Configuration (address = 0x08) (Read/Write)

BIT #	D7	D6	D5	D4	D3	D2	D1	D0
BIT Name	0	VP2	VP1	VP0	0	VN2	VN1	VN0

This register connects the inputs of the PGA to the various multiplexed input pins. Table 1 and Table 2 show the relationship between register, contents, and PGA inputs.

Bit Descriptions

Reserved (Bit 7, Bit 3)
These bits are reserved and must be set to '0'.

VP: PGA Positive Input (Bits 6-4)
These bits specify which input channel to connect to the positive input of the PGA.

VN: PGA Negative Input (Bits 2-0)
These bits specify which input channel to connect to the negative input of the PGA.

VP2	VP1	VP0	PGA POSITIVE INPUT
0	0	0	PGA V_{IN+} connected to V/I-0
0	0	1	PGA V_{IN+} connected to V/I-1
0	1	0	PGA V_{IN+} connected to V/I-2
0	1	1	PGA V_{IN+} connected to V/I-3
1	0	0	PGA V_{IN+} connected to V/I-4
1	0	1	PGA V_{IN+} connected to V/I-5
1	1	0	Reserved
1	1	1	Reserved

Table 1. PGA Positive Input Selection

VP2	VP1	VP0	PGA NEGATIVEINPUT
0	0	0	PGA V_{IN-} connected to V/I-0
0	0	1	PGA V_{IN-} connected to V/I-1
0	1	0	PGA V_{IN-} connected to V/I-2
0	1	1	PGA V_{IN-} connected to V/I-3
1	0	0	PGA V_{IN-} connected to V/I-4
1	0	1	PGA V_{IN-} connected to V/I-5
1	1	0	Reserved
1	1	1	Reserved

Table 2. PGA Negative Input Selection