Register 0—Control Register 1 (address = 0x00) (Read/Write)

BIT #	D7	D14	D6	D5	D4	D3	D2	D1	D0
BIT Name	RST	CSE	0	0	0	0	0	0	0

Bit Descriptions

RST: Reset (Bit 7)
If the RST bit is set to ‘1’ in a write operation, all the registers in the XTR108 will be returned to their power-on reset condition. The RST bit will always read as a ‘0’.

CSE: Checksum Error (Bit 6)
The checksum error bit is read only and will be set to ‘1’ if a checksum error has been detected. This bit is cleared by a reset operation or by detection of a valid checksum.

Reserved (Bits 5-0)
These bits are reserved and must be set to ‘0’.