6.2.5 Register 4: PGA Coarse Offset Adjust and Gain Select/Output Amplifier Gain Select Register (Read/Write, Address Pointer = 00100)

Bit #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	0WD	GO2	GO1	GO0	GI3	GI2	GI1	GI0	RFB	RFB	RFB	OS4	OS3	OS2	OS1	OS0
POR Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit Descriptions:

OWD: **One-Wire Disable (only valid while V_{OUT} is enabled, for use when PRG is connected to V_{OUT})**
1 = Disable
0 = Enable

GO[2:0]: **Output Amplifier Gain Select, 1-of-7 plus internal feedback disable**

GI[3:0]: **Front-End PGA Gain Select, 1-of-8, and Input Mux Control**
GI[3] = Input Mux Control
GI[2:0] = Gain Select

RFB: **Reserved Factory Bit: Set to zero for proper operation**

OS[4:0]: **Coarse Offset Adjust on Front-End PGA, 4-bit + sign**
1LSB = $(V_{REF})(0.85E - 3)$

Table 6−7. Output Amplifier—Gain Select

GO2 [14]	GO1 [13]	GO0 [12]	Output Amplifier Gain
0	0	0	2
0	0	1	2.4
0	1	0	3
0	1	1	3.6
1	0	0	4.5
1	0	1	6
1	1	0	9
1	1	1	Disable Internal Feedback

Table 6−8. Front End PGA—Gain Select

GI3 MUX CNTL [11]	GI2 GAIN SEL2 [10]	GI1 GAIN SEL1 [9]	GI0 GAIN SEL0 [8]	Input MUX State(1)	Front-End PGA Gain
0	0	0	0	$V_{IN1} = V_{INP}$, $V_{IN2} = V_{INN}$	4
0	0	0	1	$V_{IN1} = V_{INP}$, $V_{IN2} = V_{INN}$	8
0	0	1	0	$V_{IN1} = V_{INP}$, $V_{IN2} = V_{INN}$	16
0	0	1	1	$V_{IN1} = V_{INP}$, $V_{IN2} = V_{INN}$	23.27
0	1	0	0	$V_{IN1} = V_{INP}$, $V_{IN2} = V_{INN}$	32
0	1	0	1	$V_{IN1} = V_{INP}$, $V_{IN2} = V_{INN}$	42.67
0	1	1	0	$V_{IN1} = V_{INP}$, $V_{IN2} = V_{INN}$	64
0	1	1	1	$V_{IN1} = V_{INP}$, $V_{IN2} = V_{INN}$	128
1	0	0	0	$V_{IN1} = V_{INN}$, $V_{IN2} = V_{INP}$	−4
1	0	0	1	$V_{IN1} = V_{INN}$, $V_{IN2} = V_{INP}$	−8
1	0	1	0	$V_{IN1} = V_{INN}$, $V_{IN2} = V_{INP}$	−16
1	0	1	1	$V_{IN1} = V_{INN}$, $V_{IN2} = V_{INP}$	−23.27
1	1	0	0	$V_{IN1} = V_{INN}$, $V_{IN2} = V_{INP}$	−32
1	1	0	1	$V_{IN1} = V_{INN}$, $V_{IN2} = V_{INP}$	−42.67
1	1	1	0	$V_{IN1} = V_{INN}$, $V_{IN2} = V_{INP}$	−64
1	1	1	1	$V_{IN1} = V_{INN}$, $V_{IN2} = V_{INP}$	−128

(2) V_{IN1} = Pin 4, V_{IN2} = Pin 5, V_{INP} = positive input to Front-End PGA, V_{INN} = negative input to Front-End PGA; see detailed block diagram (Figure B−1 on page B-2).

Table 6−9. Coarse Offset Adjust on Front-End PGA—Data Format Example (V_{REF} = +5V)

OS4 [4]	OS3 [3]	OS2 [2]	OS1 [1]	OS0 [0]	Coarse Offset (mV)	Coarse Offset
1	1	1	1	1	−59.5	$-14(V_{REF})(0.85E-3)$
1	1	1	1	0	−55.25	$-13\ (V_{REF})(0.85E-3)$
1	1	1	0	1	−51	$-12\ (V_{REF})(0.85E-3)$
1	1	1	0	0	−46.75	$-11\ (V_{REF})(0.85E-3)$
1	1	0	1	1	−42.5	$-10\ (V_{REF})(0.85E-3)$
1	1	0	1	0	−38.25	$-9\ (V_{REF})(0.85E-3)$
1	1	0	0	1	−34	$-8(V_{REF})(0.85E-3)$
1	1	0	0	0	−29.75	$-7\ (V_{REF})(0.85E-3)$
1	0	1	1	1	−29.75	$-7\ (V_{REF})(0.85E-3)$
1	0	1	1	0	−25.5	$-6\ (V_{REF})(0.85E-3)$
1	0	1	0	1	−21.25	$-5\ (V_{REF})(0.85E-3)$
1	0	1	0	0	−17	$-4\ (V_{REF})(0.85E-3)$
1	0	1	0	1	−12.75	$-3\ (V_{REF})(0.85E-3)$
1	0	0	1	0	−8.5	$-2\ (V_{REF})(0.85E-3)$
1	0	0	0	1	−4.25	$-1\ (V_{REF})(0.85E-3)$
1	0	0	0	0	0	$0V_{REF}$
0	0	0	0	0	0	$0V_{REF}$
0	0	0	0	1	+4.25	$+1\ (V_{REF})(0.85E-3)$
0	0	0	1	0	+8.5	$+2\ (V_{REF})(0.85E-3)$
0	0	0	1	1	+12.75	$+3\ (V_{REF})(0.85E-3)$
0	0	1	0	0	+17	$+4\ (V_{REF})(0.85E-3)$
0	0	1	0	1	+21.25	$+5\ (V_{REF})(0.85E-3)$
0	0	1	1	0	+25.5	$+6\ (V_{REF})(0.85E-3)$
0	0	1	1	1	+29.75	$+7\ (V_{REF})(0.85E-3)$
0	1	0	0	0	+29.75	$+7\ (V_{REF})(0.85E-3)$
0	1	0	0	1	+34	$+8\ (V_{REF})(0.85E-3)$
0	1	0	1	0	+38.25	$+9\ (V_{REF})(0.85E-3)$
0	1	0	1	1	+42.5	$+10\ (V_{REF})(0.85E-3)$
0	1	1	0	0	+46.75	$+11\ (V_{REF})(0.85E-3)$
0	1	1	0	1	+51	$+12\ (V_{REF})(0.85E-3)$
0	1	1	1	0	+55.25	$+13\ (V_{REF})(0.85E-3)$
0	1	1	1	1	+59.5	$+14\ (V_{REF})(0.85E-3)$