

### 6.2.2 Register 1: Fine Offset Adjust (Zero DAC) Register (Read/Write, Address Pointer = 00001)

Bit #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	ZD15	ZD14	ZD13	ZD12	ZD11	ZD10	ZD9	ZD8	ZD7	ZD6	ZD5	ZD4	ZD3	ZD2	ZD1	ZD0
POR Value	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

#### Bit Descriptions:

**ZD[15:0]: Zero DAC control, 16-bit unsigned data format**

Table 6-4. Zero DAC—Data Format Example ( $V_{REF} = +5V$ )

Digital Input (Hex)	Digital Input ZD15.....ZD0 (Binary)	Zero DAC Output (V)	Zero DAC Output
0000	0000 0000 0000 0000	0	0 $V_{REF}$
0001	0000 0000 0000 0001	0.00007629	(1/65536) $V_{REF}$
051F	0000 0101 0001 1111	0.100021362	0.02 $V_{REF}$ <sup>(1)</sup>
4000	0100 0000 0000 0000	1.25	0.25 $V_{REF}$
8000	1000 0000 0000 0000	2.5	0.50 $V_{REF}$
C000	1100 0000 0000 0000	3.75	0.75 $V_{REF}$
FAE1	1111 1010 1110 0001	4.899978638	0.98 $V_{REF}$ <sup>(1)</sup>
FFFF	1111 1111 1111 1111	4.999923706	0.9999847 $V_{REF}$

(1) Ensured by design Zero DAC Range of Adjustment (0.02 $V_{REF}$  to 0.98 $V_{REF}$ )

#### Zero DAC Equation:

$$\begin{aligned} \text{Decimal # Counts} &= (V_{ZERO\ DAC}/V_{REF})(65536) \\ 0.1V \leq \text{Zero DAC Analog Range} &\leq V_{SA} - 0.1V \\ 0 \leq \text{Zero DAC Programming Range} &\leq V_{REF} \end{aligned}$$

#### Zero DAC Example:

$$\begin{aligned} \text{Want: } V_{ZERO\ DAC} &= 0.5V \\ \text{Given: } V_{REF} &= 5V \\ \text{Decimal # Counts} &= 0.5 / (5/65536) = 6553.6 \\ \text{Use 6554 counts} &\rightarrow 199Ah \rightarrow 0001\ 1001\ 1001\ 1010 \end{aligned}$$