

J7 Interrupt Architecture

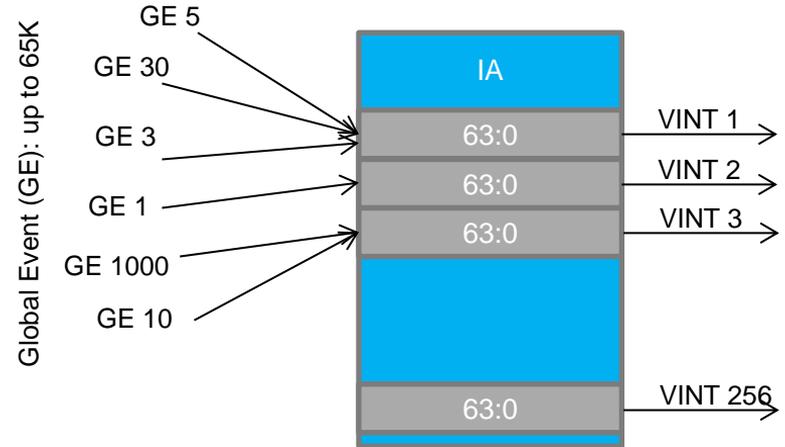
K3 Processors
18th March 2019
V1.0

Agenda

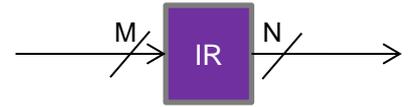
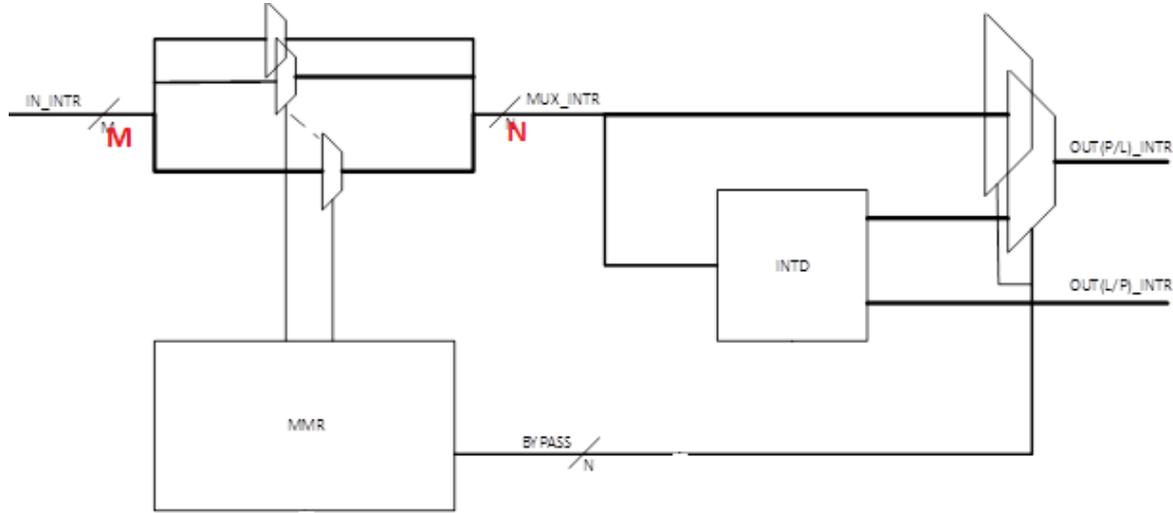
- Understanding Interrupt Aggregator
- Understanding Interrupt Router
- J721E Interrupt Architecture
 - MCU/Wakeup Domain
 - ARMSS0
 - ARMSS1
 - C66x 0/1
 - Compute Cluster: A72, C7x

Interrupt Aggregator (IA)

- For each received event, the IA performs a lookup into an interrupt mapping table which specifies:
 - Interrupt Status Register Number (regnum) – up to 256
 - Interrupt Status Bit Number (bitnum) – up to 64 per register
- Provides option to enable, disable and clear status per status bit (event)
 - Can generate interrupt through Interrupt Router (IR) via Virtual Interrupts (VINT)
 - SW can poll on these bits without interrupt as well

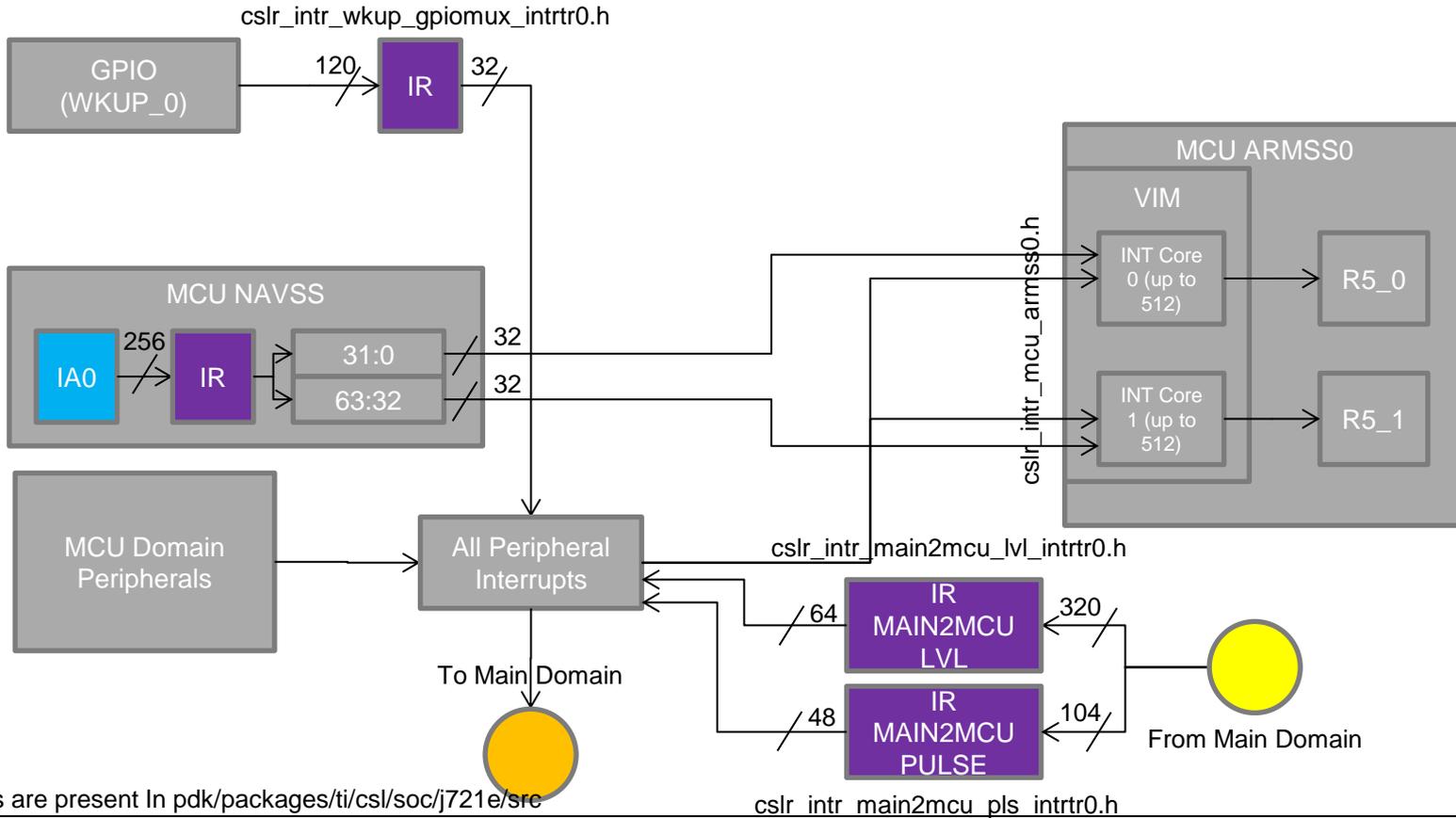


Interrupt Router (IR)



- Interrupt Router is a M to N mux

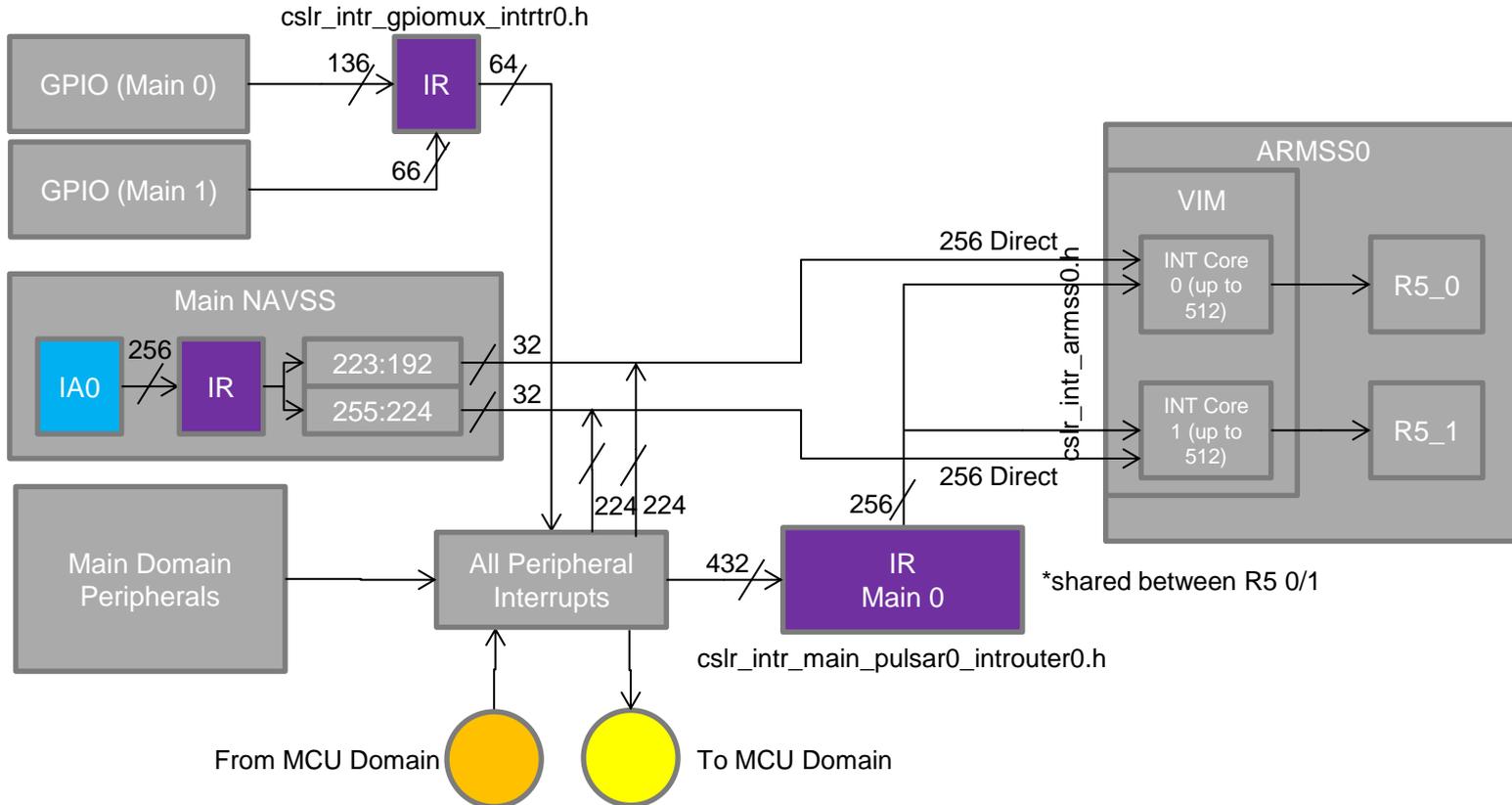
J721E Interrupt Architecture – MCU/Wakeup Domain



cslr files are present in `pdk/packages/ti/csl/soc/j721e/src`

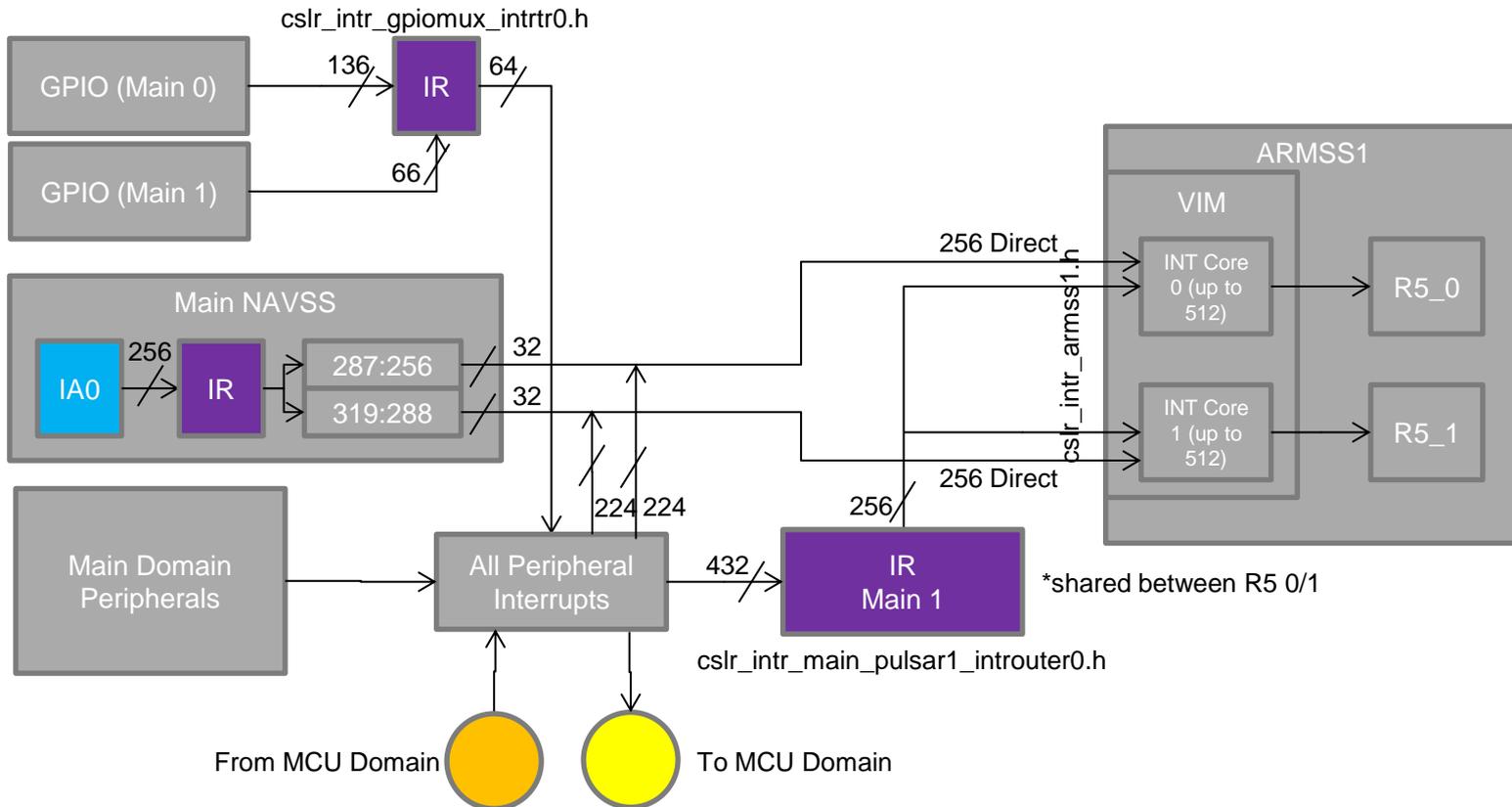
`cslr_intr_main2mcpu_pls_intrtr0.h`

J721E Interrupt Architecture – Main Domain: ARMSS0



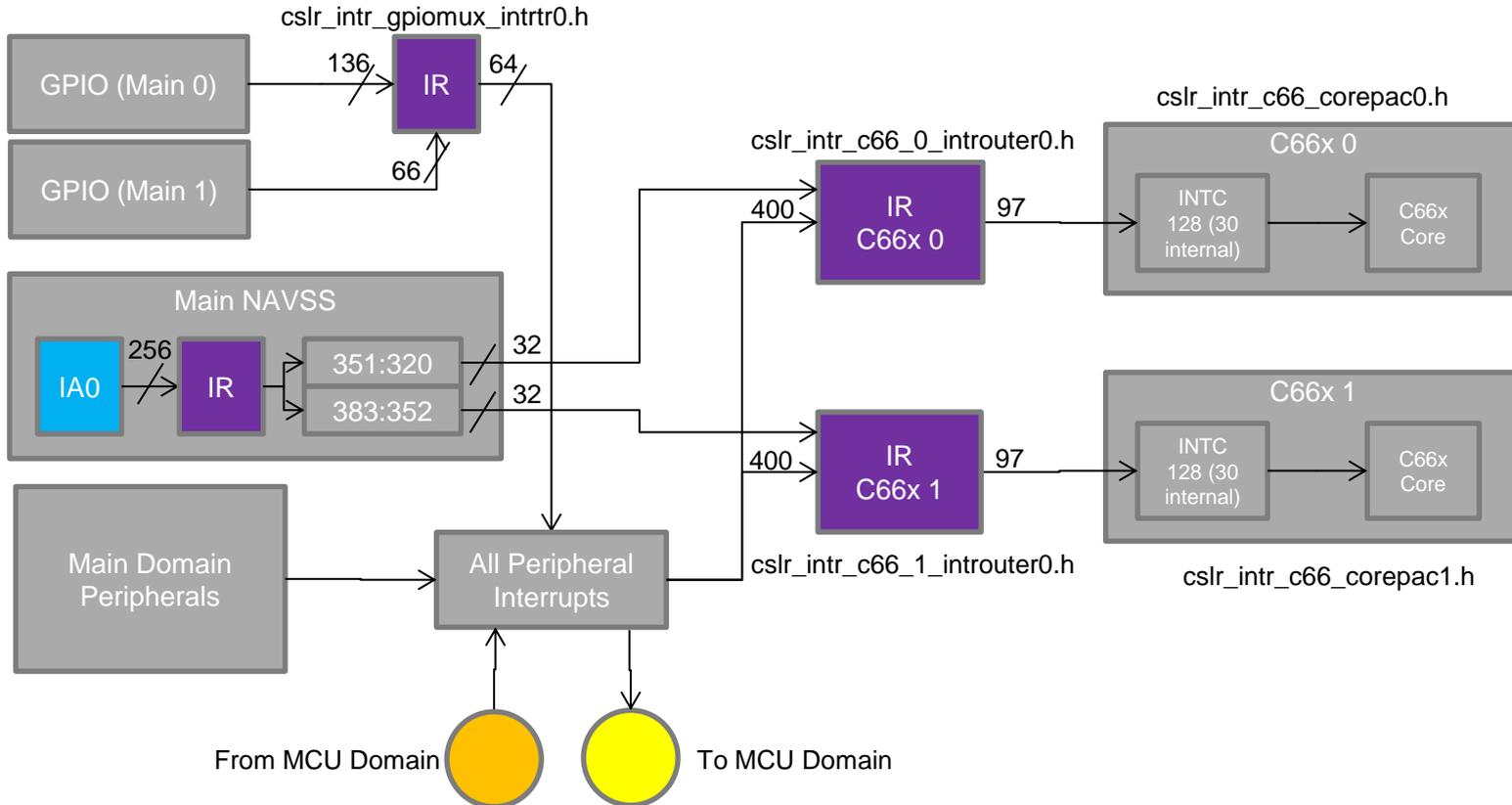
cslr files are present in `pdk/packages/ti/csl/soc/j721e/src`

J721E Interrupt Architecture – Main Domain: ARMSS1



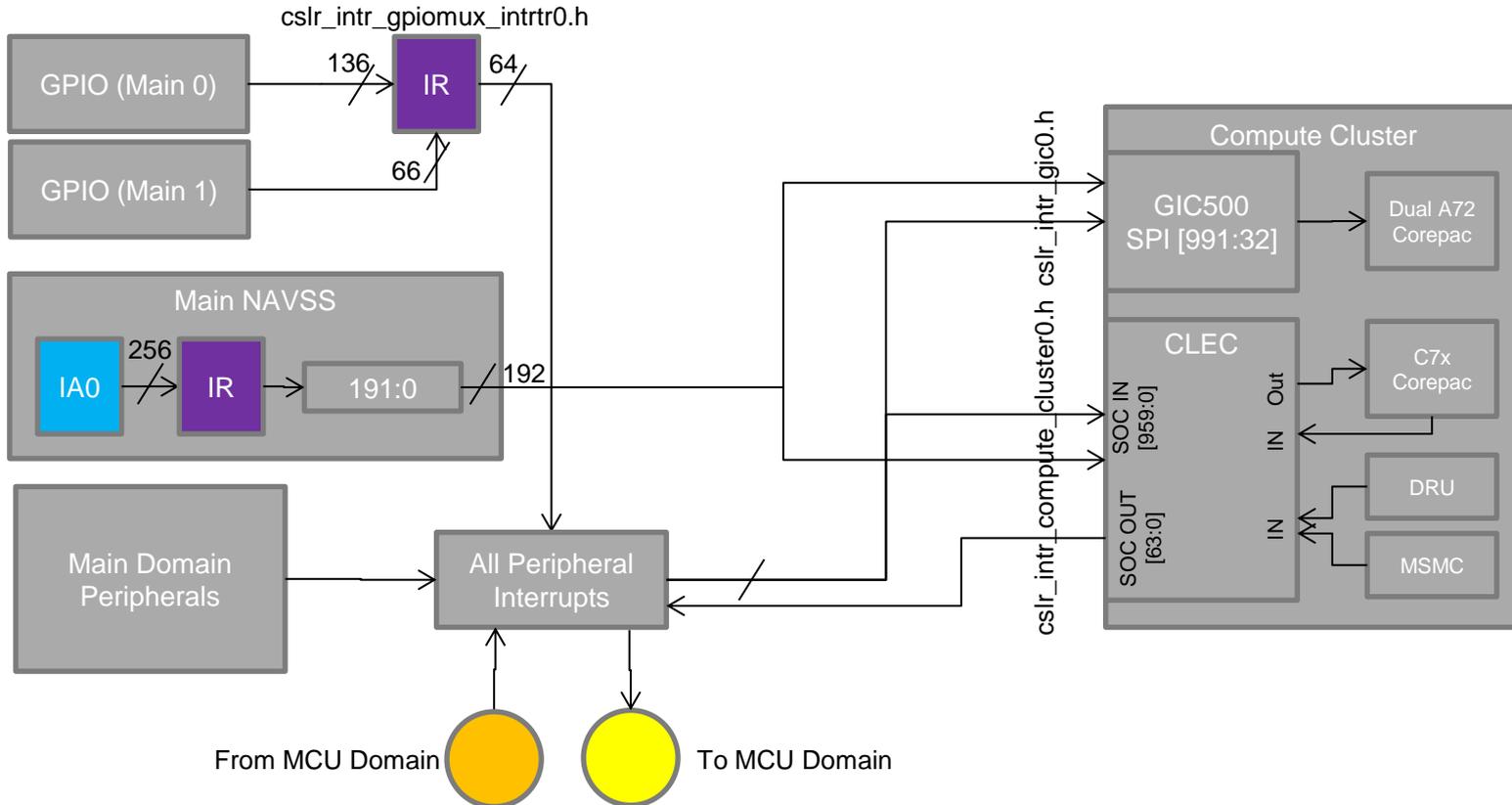
cslr files are present in `pdk/packages/ti/csl/soc/j721e/src`

J721E Interrupt Architecture – Main Domain: C66x 0/1



cslr files are present in `pdk/packages/ti/csl/soc/j721e/src`

J721E Interrupt Architecture – Main Domain: A72/C7x



cslr files are present in `pdk/packages/ti/csl/soc/j721e/src`



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