EtherCAT : Errata for Industrial SDK 1.1.0.3

For application developers: Known Issues/Limitations

Single datagram accessing multiple FMMU mapped areas using LRD/LWR commands

- Issue/ Failure Description or state
  - SDOCM00092510 : Single datagram accessing multiple FMMU mapped areas in a single slave will only update the data corresponding to first FMMU in datagram
- Conditions in which failures occur
  - Single datagram accessing multiple FMMU mapped areas in single slave.

    FMMU0(0x1000:0x1007)->SM2 (Write SM)

    FMMU1(0x1000:0x1007)->SM3 (Read SM)

    FMMU2(0x1008:0x100F)->SM4 (Write SM)

    FMMU3(0x1008:0x100F)->SM5 (Read SM)
    - Single LRD to access (0x1000:100F) will only access SM3
    - Single LWR to access (0x1000:100F) will only access SM2
    - 2 LRD/LWRs are required in this case to access both pair of SMs - LRD1/LWR1(0x1000:0x1007) and LRD2/LWR2(0x1008:0x100F)
- Root cause
  - Increased code memory requirements in firmware to implement this support
- Work around
  - For above example instead of one LRD datagram to logical address 0x1000 and length 16, master needs to send two LRD datagrams, one to logical address 0x1000 and length 8 second to logical address 0x1008 and length 8 or use LRW in place of LRD/LWR which is more efficient for most of the use cases

NOTE: This issue will not be fixed

LRW access to non-interleaved input and output process data of multiple slaves does not work

- Issue/ Failure Description or state
  - SDOCM00105048: LRW access to non-interleaved input and output process data of multiple slaves does not work. SOEM accesses slaves in LRW mode this way
- Conditions in which failures occur
  - Single LRW datagram accessing FMMU mapped areas in multiple slaves and PD out is mapped
    FMMU0(0x1000:0x1007)->SM2 #1(Write SM) FMMU1(0x1008:0x100F)->SM2#2 (Write SM)
    FMMU2(0x1010:0x1017)->SM3 #1 (Read SM) FMMU3(0x1018:0x101F)->SM3#2(Read SM)
    - Single LRW access from (0x1000:101F)
- Root cause
  - Increased code memory requirements in firmware to implement this support as well as non-interleaved access I/O data is not a very optimal use of EtherCAT – it increases the cycle time overhead/datagram size and not effective use of LRW datagram which can perform read and write in the same cycle.
- Work around
  - Use LRD/LWR datagram to access process data
  - Use LRW datagram to access process data
    - Input and output overlaid on the same logical address range (TwinCAT usage)
    - Input and output of a given slave back to back in logical address space
      - FMMU0(0x1000:0x1007)->SM2 #1(Write SM) FMMU1(0x1008:0x100F)->SM3#1 (Read SM)
      - FMMU2(0x1010:0x1017)->SM2 #2 (Write SM) FMMU3(0x1018:0x101F)->SM3#2 (Read SM)

NOTE: This issue will not be fixed

SYNC0 jitter increases with distance of slave from reference

- Issue/ Failure Description or state
  - SDOCM00097012 : SYNC0 jitter increases with distance of slave from reference
- Conditions in which failures occur
  - TI ESC in a large network of slaves and away from reference slave shows variable jitter which increases with distance of the slave
- Root cause
  - Drift compensation algorithm in firmware requires optimization

NOTE: This issue will be addressed in subsequent releases

LRD access on unused registers

- Issue/ Failure Description or state
  - SDOCM00098950: LRD access on unused registers results in WKC increment
- Conditions in which failures occur
  - LRD access on unused registers result in WKC increment
- Root cause
  - Firmware does not support register protection in LRD mode at this moment, it requires more firmware footprint to support, this minor spec compliance does not justify the footprint increase and no Write Only registers in ESC

NOTE: This issue will not be fixed

PD/PDI watchdog counter issue

- Issue/ Failure Description or state
  - SDOCM00098105: PDI/PD watchdog counter incremented by 1 whenever PDI/PD watchdog is disabled using EtherCAT master
- Conditions in which failures occur
  - Whenever EtherCAT master disables WD by writing zero to respective Watchdog Time registers (0x410:0x411 or 0x420:0x421)
- Root cause
  - This is PRU-ICSS h/w behavior

NOTE: This issue will be not be fixed

Enhanced link detection bit not updated in port status 0x110 bit2

- Issue/ Failure Description or state
  - SDOCM00105357: Enhanced link detection bit not updated in port status 0x110 bit2 even after enabling the same in 0x141
- Conditions in which failures occur
  - When enhanced link detection is enabled by setting 0x141 Bit1 or Bit4 or Bit 5 in EEPROM
- Root cause
  - There was a timing issue due to which EEPROM loaded register configuration was overwritten PRU firmware which is loaded a bit later in the sequence

NOTE: This issue will be fixed in 1.1.0.4

SM Watchdog status reads "expired" when no output process data is configured

- Issue/ Failure Description or state
  - SDOCM00106812: SM Watchdog status reads "expired" when no output process data is configured and SM WD is enabled for input SM
- Conditions in which failures occur
  - Configure ESC for Process data input only mode and take to operational state
- Root cause
  - Firmware does not trigger SM WD for input SM even if its enabled via SM control register

NOTE: This issue will be fixed in 1.1.0.4

For stack integrators: Known Issues/Limitations

Unable to go to OP state with SYNC1 enabled (DC mode)

- Issue/ Failure Description or state
  - SDOCM00106811: Unable to go to OP state with SYNC1 enabled (DC mode) - appeared after applying SSC5.10 bugfix posted in EtherCAT forum
- Conditions in which failures occur
  - When SYNC1 is enabled and EtherCAT forum patch dated 21st Feb 2014 for SSC5.10 applied “DC mode state transition issue without DC sync enabled at slave - slave incorrectly transitions to OP state without this fix”
- Root cause
  - SYNC1 watchdog counter does not get reset with ENABLE_SYNC_TASK enabled (SYNC ISR handling in task context)

NOTE: This issue will be fixed in 1.1.0.4