

LMX9830 Bluetooth Serial Port Module Firmware Release Notes

Texas Instruments
Firmware Release Notes
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Revision 1.4



Introduction

The Texas Instruments® LMX9830 Bluetooth™ Serial Port module is a highly integrated radio, baseband controller and memory device. All hardware and the on-chip ROM firmware is included to provide a complete solution from antenna through the complete lower and upper layers of the Bluetooth stack, up to the application including the Generic Access Profile (GAP), the Service Discovery Application Profile (SDAP), and the Serial Port Profile (SPP). The module includes a configurable service database to fulfil service requests for additional profiles on the host.

LMX9830 is optimized to handle the data and link management processing requirements of a Bluetooth node. The firmware supplied within this device offers a complete Bluetooth (v2.0) stack including profiles and command interface. This firmware features point-to-point and point-to-multipoint link management supporting data rates up to the theoretical maximum over RFCOMM of 704 kbps. The internal memory supports up to 7 active Bluetooth data links and 1 active SCO link.

Due to our continuously ongoing quality tests and firmware improvements, several changes to the firmware have been made to provide highest reliability and performance.

This document describes all release changes within the LMX9830 firmware.

This document is based on:

Table 0-1. LMX9830 Module configuration

Item	Version
Hardware	LMX9830
Firmware	v2.12 and previous
Actual Firmware Release in production	v2.12

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1.0 Key considerations on converting from 2.10 to 2.12

Since the LMX9830 is ROM based, firmware upgrades can only be done by complete ROM spins, which result in a new chip delivered by Texas Instruments.

The following considerations should be kept in mind from the software developer, to prepare the host software for future upgrades of the LMX9830 ROM code. Texas Instruments of course will try keep backwards compatibility at 100%, to avoid compatibility problems in replacing existing devices in your products.

However, some important issues need to be considered in software.

1.1 FIRMWARE VERSION IN READY EVENT

Each LMX9830 comes up with a certain “Ready” Event, which indicates the completed boot process of the device. This event also includes the firmware version of the device. The “Ready” appears after boot or after a software reset.

See Figure 1-1 for a screenshot of the event in Simply Blue Commander.

For example, the LMX9830 will come up with the hexadecimal code

Rx(RAW): 02,69,25,05,00,93,04,**30,32,31,32**,03

on which the bold bytes indicate the firmware version (in this case 0212).

In order to avoid any future upgrade problems, please make sure your software does not use this parameter as part of the decision to continue. The parameter should just be used for informational purposes.

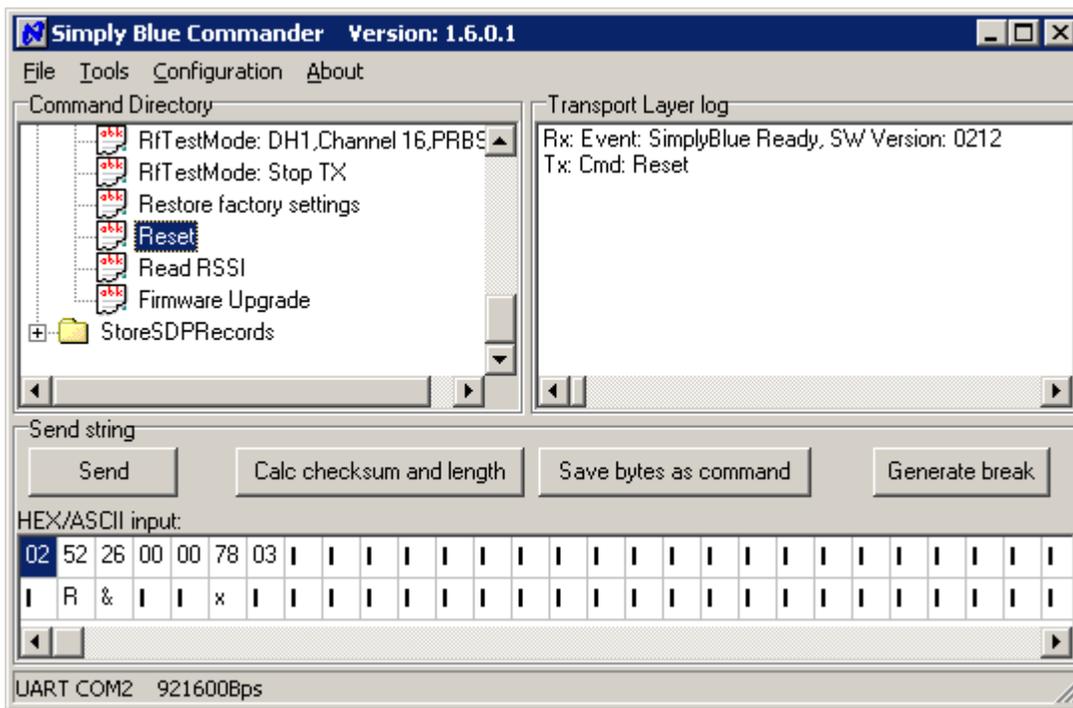


Figure 1-1. “SimplyBlue Ready” in Simply Blue Commander

1.2 PATCHES

The LMX9830 includes the functionality of patching, which allows small bug fixing and firmware modifications. Latest patches are distributed and can be downloaded at the Simply Blue Developers Website at <http://www.ti.com>. Please see Section 4.0 on page 7 for patches available at release of this document.

Since patches are specific to each firmware release, the patches should only be applied to those devices. To avoid, that a wrong patch is applied to the firmware, the patch includes the firmware version information, which is verified by the LMX9830 firmware at the beginning of the patching process.

1.2.1 Patching with command interface in case of no EEPROM connected

In case no EEPROM is connected, patches need to be supplied via the command interface using the “Write ROM patch” command. Since patches usually require more than one command, the patching requires a specific command flow to be

followed. See Figure 1-2 for the general patch flow. The complete process is also described in the “LMX9830 Software Users Guide”.

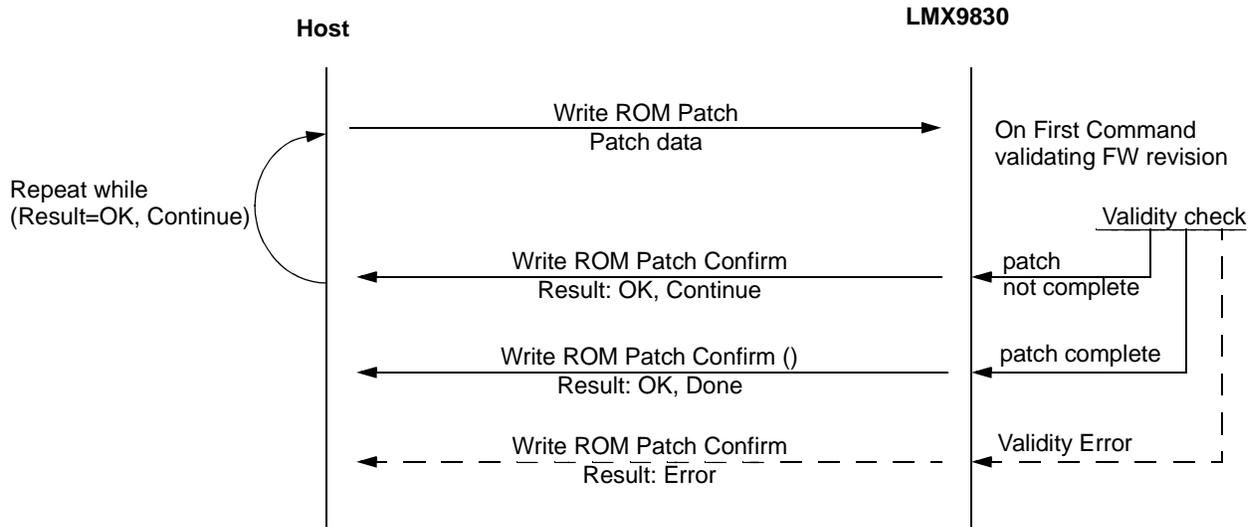


Figure 1-2. Write ROM patch flow

The Write ROM patch mechanism includes a validity check of the ROM pushed to the device. In case, no error is found the error code is either 0x01 for continue or 0x00 for OK, Done.

In case the error code is different to those two, some error must have occurred. The following error codes are defined

- 0x00 = Ok, Done
- 0x01 = Ok, Continue
- 0x80 = Error, Not enough info to continue download (a “global” or “segment” meta data group appears to be split)
- 0x81 = Error, Not enough resources to continue download
- 0x82 = Error, Patch too big
- 0x83 = Error, Unsupported Patch format revision
- 0x84 = Error, Patch not applicable to firmware in device.
- 0x85 = Error, Patch CRC check failed.
- 0x86 = Error, Patch NVS validation failed.
- 0x87 = Error, RAMAddr or VarAddr out of RAM area.
- 0xFF = Error, Unspecified error.

So in case the host tries to apply a patch released for firmware 2.10, to a 2.12 device, the confirm will respond with error message 0x84.

Therefore the software needs to be prepared to handle this error code correctly by either continuing with the normal boot process without the patch, or to try to apply a patch for another firmware version.

To be prepared for future upgrades, the host application should not stop the execution due to this error code.

1.2.2 Patch in pre-programmed EEPROM

The LMX9830 supports the usage of an external EEPROM, in which the patch can be stored and will be fetched on each boot process. Depending on the manufacturing process, the EEPROM may be pre-programmed separately with all NVS parameters, BD_Addr and patch and just placed on the board.

On normal boot-up, the LMX9830 will check the existence of the EEPROM and will apply the data stored.

In case the EEPROM does include a patch, firmware versions newer than 2.10 will ignore the patch in case the firmware versions of patch and hardware do not match. Therefore no change required if replacing LMX9830 with 2.10 firmware by 2.12 or higher.

Example:

Existing design using LMX9830, FW 2.10 with Patch 4. The EEPROM is serialized and pre-programmed on an external programmer with the patch. The firmware will boot up as expected and will apply the patch

In case this LMX9830 will be replaced by a LMX9830 FW 2.12, the patch in the EEPROM will not cause any problems as it will be ignored by the firmware.

NOTE: Problems will only occur if downgrading from 2.12 back to 2.10 (e.g due to old stock) and the EEPROM already contains a patch for 2.12. Since 2.10 does not check the version of the patch stored in the EEPROM, a patch intended for 2.12 will cause a device with 2.10 firmware to malfunction.

1.2.3 Patch in EEPROM, but supplied via command interface

In case the EEPROM is not serialized and pre-programmed separately, the BD_Addr and patch would need to be stored via the command interface from either the host or a manufacturing device.

In case a patch needs to be supplied using the "Write ROM Patch" command, the mechanism to take care of is similar to the flow described in Section 1.2.1. A previously stored patch would be overwritten. Since the patch is stored in EEPROM, this only needs to be done once.

2.0 Known Bugs

2.1 VERSION 2.12

Table 2-1. List of known bugs on firmware v2.12

Bug Type	Description	Workaround
Transmission Problem in command mode	When the module is in command mode, Data pending are not flushed when the RFCOMM connection is terminated by link timeout.	Patch 2
SDAP_SERVICE_RE QUEST command confirm wrong	Confirm includes additional wrong byte after the correct handle on position 3+4*Length (Last byte of payload).	Ignore Last Payload Byte

2.2 VERSION 2.10

Table 2-2. List of known bugs on firmware v2.10

Bug type	Description	Workaround
Transmission Problem in command mode	When the module is in command mode, Data pending are not flushed when the RFCOMM connection is terminated by link timeout.	Patch 8
Memory leak with no EEPROM	If no EEPROM connected, numerous number of write NVS events can cause the device to crash due to memory overflow	Patch 2
Store SDP delay	If more than 2 SDP records created, a delay of about 1 second in between is needed or the records will not be created	Patch 2
Start delay with no EEPROM	A delay from about 3 seconds from POWER ON is needed if no EEPROM is connected	No Patch available
No Enhanced Power Management after link release	The module does not switch to 32 khz when the transport layer is switched off after a connection has been established and disconnected again	Software workaround possible. See Section 3.1 "Power Management" on page 6.
Local loop back non functional	Local loop back does not work	No Patch available

3.0 Workarounds

3.1 POWER MANAGEMENT

Valid for v2.10: To fix this issue, either do a Reset **before** Transport Layer Disable, or send the following command **before** TL Disable and **after** all ACL links have been disconnected:

```
02 52 71 06 00 C9 F5 47 0E 00 01 00 03
```

4.0 Firmware Release History

4.1 VERSION 2.12

Release date: January 2006

Please see Section 1.0 "Key considerations on converting from 2.10 to 2.12" on page 2 for details to consider if replacing LMX9830 v2.10 with LMX9830 v2.12 in an existing product.

Table 4-1. Firmware Release Changes 2.12

Issue	Type	Description
Memory leak with no EEPROM	Bug fix	If no EEPROM connected, numerous number of write NVS events could cause the device to crash due to memory overflow
Store SDP delay	Bug fix	If more than 2 SDP records created, a delay of about 1 second in between was needed or the records will not be created
Start delay with no EEPROM	Bug fix	A delay from about 3 seconds from POWER ON was needed if no EEPROM was connected
No Enhanced Power Management after link release	Bug fix	The module did not switch to 32 khz when the transport layer is switched off after a connection has been established and disconnected again
Local loop back non functional	Bug fix	Local loop back did not work
Detection of wrong Patch in EEPROM	New feature	Patches in EEPROM will not be applied in case the firmware versions don't match

4.1.1 Patch 2

Release date: July 2006

Table 4-2. Firmware Patch 2 v2.12 changes

Issue	Type	Description
Transmission Problem in command mode when link terminated by link timeout	Bug Fix	When the module is in command mode, Data pending are not flushed when the RFCOMM connection is terminated by link timeout. This could cause the device to be stucked.

4.1.2 Patch 1 (Internal use)

Release date: January 2006

Table 4-3. Firmware Patch 1 v2.12 changes

Issue	Type	Description
None	Validation	Internal use. Test Patch for validation

4.2 VERSION 2.10

Release date: September 2005

Table 4-4. Firmware Release Changes 2.10

Issue	Type	Description
Initial Release		

4.2.1 Patch 8

Release date: July 2006

This Patch combines all changes from Patch 4 and the RFCOMM bug fix.

Table 4-5. Firmware Patch 8 v2.10 changes

Issue	Type	Description
Transmission Problem in command mode when link terminated by link timeout	Bug Fix	When the module is in command mode, Data pending are not flushed when the RFCOMM connection is terminated by link timeout. This could cause the device to be stucked.
Memory leak with no EEPROM	Bug fix	If no EEPROM used, Numerous write NVS events can cause device to crash due to memory overflow
Store SDP delay	Bug fix	If more than 2 SDP records created, a delay of about 1 second in between is needed or the records will not be created
Radio register initialization change	New feature	Change of Register initialization to enable possibility Enhanced Power Management (32 khz usage) with external crystal (instead of TCXO)

4.2.2 Patch 7 (internal use)

Release date: April 2006

Table 4-6. Firmware Patch 7 v2.10 changes

Issue	Type	Description
None	Validation	Internal use.

4.2.3 Patch 6 (internal use)

Release date: April 2006

Table 4-7. Firmware Patch 6 v2.10 changes

Issue	Type	Description
None	Validation	Internal use.

4.2.4 Patch 5 (internal use)

Release date: September 2005

Table 4-8. Firmware Patch 5 v2.10 changes

Issue	Type	Description
None	Validation	Internal use.

4.2.5 Patch 4

Release date: September 2005

This Patch groups the updates from Patch 2 and Patch 3

Table 4-9. Firmware Patch 4 v2.10 Changes

Issue	Type	Description
Memory leak with no EEPROM	Bug fix	If no EEPROM used, Numerous write NVS events can cause device to crash due to memory overflow
Store SDP delay	Bug fix	If more than 2 SDP records created, a delay of about 1 second in between is needed or the records will not be created
Radio register initialization change	New feature	Change of Register initialization to enable possibility Enhanced Power Management (32 khz usage) with external crystal (instead of TCXO)

4.2.6 Patch 3

Release date: September 2005

Table 4-10. Firmware Patch 3 v2.10 Changes

Issue	Type	Description
Radio register initialization change	New feature	Change of Register initialization to enable possibility Enhanced Power Management (32 khz usage) with external crystal (instead of TCXO)

4.2.7 Patch 2

Release date: September 2005

Table 4-11. Firmware Patch 2 v2.10 Changes

Issue	Type	Description
Memory leak with no EEPROM	Bug fix	If no EEPROM used, Numerous write NVS events can cause device to crash due to memory overflow
Store SDP delay	Bug fix	If more than 2 SDP records created, a delay of about 1 second in between is needed or the records will not be created

4.2.8 Patch 1 (internal use)

Release date: September 2005

Table 4-12. Firmware Patch 1 v2.10 Changes

Issue	Type	Description
none	validation	Internal use. Test patch for validation

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