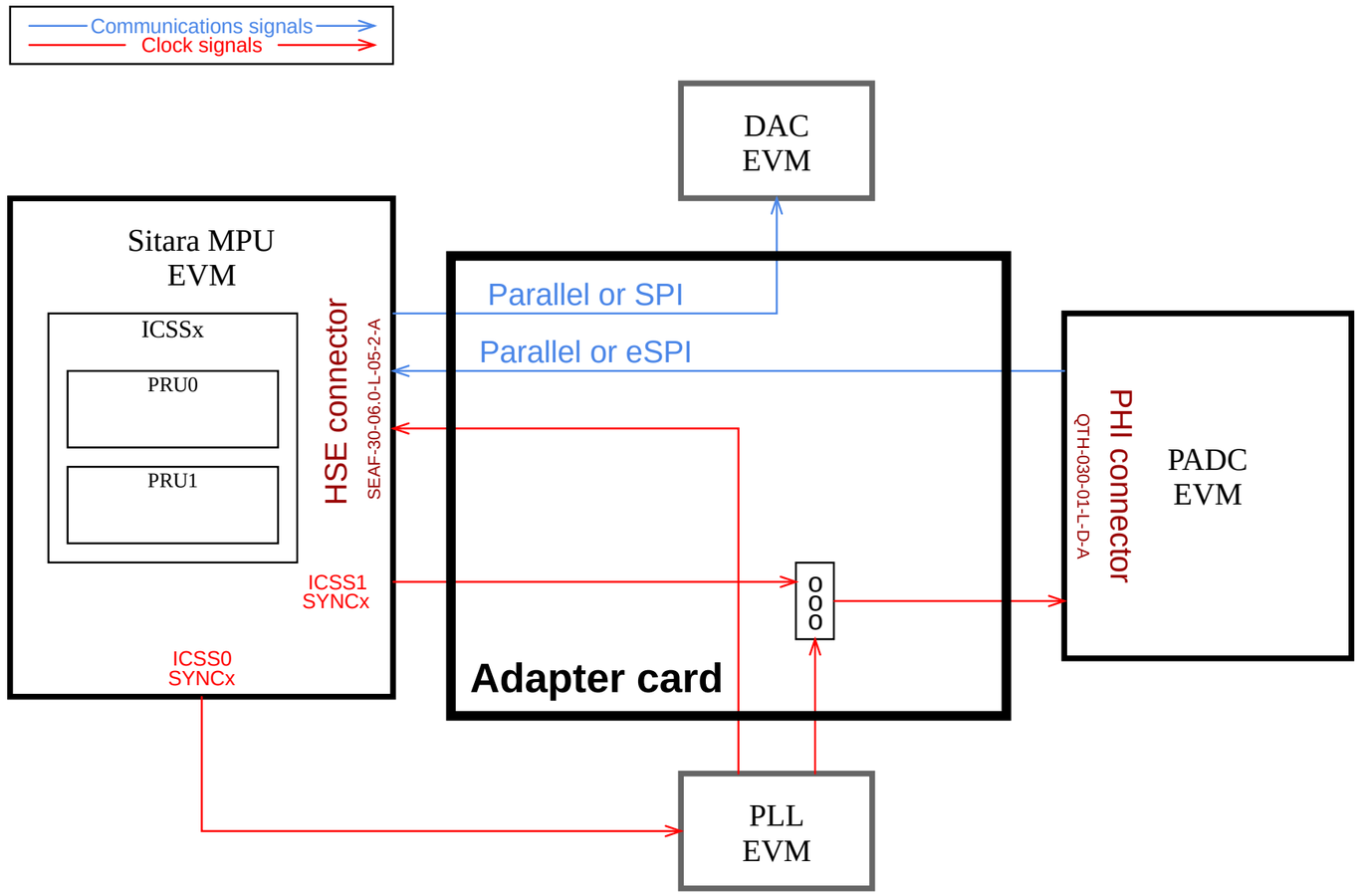

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Orderable:		Designed for:	Mod. Date: 3/22/2021
TID #:		Project Title: MPU_PADC_adapterBoard	
Number: MPU_PADC	Rev: A	Sheet Title: *	
SVN Rev: Not in version control		Assembly Variant: 001	Sheet: 1 of 5
Drawn By: *		File: MPU_PADC_adapter_coversheet.SchDoc	Size: Letter
Engineer:		Contact:	

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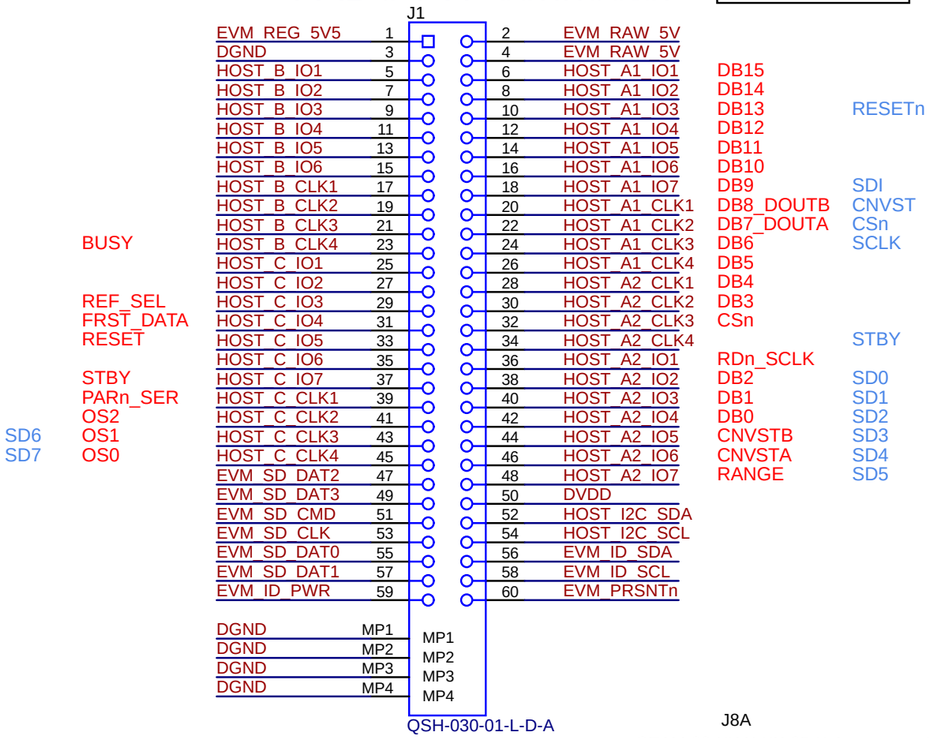
PADC/PHI connector

Parallel i/f signals
eSPI i/f signals

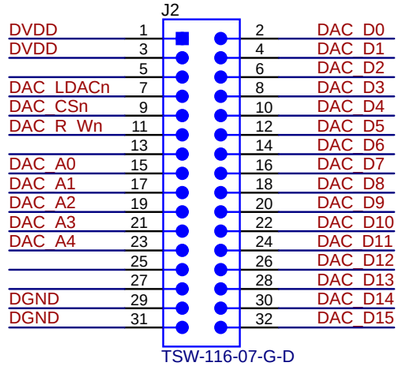


BUSY
REF_SEL
FRST_DATA
RESET
STBY
PARn_SER
OS2
OS1
OS0
SD6
SD7

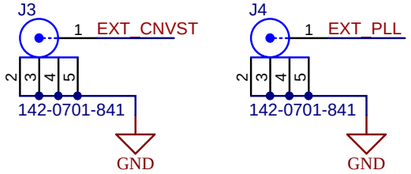
DB15
DB14
DB13
DB12
DB11
DB10
DB9
DB8_DOUTB
DB7_DOUTA
DB6
DB5
DB4
DB3
CSn
RDn_SCLK
DB2
DB1
DB0
CNVSTB
CNVSTA
RANGE

RESETn
SDI
CNVST
CSn
SCLK
STBY
SD0
SD1
SD2
SD3
SD4
SD5

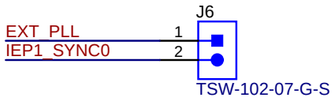
DAC connector



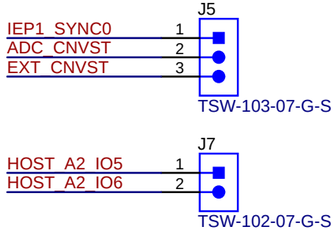
External PLL connectors



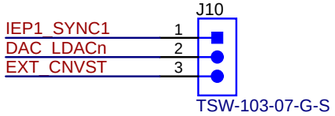
Ext. clock ref.



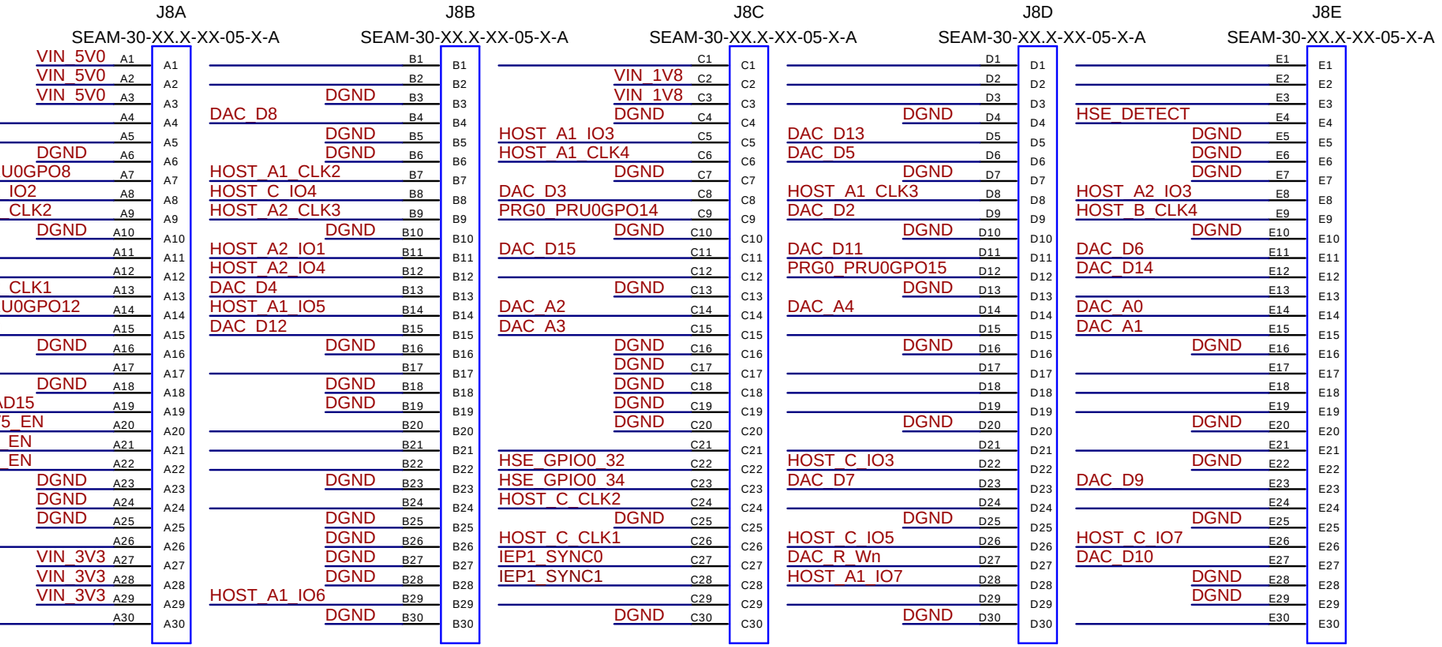
CNVST select

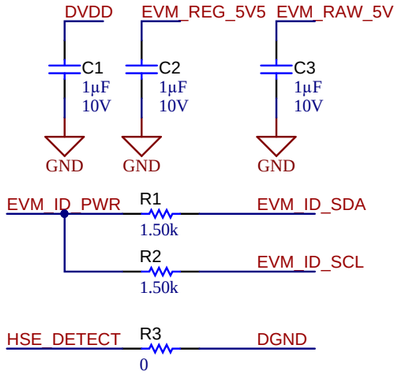


LDAC select



AM64x/HSE connector





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Orderable:		Designed for:	Mod. Date: 6/9/2021
TID #:		Project Title: MPU_PADC_adapterBoard	
Number: MPU_PADC	Rev: A	Sheet Title: *	
SVN Rev: Not in version control		Assembly Variant: 001	Sheet: 2 of 5
Drawn By: *		File: MPU_PADC_adapter_connectors.SchDoc	Size: Letter
Engineer:		Contact:	

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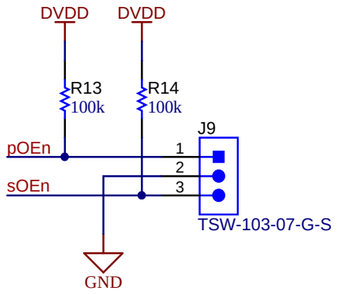
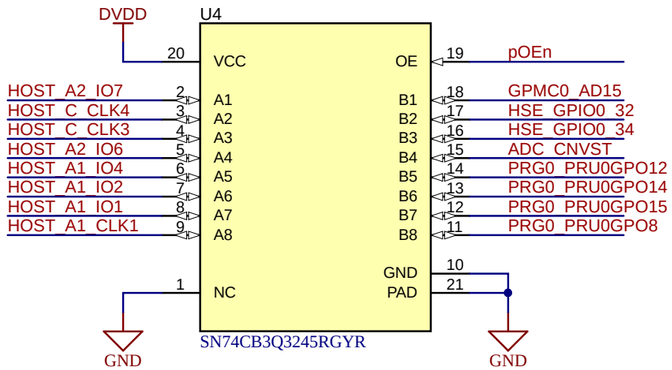
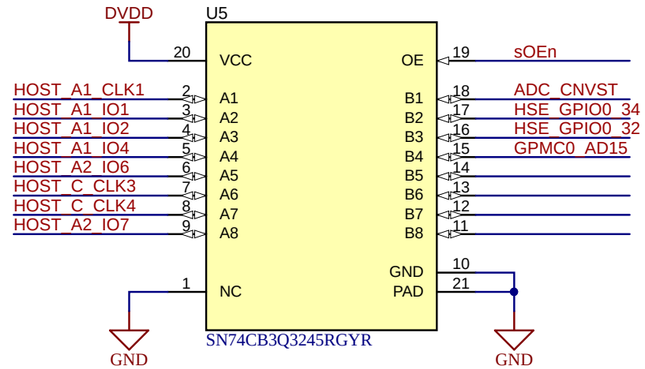




ADC parallel comms signals



ADC eSPI comms signals

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Orderable:		Designed for:	Mod. Date: 3/23/2021
TID #:		Project Title: MPU_PADC_adapterBoard	
Number: MPU_PADC	Rev: A	Sheet Title: *	
SVN Rev: Not in version control		Assembly Variant: 001	Sheet: 3 of 5
Drawn By: *		File: MPU_PADC_adapter_main.SchDoc	Size: Letter
Engineer:		Contact:	

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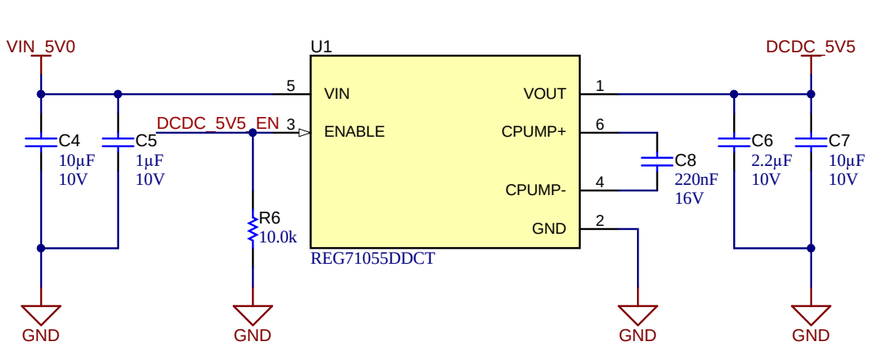

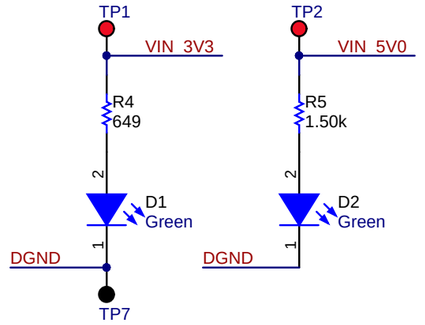

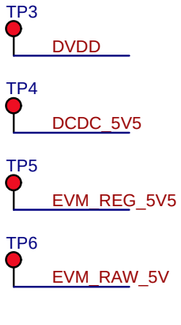

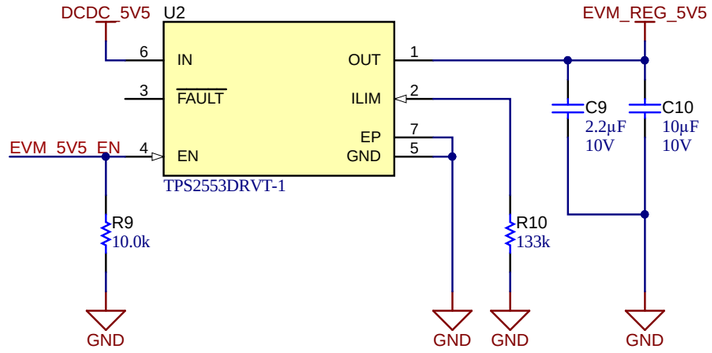

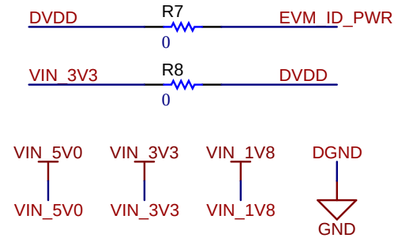

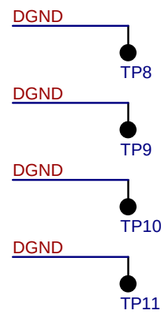

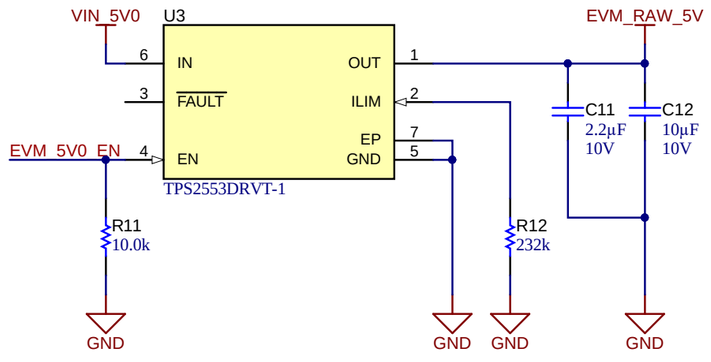

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Orderable:		Designed for:	Mod. Date: 3/23/2021
TID #:		Project Title: MPU_PADC_adapterBoard	
Number: MPU_PADC	Rev: A	Sheet Title: *	
SVN Rev: Not in version control		Assembly Variant: 001	Sheet: 4 of 5
Drawn By: *		File: MPU_PADC_adapter_power.SchDoc	Size: Letter
Engineer:		Contact:	

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H1
NY PMS 440 0025 PH

H2
NY PMS 440 0025 PH

H3
1
NY PMS 440 0025 PH

H4
1
NY PMS 440 0025 PH

SH1 SH2 SH3 SH4 SH5

FID1 FID2 FID3

PCB Number: MPU_PADC
PCB Rev: A

Logo2
PCB LOGO
Texas Instruments

Logo1
CE Mark

Logo3
PCB LOGO
FCC disclaimer

Logo4
PCB LOGO
WEEE logo

Variant/Label Table

Variant	Label Text
001	MPU/PADC adapter card

LBL1
PCB Label
THT-14-423-10
Size: 0.65" x 0.20 "

ZZ1
Assembly Note
These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

ZZ2
Assembly Note
These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ3
Assembly Note
These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ4
Label Assembly Note
This Assembly Note is for PCB labels only

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Orderable:		Designed for:	Mod. Date: 3/23/2021
TID #:		Project Title: MPU_PADC_adapterBoard	
Number: MPU_PADC	Rev: A	Sheet Title: *	
SVN Rev: Not in version control		Assembly Variant: 001	Sheet: 5 of 5
Drawn By: *		File: MPU_PADC_adapter_hardware.SchDoc	Size: Letter
Engineer:		Contact:	

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