VISION SDK on BIOS (v03.06.00)

Data Sheet

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1 Introduction

IMPORANT NOTE:

- This datasheet has performance and feature information about use-cases running on TDA2xx (EVM), TDA2Px (EVM), TDA2Ex (EVM) and TDA3xx (EVM). Many use-cases can be run on multiple SOC/Platforms however the measurement of performance and other metrics is done only on one of these as indicated in the use-case details.

1.1 Framework features

- Compile and build for all CPUs
  - TDA2xx system (IPU1-0, IPU1-1, IPU2, DSP1, DSP2, EVE1, EVE2, EVE3, EVE4, A15_0).
  - TDA2Px system (IPU1-0, IPU1-1, IPU2, DSP1, DSP2, EVE1, EVE2, A15_0).
  - TDA2Ex system (IPU1-0, IPU1-1, IPU2, DSP1, A15_0).
  - TDA3xx system (IPU1-0, IPU1-1, DSP1, DSP2, EVE1).
- Debug and release build profiles.
- Single place to setup memory map
  - Default 512MB DDR
- Ability to create and control links on any CPU.
- Remote log feature with ability to print logs from all CPUs to UART controlled by IPU1-0.
- CPU load profiling for all cores.
- Memory usage log for all cores.
- Run time use-cases performance statistics like frame-rate, latency, frame-drop.
- Exception handler log for IPU, DSP.
- EDMA support on all cores, wherever applicable
  - A15, IPU uses system EDMA (via EDMA3LLD library)
  - DSP uses system EDMA or local EDMA (via EDMA3LLD library)
  - EVE uses local EDMA (via EDMA3LLD library and/or EVE SW library)
- Global timestamp to keep track of common time across all CPUs.
- Buffer allocation APIs for DDR, OCMC memory, L2 memory (DSP/EVE).
- Use-Case Auto Generation tool which generates C code for Vision SDK use-cases from config file.

1.2 Supported Links

No.	Links	TDA2xx	TDA2Px	TDA2Ex	TDA3xx
1	VIP Capture	√	√	√	√
2	Display	√	√	√	√
3	Display controller	√	√	√	√
4	IPC OUT/IN	√	√	√	√
5	Dup	√	√	√	√
6	Merge	√	√	√	√
7	Sync	√	√	√	√
8	Select	√	√	√	√
9	Null	√	√	√	√
10	Null Source	√	√	√	√
11	ISS Capture	X	√	X	√
12	ISS M2M ISP	X	√	X	√
13	ISS M2M Simcop	X	√	X	√
14	VPE	√	√	√	√
15	AVB receiver	√	√	√	X
16	MJPEG decoder	√	√	√	X
17	MJPEG encoder	√	√	√	X
18	H264 decoder	√	√	√	X
19	H264 encoder	√	√	√	X
20	Gate	√	√	√	√
1	Graphics Source	√	√	√	√
2	Ultrasonic Capture	√	X	X	X
3	Network Ctrl	√	√	√	√
4	Split	√	√	√	√
1	Alg plugin for Frame Copy	√	√	√	√
2	Alg plugin for Color to gray	√	√	√	√
3	Alg plugin for DMA Software Mosaic	√	√	√	√
4	Alg plugin for Edge detection	√	√	X	√
5	Alg plugin for Dense Optical Flow	√	X	X	√

No.	Links	TDA2xx	TDA2Px	TDA2Ex	TDA3xx
6	Alg plugin for Object detection	√	√	X	√
7	Alg plugin for Sparse optical flow	√	√	X	√
8	Alg plugin for Sub Frame Copy	√	√	X	√
9	Alg plugin for ISS AEWB	X	√	X	√
10	Alg plugin for Synthesis	√	√	√	√
11	Alg plugin for Photometric Alignment	√	√	√	√
12	Alg plugin for Geometric Alignment	√	√	√	√
13	Alg plugin for Ultrasound	√	X	X	X
14	Alg plugin Soft ISP	X	X	X	X
15	Alg plugin Census	X	X	X	X
16	Alg plugin Disparity	X	X	X	X
17	Alg plugin Stereo Post Process	X	X	X	X
18	Alg plugin Remap Merge	X	X	X	X
19	Alg Plugin Lane Detect	√	√	√	√
20	Alg Plugin CRC	X	X	X	√
21	Alg DeWarp	X	√	X	√

1.3 Features Not Supported and/or not Tested

- Capture link
  - Enabling multiple VIP ports when sub frame capture is enabled.
- VPE link
  - VPE link in DEI mode
- Algorithm link
  - Multi-channel mode NOT supported in Algorithm plugin's

For detailed list refer to
\vision_sdk\docs\FeatureSpecificUserGuides\vision_sdk_feature_list.xlsx.

2 TDA2xx Common System Parameters

2.1 System Parameters

The system parameters mentioned below are common across all configurations unless specified otherwise.

COMPONENT	PROPERTY	VALUE
SOC	SOC Name	TDA2xx
	SOC revision	ES1.0 or ES1.1 or ES2.0
EVM	EVM Name	TI TDA2xx EVM Vision Daughter card
IPU	Clock	212.8Mhz
	L1-P cache	ENABLED
	L1-D cache	ENABLED
	Code/Data Placement	DDR
DSP	Clock	600Mhz
	L1-P cache	32KB ENABLED
	L1 D cache	32KB ENABLED
	L2 P/D cache	32KB ENABLED
	Code/Data Placement	DDR
EVE	Clock	ARP32 267.5MHz VCOP 535Mhz
	L1-P cache	ENABLED
	DMEM	USED FOR IPC and ALG TASK STACK
	Code/Data Placement	DDR
A15-0	Clock	750Mhz
	P/D cache	ENABLED
	Code/Data Placement	DDR
DDR Config	Clock	532Mhz
	Bus Width	32-bit
	Number of EMIFs	1
	DDR size	512 MB

COMPONENT	PROPERTY	VALUE
Sensor	Part number	OV10635
	PCLK	74.25Mhz
	Resolution @ frame-rate	1280x720@30fps
	Data format	YUV422 interleaved
	Bus width	8-bit
	Sync Type	HS/VS discrete sync
HDMI Receiver 1 *	Part number	SII 9127
	Resolution @ frame-rate	1920x1080@60fps
	Data format	YUV422 interleaved
	Bus width	16-bit
	Sync Type	Discrete sync with AVID and VBLK control signals
HDMI Receiver 2 *	Part number	ADV 7611
	Resolution @ frame-rate	1920x1080@60fps
	Data format	YUV422 interleaved
	Bus width	16-bit
	Sync Type	Discrete sync with AVID and VBLK control signals
LCD 1 *	Part number	7-inch, WVGA LCD #703663
	DCLK	29.232Mhz
	Resolution @ frame-rate	800x480 @ 60fps
	Data format	RGB888
	Bus width	24-bit
	Sync Type	HS/VS discrete sync
LCD 2 *	Part number	10-inch, WXGA LCD #LG LP101WX2
	DCLK	74.5Mhz
	Resolution @ frame-rate	1280x800 @ 60fps
	Data format	RGB888
	Bus width	24-bit
	Sync Type	HS/VS discrete sync

COMPONENT	PROPERTY	VALUE
DSS Display	DSS pipe	VID1 VID2 VID3 GRPX Any or all of above used based on use-case
	DSS output port	DPI1 for LCD and HDMI for HDMI display type
	DSS VENC	LCD1 or LCD2 for LCD and HDMI for HDMI display type
	Inline scaling	ENABLED or DISABLED based on use-case

* NOTE Above table lists all HDMI receivers and LCDs supported. But at a time only one type of LCD can be connected. Same applies to other devices.

2.2 Code/Data Memory Usage

NOTE: Code/data memory for data structures is same for all configurations and all use-cases since a single binary is used for all configurations and all use-cases. These configurations are with respect to 512MB Memory map.

CPU	MEMORY SECTION	MEMORY SIZE RESERVED	MEMORY SIZE USED
IPU1-0	Initialized section (.text, .const)	10 MB	8.8 MB
	Uninitialized section (.bss, .heap, .stack)	11 MB	10.35 MB
IPU1-1	Initialized section (.text, .const)	2 MB	227 KB
	Uninitialized section (.bss, .heap, .stack)	9 MB	2.75 MB
IPU2	Initialized section (.text, .const)	2 MB	
	Uninitialized section (.bss, .heap, .stack)	9 MB	
DSP1	Initialized section (.text, .const)	4 MB	670 KB
	Uninitialized section (.bss, .heap, .stack, .far, .fardata)	13.5 MB	8.17 MB
DSP2	Initialized section (.text, .const)	2 MB	670 KB
	Uninitialized section (.bss, .heap, .stack)	13.5 MB	8.67 MB
EVE1	Initialized section (.text, .const)	2 MB	538 KB
	Uninitialized section (.bss, .heap, .stack)	13.5 MB	1.43 MB
EVE2	Initialized section (.text, .const)	2 MB	487 KB

	Uninitialized section (.bss, .heap, .stack)	13.5 MB	5.67 MB
EVE3	Initialized section (.text, .const)	2 MB	449.8 KB
	Uninitialized section (.bss, .heap, .stack)	13.5 MB	1.43 MB
EVE4	Initialized section (.text, .const)	2 MB	449.8 KB
	Uninitialized section (.bss, .heap, .stack)	13.5 MB	1.43 MB
A15-0	Initialized section (.text, .const) Uninitialized section (.bss, .heap, .stack)	13 MB	11 MB

2.3 App Image Size

PARAMETER	VALUE
App Image size (10 CPU images and all default supported usecase enabled)	41.6 MB

This App Image contains images for all the 10 processors and all default supported usecase enabled.

3 TDA2Px Common System Parameters

3.1 System Parameters

The system parameters mentioned below are common across all configurations unless specified otherwise.

COMPONENT	PROPERTY	VALUE
SOC	SOC Name	TDA2Px
	SOC revision	ES1.0
EVM	EVM Name	TI TDA2Px EVM Vision Daughter card
IPU	Clock	212.8Mhz
	L1-P cache	ENABLED
	L1-D cache	ENABLED
	Code/Data Placement	DDR
DSP	Clock	600Mhz
	L1-P cache	32KB ENABLED
	L1 D cache	32KB ENABLED
	L2 P/D cache	32KB ENABLED
	Code/Data Placement	DDR
EVE	Clock	ARP32 267.5MHz VCOP 535Mhz
	L1-P cache	ENABLED
	DMEM	USED FOR IPC and ALG TASK STACK
	Code/Data Placement	DDR
A15-0	Clock	750Mhz
	P/D cache	ENABLED
	Code/Data Placement	DDR
DDR Config	Clock	532Mhz
	Bus Width	32-bit
	Number of EMIFs	1
	DDR size	512 MB

COMPONENT	PROPERTY	VALUE
Sensor 1 *	Part number	OV10635
	PCLK	74.25Mhz
	Resolution @ frame-rate	1280x720@30fps
	Data format	YUV422 interleaved
	Bus width	8-bit
	Sync Type	HS/VS discrete sync
Sensor 2 *	Part number	OV10640 CSI2
	PCLK	90 MHz
	Resolution @ frame-rate	1280x720@23fps
	Data format	RAW Bayer
	Bus width	4 lanes
	Sync Type	HS/VS discrete sync
HDMI Receiver 1 *	Part number	SII 9127
	Resolution @ frame-rate	1920x1080@60fps
	Data format	YUV422 interleaved
	Bus width	16-bit
	Sync Type	Discrete sync with AVID and VBLK control signals
HDMI Receiver 2 *	Part number	ADV 7611
	Resolution @ frame-rate	1920x1080@60fps
	Data format	YUV422 interleaved
	Bus width	16-bit
	Sync Type	Discrete sync with AVID and VBLK control signals
DSS Display	DSS pipe	VID1 VID2 VID3 GRPX Any or all of above used based on use-case
	DSS output port	HDMI for HDMI display type
	DSS VENC	HDMI for HDMI display type

COMPONENT	PROPERTY	VALUE
	Inline scaling	ENABLED or DISABLED based on use-case

* NOTE Above table lists all Sensors, HDMI receivers supported. But at a time only one type of sensor can be connected. Same applies to other devices.

3.2 Code/Data Memory Usage

NOTE: Code/data memory for data structures is same for all configurations and all use-cases since a single binary is used for all configurations and all use-cases. These configurations are with respect to 512MB Memory map.

CPU	MEMORY SECTION	MEMORY SIZE RESERVED	MEMORY SIZE USED
IPU1-0	Initialized section (.text, .const)	10 MB	8.8 MB
	Uninitialized section (.bss, .heap, .stack)	15 MB	10.35 MB
IPU1-1	Initialized section (.text, .const)	2 MB	227 KB
	Uninitialized section (.bss, .heap, .stack)	9 MB	2.75 MB
IPU2	Initialized section (.text, .const)	2 MB	
	Uninitialized section (.bss, .heap, .stack)	9 MB	
DSP1	Initialized section (.text, .const)	4 MB	670 KB
	Uninitialized section (.bss, .heap, .stack, .far, .fardata)	13.5 MB	8.17 MB
DSP2	Initialized section (.text, .const)	2 MB	670 KB
	Uninitialized section (.bss, .heap, .stack)	13.5 MB	8.67 MB
EVE1	Initialized section (.text, .const)	2 MB	538 KB
	Uninitialized section (.bss, .heap, .stack)	13.5 MB	1.43 MB
EVE2	Initialized section (.text, .const)	2 MB	487 KB
	Uninitialized section (.bss, .heap, .stack)	13.5 MB	5.67 MB
A15-0	Initialized section (.text, .const) Uninitialized section (.bss, .heap, .stack)	13 MB	11 MB

3.3 App Image Size

PARAMETER	VALUE
App Image size (8 CPU images and all default supported usecase enabled)	27.7 MB

This App Image contains images for all the 8 processors and all default supported usecase enabled.

4 TDA2Ex- Common System Parameters

4.1 System Parameters

The system parameters mentioned below are common across all configurations unless specified otherwise.

COMPONENT	PROPERTY	VALUE
SOC	SOC Name	TDA2Ex
	SOC revision	ES1.0 or ES2.0
EVM	EVM Name	TI TDA2Ex EVM Vision Daughter card
IPU	Clock	212.8MHz
	L1-P cache	ENABLED
	L1-D cache	ENABLED
	Code/Data Placement	DDR
DSP	Clock	600MHz
	L1-P cache	32KB ENABLED
	L1 D cache	32KB ENABLED
	L2 P/D cache	32KB ENABLED
	Code/Data Placement	DDR
A15-0	Clock	800MHz
	P/D cache	ENABLED
	Code/Data Placement	DDR
DDR Config	Clock	666Mhz
	Bus Width	32-bit
	Number of EMIFs	1
	DDR size	1 GB
Sensor	Part number	OV10635
	PCLK	74.25Mhz
	Resolution @ frame-rate	1280x720@30fps
	Data format	YUV422 interleaved
	Bus width	8-bit
	Sync Type	HS/VS discrete sync

COMPONENT	PROPERTY	VALUE
HDMI Receiver 1 *	Part number	SII 9127
	Resolution @ frame-rate	1920x1080@60fps
	Data format	YUV422 interleaved
	Bus width	16-bit
	Sync Type	Discrete sync with AVID and VBLK control signals
HDMI Receiver 2 *	Part number	ADV 7611
	Resolution @ frame-rate	1920x1080@60fps
	Data format	YUV422 interleaved
	Bus width	16-bit
	Sync Type	Discrete sync with AVID and VBLK control signals
LCD 1 *	Part number	10-inch, WXGA LCD #LG LP101WX2
	DCLK	74.5Mhz
	Resolution @ frame-rate	1280x800 @ 60fps
	Data format	RGB888
	Bus width	24-bit
	Sync Type	HS/VS discrete sync
DSS Display	DSS pipe	VID1 VID2 VID3 GRPX Any or all of above used based on use-case
	DSS output port	DPI1 for LCD and HDMI for HDMI display type
	DSS VENC	LCD1 or LCD2 for LCD and HDMI for HDMI display type
	Inline scaling	ENABLED or DISABLED based on use-case

* NOTE Above table lists all HDMI receivers and LCDs supported. But at a time only one type of LCD can be connected. Same applies to other devices.

4.2 Code/Data Memory Usage

NOTE: Code/data memory for data structures is same for all configurations and all use-cases since a single binary is used for all configurations and all use-cases. These configurations are with respect to 512MB Memory map.

CPU	MEMORY SECTION	MEMORY SIZE RESERVED	MEMORY SIZE USED
IPU1-0	Initialized section (.text, .const)	10 MB	8.6 MB
	Uninitialized section (.bss, .heap, .stack)	12 MB	8.7MB
IPU1-1	Initialized section (.text, .const)	2 MB	226 KB
	Uninitialized section (.bss, .heap, .stack)	10 MB	2.76 MB
IPU2	Initialized section (.text, .const)	2 MB	
	Uninitialized section (.bss, .heap, .stack)	10 MB	
DSP1	Initialized section (.text, .const)	2 MB	669 KB
	Uninitialized section (.bss, .heap, .stack, .far, .fardata)	15 MB	8.17 MB
A15-0	Initialized section (.text, .const) Uninitialized section (.bss, .heap, .stack)	13 MB	11 MB

4.3 App Image Size

PARAMETER	VALUE
App Image size (5 CPU images and all default supported usecase enabled)	23.3 MB

This App Image contains images for all the 5 processors and all default supported usecase enabled.

5 TDA3xx Common System Parameters

5.1 System Parameters

The system parameters mentioned below are common across all configurations unless specified otherwise.

COMPONENT	PROPERTY	VALUE
SOC	SOC Name	TDA3xx
	SOC revision	1.0 or 2.0
EVM	EVM Name	TI TDA3xx EVM
IPU	Clock	212.8Mhz
	L1-P cache	ENABLED
	L1-D cache	ENABLED
	Code/Data Placement	DDR
DSP	Clock	500Mhz
	L1-P cache	32KB ENABLED
	L1 D cache	32KB ENABLED
	L2 P/D cache	32KB ENABLED
	Code/Data Placement	DDR
EVE	Clock	ARP32 250MHz VCOP 500Mhz
	L1-P cache	ENABLED
	DMEM	USED FOR IPC and ALG TASK STACK
	Code/Data Placement	DDR
DDR Config	Clock	532Mhz
	Bus Width	32-bit
	Number of EMIFs	1
	DDR size	512 MB
Sensor 1 *	Part number	OV10635
	PCLK	74.25Mhz
	Resolution @ frame-rate	1280x720@30fps
	Data format	YUV422 interleaved
	Bus width	8-bit

COMPONENT	PROPERTY	VALUE
	Sync Type	HS/VS discrete sync
Sensor 2 *	Part number	OV10640 CSI2
	PCLK	90 MHz
	Resolution @ frame-rate	1280x720@23fps
	Data format	RAW Bayer
	Bus width	4 lanes
	Sync Type	HS/VS discrete sync
Sensor 3 *	Part number	AR0132
	PCLK	74.25 MHz
	Resolution @ frame-rate	1280x720@60fps
	Data format	RAW Bayer
	Bus width	12-bit
	Sync Type	HS/VS discrete sync
Sensor 4 *	Part number	AR0140
	PCLK	74MHz
	Resolution @ frame-rate	1280x800 @ 30fps
	Data format	Bayer
	Bus width	12bit
	Sync Type	Discrete sync
HDMI Receiver *	Part number	ADV 7611
	Resolution @ frame-rate	1920x1080@60fps
	Data format	YUV422 interleaved
	Bus width	16-bit
	Sync Type	Discrete sync with AVID and VBLK control signals
LCD 1 *	Part number	10-inch, WXGA LCD #LG LP101WX2
	DCLK	74.5Mhz
	Resolution @ frame-rate	1280x800 @ 60fps
	Data format	RGB888
	Bus width	24-bit
	Sync Type	HS/VS discrete sync

COMPONENT	PROPERTY	VALUE
HDMI TX 1 *	Part number	SII 9022A
	DCLK	148.5Mhz
	Resolution @ frame-rate	1920x1080 @ 60fps
	Data format	RGB888
	Bus width	24-bit
	Sync Type	HS/VS discrete sync
SD Display 1	Part number	On-Chip SDDAC
	DCLK	27Mhz
	Resolution @ frame-rate	NTSC: 720x240 @ 60 fps (Interlaced) PAL: 720x288 @ 50 fps (Interlaced)
DSS Display	DSS pipe	VID1 VID2 GRPX Any or all of above used based on use-case
	DSS output port	DPI1 for LCD, HDMI (Off-Chip HDMI TX)
	DSS VENC	LCD1 for LCD and HDMI (Off-Chip HDMI TX) SDDAC for NTSC/PAL Display
	Inline scaling	ENABLED or DISABLED based on use-case

* NOTE Above table lists all Sensors, HDMI receivers and LCDs supported. But at a time only one type of sensor can be connected. Same applies to other devices.

5.2 Code/Data Memory Usage

NOTE: Code/data memory for data structures is same for all configurations and all use-cases since a single binary is used for all configurations and all use-cases. These configurations are with respect to 512MB Memory map.

CPU	MEMORY SECTION	MEMORY SIZE RESERVED	MEMORY SIZE USED
IPU1-0	Initialized section (.text, .const)	10 MB	7.5 MB
	Uninitialized section (.bss, .heap, .stack)	13 MB	11.8 MB

IPU1-1	Initialized section (.text, .const)	2 MB	219 KB
	Uninitialized section (.bss, .heap, .stack)	10 MB	2.80 MB
DSP1	Initialized section (.text, .const)	2 MB	631KB
	Uninitialized section (.bss, .heap, .stack)	14 MB	7.25 MB
DSP2	Initialized section (.text, .const)	2 MB	631KB
	Uninitialized section (.bss, .heap, .stack)	14 MB	7.75 MB
EVE1	Initialized section (.text, .const)	2 MB	400 KB
	Uninitialized section (.bss, .heap, .stack)	13.5 MB	1.39 MB

5.3 App Image Size

PARAMETER	VALUE
App Image size (5 CPU images and all default supported usecase enabled)	26.1 MB

This App Image contains images for all the 5 processors and all default supported usecase enabled.

6 Single Channel Capture Use Case

6.1 Overview

This use case consists of continuous capture and display with optional frame copy using DSP/EVE/A15 in between or edge detect algorithm using EVE.

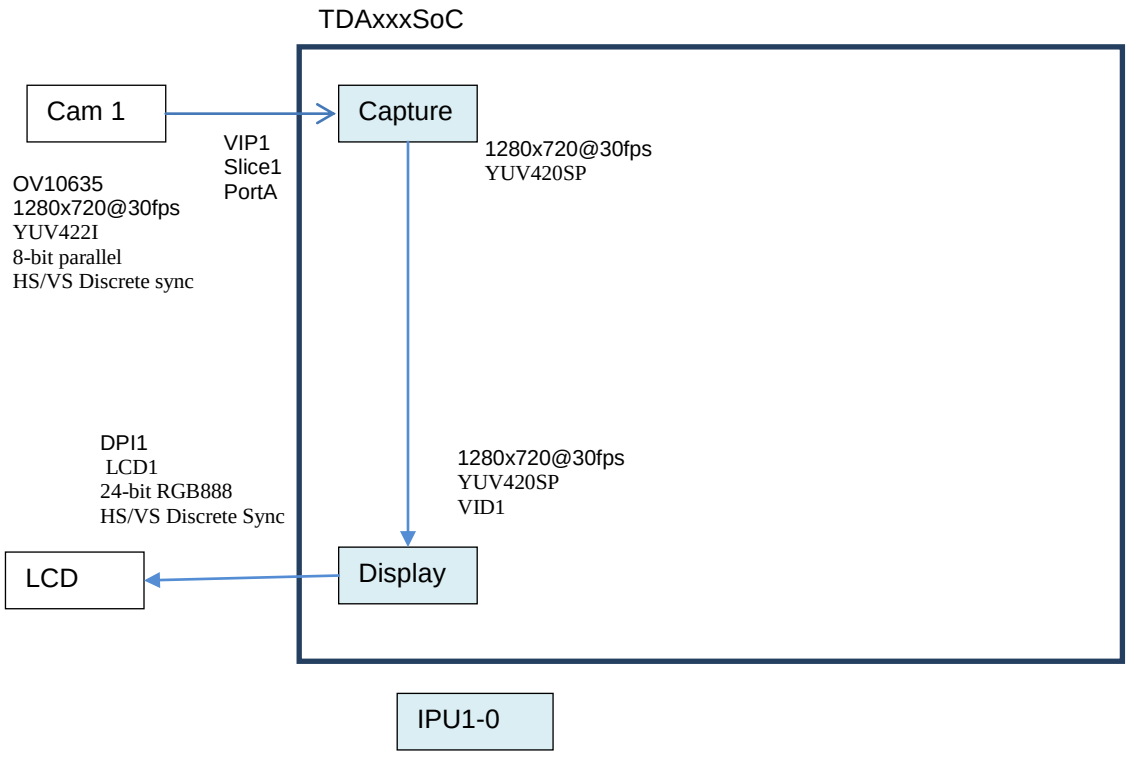
Frame copy/Edge Detect is used to show how an algorithm can be integrated in a capture to display data flow.

Capture can be done at 720p@30fps (OV Sensor)or 1080p@60fps (HDMI capture)via the VIP1 Slice1 PortA. Display can be on LCD via DPI1 output port or on HDMI display via HDMI output port. If required, a scalar is enabled as part of the capture path to match display resolution. The output interface runs at 60fps. In case incoming frames to display are at 30fps (when using OV Sensors), then the Display driver will repeat frames.

6.2 DataFlow

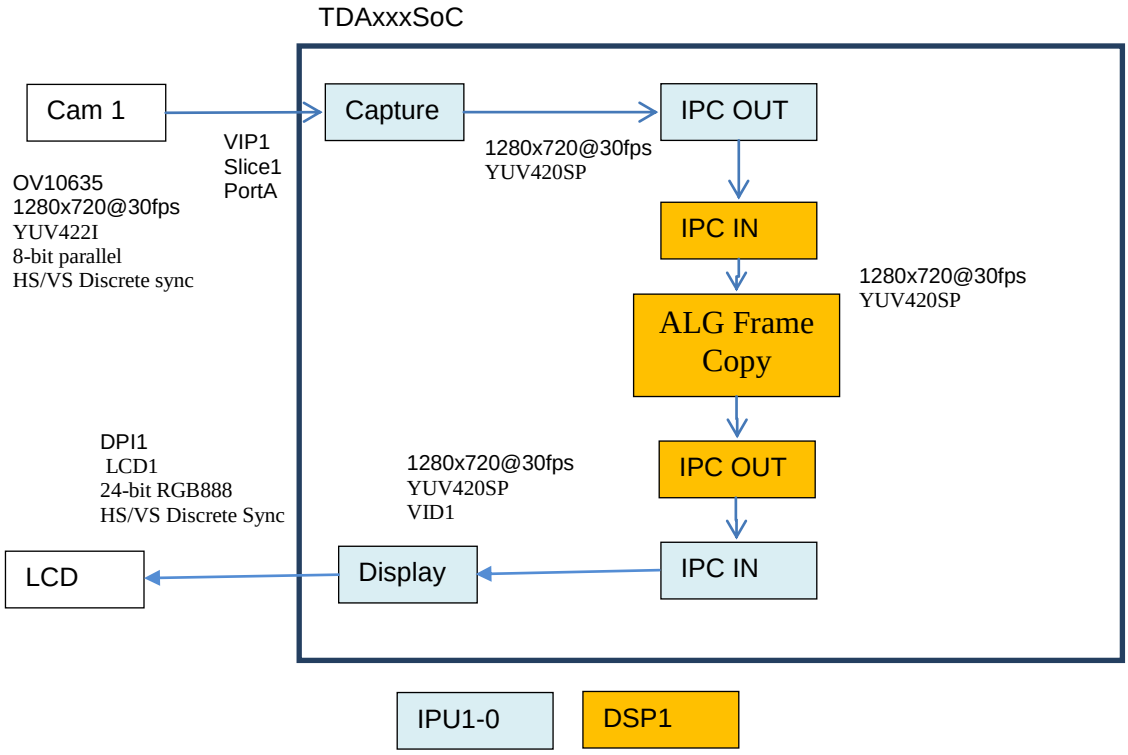
6.2.1 Configuration 1: Capture to Display on IPU 1-0

This configuration is useful for board checkout. Since only IPU1-0 CPU is required to run this use-case so it is easy to build and load and run. The data flow below shows a 720p30 capture with display on LCD. Alternately HDMI capture and HDMI display are also supported.



6.2.2 Configuration 2: Capture to Display via Frame Copy Algorithm DSP1

Frame copy algorithm on DSP uses DSP local EDMA for frame copy. EDMA3LLD library is used to access EDMA. The data flow below shows a 720p30 capture with display on LCD. Alternately HDMI capture and HDMI display are also supported.



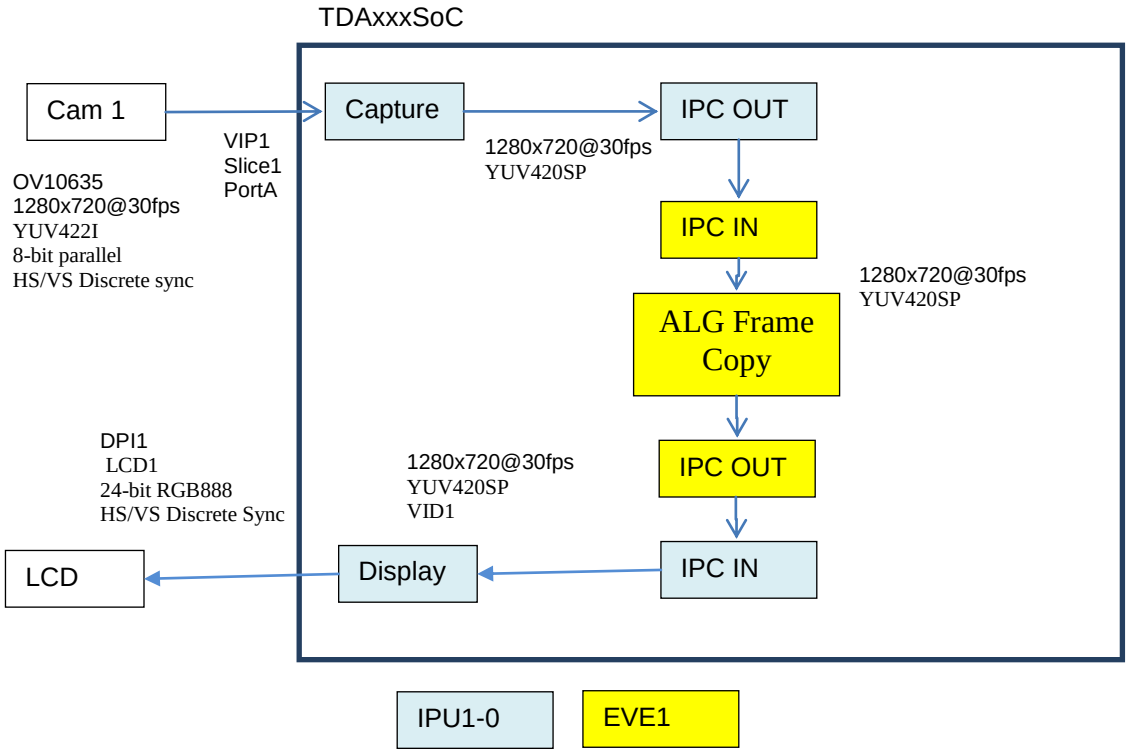
6.2.3 Configuration 3: Capture to Display via Frame Copy Algorithm EVE1

This is same as configuration 2 except EVE1 is used for frame copy instead of DSP1.

EVE1 uses its local DMA for frame copy. EVE SW library is used to do the EDMA.

EDMA3LLD is not used since normally algorithms on EVE will use the EVE SW library for EDMA.

The data flow below shows a 720p30 capture with display on LCD. Alternately HDMI capture and HDMI display are also supported.



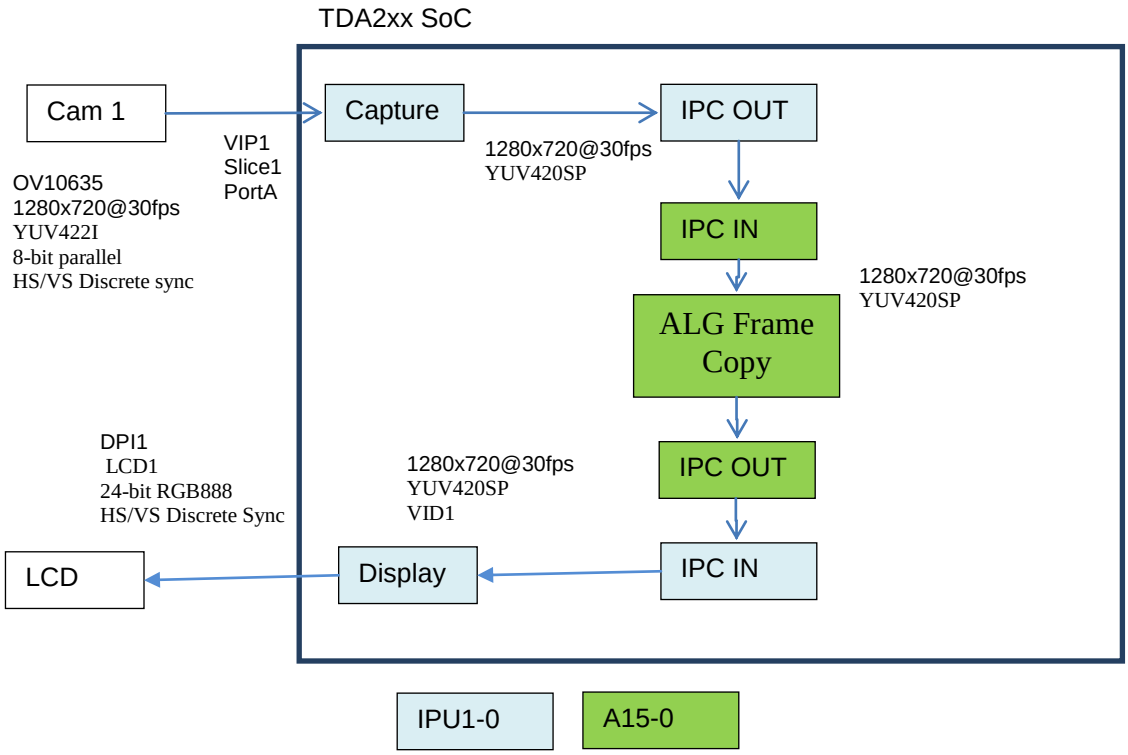
6.2.4 Configuration 4: Capture to Display via via Frame Copy Algorithm A15 (TDA2xx Only)

This is same as configuration 2 except A15 is used for frame copy instead of DSP1.

A15 uses CPU copy via cache for frame copy. Cache invalidates and write back are done as required in the process.

EDMA is not used since normally algorithms on A15 prefer to use CPU access via cache. System EDMA APIs via EDMA3LLD are however available for access via A15.

The data flow below shows a 720p30 capture with display on LCD. Alternately HDMI capture and HDMI display are also supported.



6.3 System Parameters (TDA2xx)

Refer to section 2.1 for common system parameters.

The benchmarks in this section are computed for 720p30fps capture and HDMI display (1080p60) scenario.

6.4 CPU Loading and Task Info (TDA2xx)

6.4.1 Total CPU Load

NOTE: DSP and EVE use frame copy EDMA in polled mode, since normally in between DMA, algorithm computation is done.

NOTE: A15 uses frame copy in CPU mode (via cache) hence its CPU load is higher than DSP/EVE.

CPU	LOAD TYPE	CPU LOAD (CONFIGI1 IPU ONLY)	CPU LOAD (CONFIG2 DSP FC ALG)	CPU LOAD (CONFIG3 EVE FC ALG)	CPU LOAD (CONFIG4 A15 FC ALG)
IPU1-0	HWI	1.4%	1.7%	1.8%	1.8%
	SWI	0.5%	0.6%	0.5%	0.6%
	Total	**10.1%**	**13.2%**	**10.8%**	**13.0%**
DSP1	HWI	NA	0.3%	NA	
	SWI		0.1%		
	Total		**4.3%**		
EVE1	HWI	NA		0.9%	NA
	SWI			0.2%	
	Total			**6.9%**	
A15-0	HWI	NA			0.1%
	SWI				0.1%
	Total				**6.1%**

6.4.2 Task Level Information and Task Level CPU Load

CPU	TASK NAME	TASK DESCRIPTION	CPU LOAD (CONFIG1 IPU ONLY)	CPU LOAD (CONFIG 2 DSP FC ALG)	CPU LOAD (CONFIG 3 EVE FC ALG)	CPU LOAD (CONFIG 4 A15 FC ALG)
IPU 1-0	Stat Collector	Statistics collector	3.3%	3.3%	2.8%	3.3%
	Capture	Capture frames via VIP port	0.2%	0.2%	0.2%	0.2%
	Display	Display frames via DSS	0.5%	0.6%	0.5%	0.6%
	UNKNOWN	This is unaccounted CPU load after subtracting the individual task load from total CPU Load	1.3%	1.6%	1.6%	1.4%
	IPC OUT	To send frame to another processor	NA	0.6%	0.6%	0.5%

CPU	TASK NAME	TASK DESCRIPTION	CPU LOAD (CONFIG1 IPU ONLY)	CPU LOAD (CONFIG 2 DSP FC ALG)	CPU LOAD (CONFIG 3 EVE FC ALG)	CPU LOAD (CONFIG 4 A15 FC ALG)
	IPC IN	To receive frames from another processor		0.3%	0.3%	0.3%
DSP 1	*IPC + ALG Frame Copy	Frame copy + IPC	NA	3.7%	NA	
	UNKNOWN	This is unaccounted CPU load after subtracting the individual task load from total CPU Load		0.2%		
EVE 1	*IPC + ALG Frame Copy	Framecopy + IPC	NA		5.6%	NA
	UNKNOWN	This is unaccounted CPU load after subtracting the individual task load from total CPU Load			0.2%	
A15-0	*IPC + ALG Frame Copy	Copy frames from input buffer to output buffer Using CPU copy via cache	NA			
	UNKNOWN	This is unaccounted CPU load after subtracting the individual task load from total CPU Load				5.9%

*NOTE: On DSP and similarly on EVE all links run in a single thread.

NOTE: CPU load of 0.0% means the CPU load was so low it could not be measured with sufficient granularity.

NOTE: There could be minor variations of +/-0.1% CPU load in different runs of the same use-case

NOTE: Graphics load is not accounted for in these measurements

NOTE: Other than above tasks few additional tasks as listed below are active in each processor

- Message Q task: This task is used to listen to control messages sent by any other core. Normally at run-time very few control messages are sent hence this task does not appear in the task load print log
- Processor link task: This task is used to send generic non-link specific messages to another CPU. Normally at run-time very few messages are sent to this task hence this task does not appear in the task load print log
- Remote log client task (on IPU1-0 only): This task looks at the shared remote log buffer and outputs any strings to UART terminal. Normally during run-time prints are not done hence this task does not appear in the task load log

6.5 System Performance (TDA2xx)

COMPONENT	PARAMETER	CONFIG1 IPU ONLY	CONFIG2 DSP FC ALG	CONFIG3 EVE FC ALG	CONFIG4 A15 FC ALG
Capture	Output FPS	30fps	30fps	30fps	30fps
ALG Frame Copy (DSP / A15 / EVE)	Output FPS	NA	30fps	30fps	30fps
	Avg copy time per frame		1.10ms	1.12ms	1.45ms
Display	Input FPS	30fps	30fps	30fps	30fps
	VENC FPS	60fps	60fps	60fps	60fps

NOTE: FPS numbers are rounded off to nearest integer
NOTE: The above benchmarks are computed for 720p30 fps capture and HDMI display (1080p60)

6.6 System Memory Usage (TDA2xx)

6.6.1 Code/Data Memory Usage

Refer section 2.2 for common Code/Data Memory usage.

6.6.2 Heap Memory Usage

CPU	MEMORY SECTION	MEMORY SIZE RESERVED	MEMORY SIZE USED (CONFIG1 IPU ONLY)	MEMORY SIZE USED (CONFIG2 DSP FC ALG)	MEMORY SIZE USED (CONFIG3 EVE FC ALG)	MEMORY SIZE USED (CONFIG4 A15 FC ALG)
IPU1-0	Local Heap	256 KB	16 KB	16 KB	16 KB	16 KB
	HDVPSS Descriptor Mem	1MB	114 KB	114 KB	114 KB	114 KB
DSP1	L2	221 KB	NA	0 KB	NA	
	Local Heap	512 KB		24 KB		
EVE1	L2	22 KB	NA		0 KB	NA
	Local Heap	256 KB			24 KB	
A15	Local Heap	6144 KB	NA			62 KB
Shared Memory	SR0 DDR	128 KB	36 KB	36 KB	36 KB	36 KB
	SR1 Frame Buffer	350 MB	7 MB	11 MB	11 MB	11 MB
	SR OCMC	0 KB	0 KB	0 KB	0 KB	0 KB
	Remote Log Buffer	160 KB	158 KB	158 KB	158 KB	0KB

NOTE:

- SR1 Frame Buffer now static memory allocation .map file show all memory used but in actual we don't know how much memory used. This is applicable all usecase.
- In case ECC_FFI_INCLUDE defined, three additional memory sections are added "SR1_BUFF_ECC_ASIL", "SR1_BUFF_ECC_QM" and "SR1_BUFF_NON_ECC_ASIL" with sizes 1MB, 40MB and 1MB respectively. These sections are used only by "safeframecopy" plugin and is not documented in the above table.

6.6.3 Heap Memory Usage

PARAMETER	BANDWIDTH	(CONFIGI1 IPU ONLY)	(CONFIG2 DSP FC ALG)	(CONFIG3 EVE FC ALG)	(CONFIG4 A15 FC ALG)
EMIF Read Only	Avg	154 MB/s	199 MB/s	202 MB/s	155 MB/s
	Peak	281 MB/s	503 MB/s	486 MB/s	320 MB/s
EMIF Write Only	Avg	58 MB/s	99 MB/s	101 MB/s	58 MB/s
	Peak	120 MB/s	368 MB/s	360 MB/s	126 MB/s
EMIF Read + Write	Avg	213 MB/s	298 MB/s	303 MB/s	214 MB/s
	Peak	401 MB/s	872 MB/s	844 MB/s	446 MB/s

6.7 Other Benchmarks (TDA2xx)

6.7.1 Processing Latency

		LATENCY (CONFIG1 IPU ONLY)	LATENCY (CONFIG2 DSP FC ALG)	LATENCY (CONFIG3 EVE FC ALG)	LATENCY (CONFIG4 A15 FC ALG)
Capture to Display Latency	Avg	0.12ms	1.74ms	2.35ms	2.03ms
	Min	0.09ms	1.43ms	2.01ms	1.89ms
	Max	0.21ms	1.89ms	2.92ms	2.47ms

NOTE:

- This latency is as measured inside the system by software.
- There will an additional 1/(capture rate) added on top of this from sensor/receiver itself.
- There will an additional 1/(display rate) added on top of this for the frame to actually get displayed on the screen.
- Thus e.g. in a scenario of display at 60fps and capture at 30fps - 16.67ms + 33.33ms needs to be added to latency figures in above table to get true capture to display latency

6.7.2 Boot Time

PARAMETER	VALUE
SBL to App main() (QSPI Boot) The boot time will change based on the mode of boot – SD, NOR flash or QSPI.	1.599s
main() to Use-case create	0.340s
Use-case create start to Live preview on display (max value from all 4 configurations)	0.065 s
Total Boot time	**2.004s**

QSPI Boot time measurement done with TDA2xx ES2.0 samples

GUI and Sensor initialization time not accounted for.

7 Subframe copy Use case

7.1 Overview

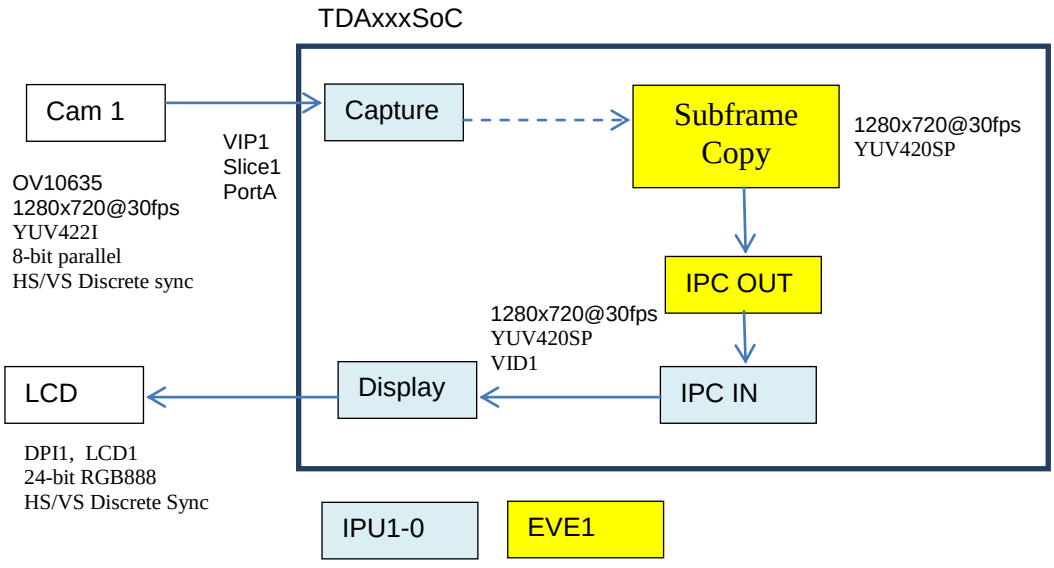
This configuration is used to demonstrate a low-latency path which utilizes the subframe capture feature.

7.2 DataFlow

7.2.1 Subframe copy example

The Capture can be either OV10635 Sensor @720p30 or HDMI @1080p60 via the VIP1 Slice1 PortA. Scalar is required to be enabled for this feature.The Capture link enables subframe-capture mode and configures the VIP but does not process any frame data. Hence no IPC link is required between the capture link on IPU1_0 and Subframe copy link on EVE1. The Subframe copy link registers interrupts with VIP at subframe and frame boundaries. Whenever a sub-frame is received an EDMA transfer for the data is initiated onto display buffer. Subframe copy algorithm on EVE uses local EDMA for subframe copy. EDMA3LLD library is used to access EDMA. The display link processes data at frame boundaries. Display can be on LCD via DPI1 output port or on HDMI display via HDMI output port.The output interface runs at 60fps. In case incoming frames to display are at 30fps (when using OV Sensors), then the Display driver will repeat frames.

The data flow below shows OV Sensor capture and LCD display. Alternately HDMI capture and HDMI display are also supported.



7.3 System Parameters (TDA2xx)

Refer to section 2.1 for common system parameters.

The benchmarks in this section are computed for OV10635capture and HDMI display (1080p60) scenario.

7.4 CPU Loading and Task Info (TDA2xx)

7.4.1 Total CPU Load

CPU	LOAD TYPE	CPU LOAD
IPU1_0	**HWI**	1.4%
	SWI	0.5%
	Total	**9.0%**
EVE1	**HWI**	2.9%
	SWI	0.2%
	Total	**8.7%**

7.4.2 Task Level Information and Task Level CPU Load

CPU	TASK NAME	TASK DESCRIPTION	CPU LOAD
IPU1-0	Stat Collector	Statistics collector	2.9%
	Capture	Capture frames from sensor via VIP port	0.0 %
	Display	Display via DSS	0.6%
	UNKNOWN	This is unaccounted CPU load after subtracting the individual task load from total CPU Load	1.5%
	IPC IN	To receive frames from another processor	0.3%
*EVE1	IPC +ALG Subframe copy	Algsubframe copy + IPC	5.4%
	UNKNOWN	This is unaccounted CPU load after subtracting the individual task load from total CPU Load	0.2%

*NOTE: On EVE all links run in a single thread.

NOTE: CPU load of 0.0% means the CPU load was so low it could not be measured with sufficient granularity in load calculations

NOTE: There could be minor variations of +/-0.1% CPU load in different runs of the same use-case

NOTE: Graphics load is not accounted for in these measurements

NOTE: Other than above tasks few additional tasks as listed below are active in each processor

- Message Q task: This task is used to listen to control messages sent by any other core. Normally at run-time very few control messages are sent hence this task does not appear in the task load print log
- Processor link task: This task is used to send generic non-link specific messages to another CPU. Normally at run-time very few messages are sent to this task hence this task does not appear in the task load print log
- Remote log client task (on IPU1-0 only): This task looks at the shared remote log buffer and outputs any strings to UART terminal. Normally during run-time prints are not done hence this task does not appear in the task load log

7.5 System Performance (TDA2xx)

COMPONENT	PARAMETER	
ALG-SubframeCopy (EVE1)	Input fps	30fps
	Output fps	30fps
Display	Input fps	30fps
	VENC fps	60fps

NOTE: The ALG subframe copy link processes ISRs from VIP for subframe and frame complete events. When the alg plugin link is in running state no other command except data command is processed, to ensure the low latency path functions effectively. Hence the stats for this link are not queries/printed on UART. The figures mentioned above have been interpreted from other logs and performance of IPC and Display links.
NOTE: FPS numbers are rounded off to nearest integer

7.6 System Memory Usage (TDA2xx)

7.6.1 Code/Data Memory Usage

Refer section 2.2 for common Code/Data Memory usage

7.6.2 Heap Memory Usage

CPU	MEMORY SECTION	MEMORY SIZE RESERVED	MEMORY SIZE USED
IPU1-0	Local Heap	256 KB	16 KB
	HDVPSS Descriptor Mem	1MB	114 KB
EVE1	L2	24 KB	0 KB
	Local Heap	256 KB	14 KB
Shared Memory	SR0	128 KB	36 KB
	Frame Buffer (SR1)	350MB	6 MB
	SR2 OCMC	512 KB	0 KB
	Remote Log Buffer	160 KB	158 KB

Note: Sub frames are allocated from OCMC RAM1 - 512KB

7.6.3 DDR Bandwidth

PARAMETER	BANDWIDTH	
EMIF Read Only	Avg	175 MB/s
	Peak	319 MB/s
EMIF Write Only	Avg	71 MB/s
	Peak	141 MB/s
EMIF Read + Write	Avg	246 MB/s
	Peak	460 MB/s

7.7 Other Benchmarks (TDA2xx)

7.7.1 Processing Latency

		LATENCY
Capture to Display Latency (Display VID 1)	Avg	0.65ms
	Min	0.61ms
	Max	0.79ms

NOTE:

- This latency is as measured inside the system by software.
- There will an additional 1/(capture rate) added on top of this from sensor/receiver itself.
- There will an additional 1/(display rate) added on top of this for the frame to actually get displayed on the screen.
- Thus e.g. in a scenario of display at 60fps and capture at 30fps - 16.67ms + 33.33ms needs to be added to latency figures in above table to get true capture to display latency

7.7.2 Boot Time

PARAMETER	DURATION
SBL to App main() (QSPI Boot) The boot time will change based on the mode of boot – SD, NOR flash or QSPI.	1.599s
main() to Use-case create	0.340s
Use-case create start to Live preview on display	0.050 s
Total Boot time	**1.989s**

QSPI Boot time measurement done with TDA2xx ES2.0 samples

GUI and Sensor initialization time not accounted for.

8 Dense Optical Flow Usecase

8.1 Overview

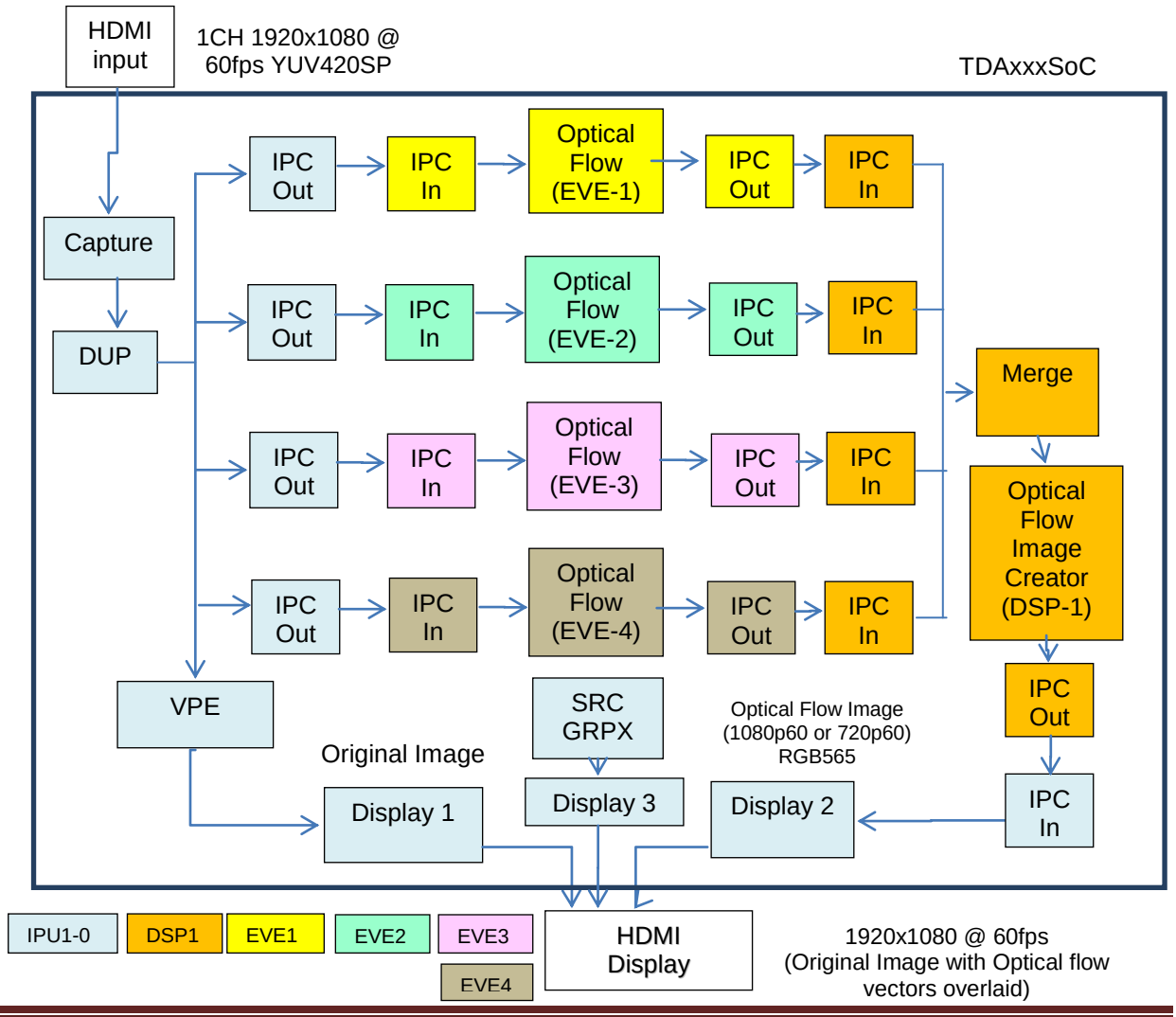
This configuration is used to demonstrate the capability of EVE. The display type is restricted to HDMI alone.

8.2 DataFlow

8.2.1 Dense Optical Flow example

The Capture can be either OV10635 Sensor @720p30 or HDMI @1080p60. The captured buffer is duplicated by DUP link running on IPU1-0 and sent to all 4 EVEs. A Dense optical flow algorithm runs on the EVEs. An algorithm setting is available by which one can choose to run a 1 pyramid (1080p60) or 2 pyramid (720p60) mode. All 4 EVEs are used in this use-case for frame processing. Each EVE processes 1 out of 4 frames. The output from the 4 EVEs is merged on DSP1 and post an Optical Flow Image creator sent to HDMI display. The original image after scaling using VPE is also displayed alongwith some overlaid graphics.The data flow below shows an HDMI capture. Alternately OV Sensor capture is also supported. This configuration supports ONLY HDMI display.

NOTE: VPE, EVE2, EVE3, EVE4 only valid in TDA2xx



8.3 System Parameters (TDA2xx)

Refer to section 2.1 for common system parameters.

The benchmarks in this section are computed for OV10635capture and HDMI display (1080p60) scenario.

8.4 CPU Loading and Task Info (TDA2xx)

8.4.1 Total CPU Load

CPU	LOAD TYPE	CPU LOAD (CONFIG - ALG 1 PYRAMID)	CPU LOAD (CONFIG - ALG 2 PYRAMID)
IPU1_0	**HWI**	2.7%	2.9%
	SWI	0.8%	0.9%
	Total	**15.8**%	**16.1**%
DSP1	**HWI**	0.3%	0.3%
	SWI	0.1%	0.1%
	Total	**14.3%**	**14.5%**
EVE1	**HWI**	0.7%	0.7%
	SWI	0.2%	0.2%
	Total	**17.5%**	**28.2%**
EVE2	**HWI**	0.7%	0.7%
	SWI	0.2%	0.2%
	Total	**17.5%**	**28.1%**
EVE3	**HWI**	0.7%	0.7%
	SWI	0.2%	0.2%
	Total	**18.6%**	**28.3%**
EVE4	**HWI**	0.7%	0.7%
	SWI	0.2%	0.2%
	Total	**18.5%**	**28.2%**

8.4.2 Task Level Information and Task Level CPU Load

CPU	TASK NAME	TASK DESCRIPTION	CPU LOAD (CONFIG ALG 1 PYRAMID)	CPU LOAD (CONFIG ALG 2 PYRAMID)
IPU1-0	Stat Collector	Statistics collector	3.6%	3.6%
	Capture	Capture frames from sensor via VIP port	0.2%	0.2%
	Display1	Display scaled frames via DSS	0.6%	0.6%
	Display2	Display DOF frame via DSS	0.5%	0.5%
	DUP	Duplicate frame to send to display without scaling as well as to VPE to scale	0.3%	0.4%
	VPE	Frame scaling	1.2%	1.2%

CPU	TASK NAME	TASK DESCRIPTION	CPU LOAD (CONFIG ALG 1 PYRAMID)	CPU LOAD (CONFIG ALG 2 PYRAMID)
	UNKNOWN	This is unaccounted CPU load after subtracting the individual task load from total CPU Load	1.9%	1.9%
	IPC OUT 0	To send frame to another processor	0.6%	0.6%
	IPC OUT 1	To send frame to another processor	0.4%	0.5%
	IPC OUT 2	To send frame to another processor	0.4%	0.5%
	IPC OUT 3	To send frame to another processor	0.4%	0.5%
	IPC IN	To receive frames from another processor	0.3%	0.3%
DSP1	IPC + ALGVector to Image	To receive frames from another processor	13.8%	13.9%
	UNKNOWN	This is unaccounted CPU load after subtracting the individual task load from total CPU Load	0.1%	0.2%
EVE1	IPC + Optical Flow	IPC Load + Dense Optical Flow Algorithm	16.4%	27.1%
	UNKNOWN	This is unaccounted CPU load after subtracting the individual task load from total CPU Load	0.2%	0.2%
EVE2	IPC + Optical Flow	IPC Load + Dense Optical Flow Algorithm	16.4%	27.0%
	UNKNOWN	This is unaccounted CPU load after subtracting the individual task load from total CPU Load	0.2%	0.2%
EVE3	IPC + Optical Flow	IPC Load + Dense Optical Flow Algorithm	17.4%	27.1%
	UNKNOWN	This is unaccounted CPU load after subtracting the individual task load from total CPU Load	0.3%	0.3%
EVE4	IPC + Optical Flow	IPC Load + Dense Optical Flow Algorithm	16.4%	27.0%
	UNKNOWN	This is unaccounted CPU load after subtracting the individual task load from total CPU Load	0.2%	0.3%

NOTE: On DSP and similarly on EVE all links run in a single thread.

NOTE: CPU load of 0.0% means the CPU load was so low it could not be measured with sufficient granularity in load calculations

NOTE: There could be minor variations of +/-0.1% CPU load in different runs of the same use-case

NOTE: Graphics load is not accounted for in these measurements

NOTE: Other than above tasks few additional tasks as listed below are active in each processor

- Message Q task: This task is used to listen to control messages sent by any other core. Normally at run-time very few control messages are sent hence this task does not appear in the task load print log
- Processor link task: This task is used to send generic non-link specific messages to another CPU. Normally at run-time very few messages are sent to this task hence this task does not appear in the task load print log
- Remote log client task (on IPU1-0 only): This task looks at the shared remote log buffer and outputs any strings to UART terminal. Normally during run-time prints are not done hence this task does not appear in the task load log

8.5 System Performance (TDA2xx)

COMPONENT	PARAMETER	(CONFIG ALG 1 PYRAMID)	(CONFIG ALG 2 PYRAMID)
Capture	Output FPS	30fps	30fps
ALG DOF (EVE)	Output FPS	~7.5 fps per EVE	~7.5 fps per EVE
	Avg time per frame	20.4ms	34.3ms
ALG Vector to Image (DSP1)	Output FPS	30fps	30fps
Display (DOF image)	Input FPS	30fps	30fps
	VENC FPS	60fps	60fps

NOTE: FPS numbers are rounded off to nearest integer
NOTE: The figures are for HDMI capture scenario.

8.6 System Memory Usage (TDA2xx)

8.6.1 Code/Data Memory Usage

Refer section 2.2 for common Code/Data Memory usage

8.6.2 Heap Memory Usage

CPU	MEMORY SECTION	MEMORY SIZE RESERVED	MEMORY SIZE USED (CONFIG ALG PYRAMID 1)	MEMORY SIZE USED (CONFIG ALG PYRAMID 2)
IPU1-0	Local Heap	256 KB	16 KB	16 KB
	HDVPSS Descriptor Mem	1MB	114 KB	114 KB
DSP1	L2	221 KB	94 KB	45 KB
	Local Heap	512 KB	12 KB	12 KB
EVE1	L2	24 KB	3 KB	3 KB
	Local Heap	256 KB	12 KB	12 KB
EVE2	L2	24 KB	3 KB	3 KB
	Local Heap	256 KB	12 KB	12 KB
EVE3	L2	24 KB	3 KB	3 KB
	Local Heap	256 KB	12 KB	12 KB
EVE4	L2	24 KB	3 KB	3 KB
	Local Heap	256 KB	12 KB	12 KB
Shared Memory	SR0	128 KB	36 KB	36 KB
	Frame Buffer (SR1)	350 MB	50 MB	50 MB
	SR2 OCMC	0KB	0KB	0KB
	Remote Log Buffer	160 KB	158 KB	158 KB

8.6.3 DDR Bandwidth

PARAMETER	BANDWIDTH	ALG PYRAMID 1	ALG PYRAMID 2
EMIF Read Only	Avg	553 MB/s	743 MB/s
	Peak	831 MB/s	1357 MB/s
EMIF Write Only	Avg	154 MB/s	176 MB/s
	Peak	384 MB/s	482 MB/s
EMIF Read + Write	Avg	708 MB/s	919 MB/s
	Peak	1159 MB/s	1822 MB/s

8.7 Other Benchmarks (TDA2xx)

8.7.1 Processing Latency

		LATENCY (CONFIG ALG PYRAMID 1)	LATENCY (CONFIG ALG PYRAMID 2)
Capture to Display Latency (Display VID 2)	Avg	26.5ms	40.9ms
	Min	26.3ms	40.5ms
	Max	27.1ms	41.5ms

NOTE:

- This latency is as measured inside the system by software.
- There will an additional 1/(capture rate) added on top of this from sensor/receiver itself.
- There will an additional 1/(display rate) added on top of this for the frame to actually get displayed on the screen.
- Thus e.g. in a scenario of display at 60fps and capture at 30fps - 16.67ms + 33.33ms needs to be added to latency figures in above table to get true capture to display latency

8.7.2 Boot Time

PARAMETER	DURATION (CONFIG 6 ALG PYRAMID 1)	DURATION (CONFIG 6 ALG PYRAMID 2)
SBL to App main() (QSPI Boot) The boot time will change based on the mode of boot – SD, NOR flash or QSPI.	1.599s	1.599s
main() to Use-case create	0.340s	0.340s
Use-case create start to Live preview on display	0.456s	0.255s
Total Boot time	**2.395s**	**2.194s**

QSPI Boot time measurement done with TDA2xx ES2.0 samples

GUI and Sensor initialization time not accounted for.

9 Single Channel Analytics2 on TDA2xx & TDA3xx - EUNCAP usecase

9.1 Overview

EUNCAP (European New Car Assessment Programme) provides consumers an independent assessment of the safety level with its five star rating systems for cars. Most of the OEMs in automotive market will strive to get highest start ranking for their car. This involves supporting algorithms required for autonomous emergency breaking, Prevention of Speed & Impaired Driving, and lateral assist systems. It is preferable to have it on a single central processing unit / ECU. The usecase showcases how this can be achieved with TDA3x efficiently; same use case works on TDA2x as well which has a lot more compute power.

9.2 DataFlow

9.2.1 Single channel analytics example

The demo accepts HD (720p / 1MP) video input from HDMI player, applies all below mentioned algorithms and produces output video augmented with information / results from algorithms.

- Pedestrian, Bi-cyclist and Powered Two Wheeler Detection
- Traffic Sign Detection and Recognition (TSR)
- Vehicle Detection (VD)
- Traffic Light Recognition (TLR)
- Lane Departure warning (LDW)
- Structure From Motion (SFM), Ground Plane Estimation and distance of objects on ground

These 6 algorithms run on 2 C66x DSPs and 1 EVE on TDA3x /TDA2x at OPP_NOM. Video input is a recorded video – “clip3” from VISION_SDK_02.XX.XX.XX.tar.gz

The term “analytics2” – This indicates this demo is significantly different than the traditional single cam analytics demo in VisionSDK. Compared to earlier FC analytics demo (until VisionSDK 2.8) this uses different alg plugins underneath and changes are done to show full entitlement of TDA3x SOC such that all 6 algorithms can co-exist in an optimized way to produce real time output for 1MP video. In addition to improved run-time, demo also shows improved output with accurate detections and significantly reduced false detections.

Image pyramid generation – The demo works on TDA3x and TDA2x both. Object Detect algorithm uses image pyramid (input image scaled down to different resolutions based on numScales and steps). The only difference between TDA3x and TDA2x is image pyramid generation; TDA3x uses ISS resizer to generate scales, while TDA2x uses VPE for the same. Traditionally, in the analytics demo this was happening on EVE, eating up almost 30% CPU, it is now being intelligently offloaded to h/w IPs (isp resizer / VPE) freeing up EVE for algorithmic computations.

Use of CNN - This use case exercise the latest deep learning technology convolution Neural Network (CNN) for object classification. CNN here helps in Object Classification and its currently being applied to recognize different traffic signs after localization of it. Based on training data and input from Object Detection algorithm this approach gives confidence on detected object and ensures accurate classification of the Traffic Sign.

Important functionalities

FCW using SFM – The purpose of detecting distance of an object from vehicle user is driving is to support Front Collision Warning and later Autonomous Emergency Breaking. Interestingly, demo shows how this can be achieved using single camera and *without any additional sensors'* input. SFM algorithm is used produce this information and gives distance of an object from bonnet.

LDW – Lane departure warning algorithm works on 640 x 360 resolutions to give Lane Departure Warning to the user, if vehicle departs right / left lane.

TLR – Red and Green traffic lights (signal lights) are detected and this can help in maneuvering car speed based on signal status.

PD/TSR/VD – The demo shows accurate detections of pedestrians, cyclists, vehicles and traffic signs. TSR can help in speed limit recognition while other ODs help for collision warning.

Please refer block diagram below which depicts complete data flow of the usecase and how it is achieved using 2 DSPs and 1 EVE.

Block Diagram:

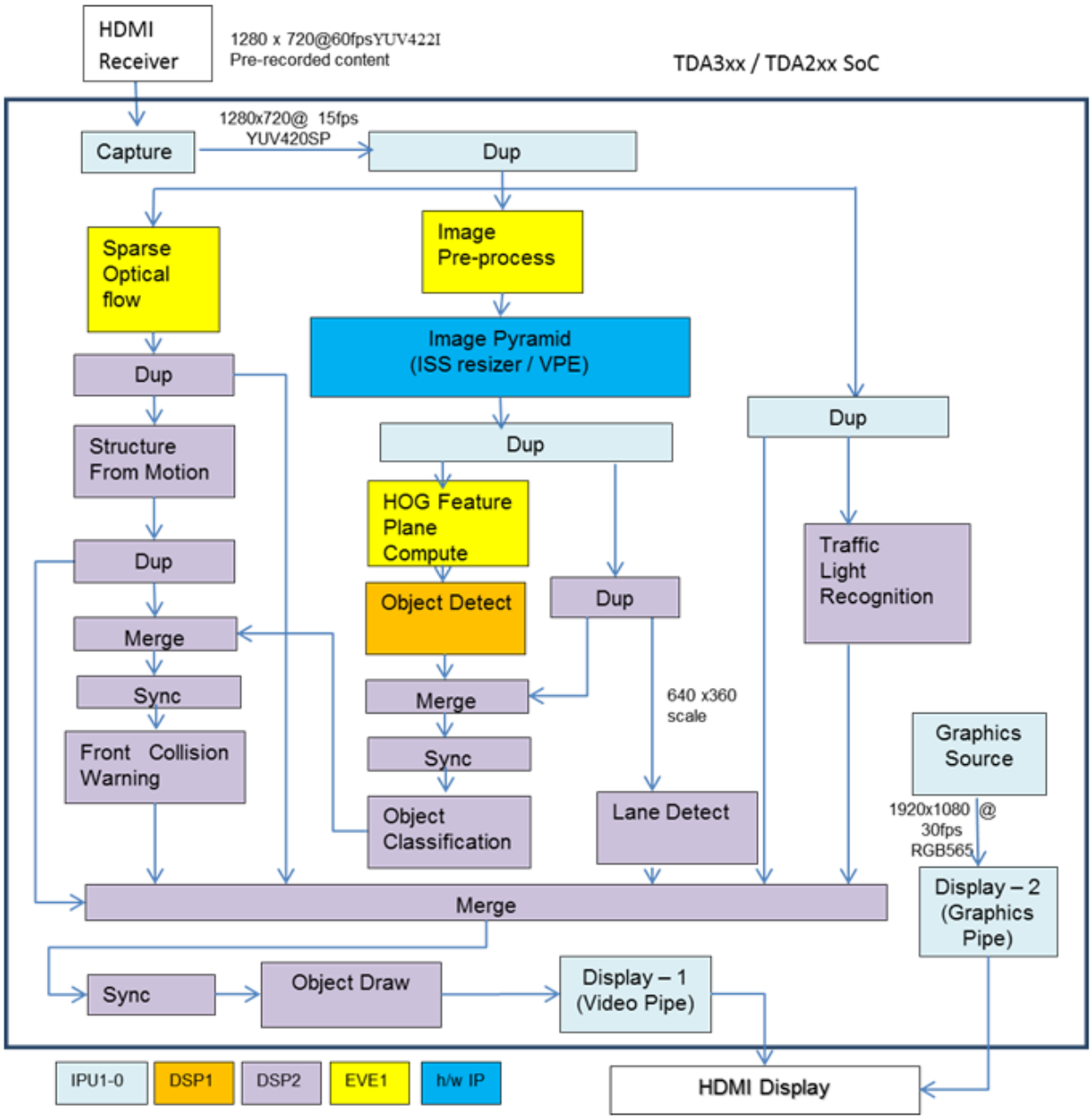


Figure – TDA3x / 2x based EUNCAP demo

**IPC IN/OUT blocks are left-out to improve readability.

9.3 System Parameters

Refer to section 2.1 for common system parameters.

The benchmarks in this section are computed for HDMI capture (1080p60) of pre-recorded content and HDMI display (1080p60) scenario.

9.4 CPU Loading and Task Info

9.4.1 Total CPU Load

CPU	LOAD TYPE	TDA2XX CPU LOAD	TDA3XX CPU LOAD
IPU1_0	**HWI**	4.0%	4.3%
	SWI	1.2%	0.8%
	Total	**28.2%**	**23.8%**
DSP1	**HWI**	0.3%	0.4%
	SWI	0.1%	0.2%
	Total	**38.9%**	**39.8%**
DSP2	**HWI**	0.6%	0.6%
	SWI	0.3%	0.3%
	Total	**23.6%**	**44.3%**
EVE1	**HWI**	1.3%	0.9%
	SWI	0.2%	0.2%
	Total	**76.9%**	**81.9%**

9.4.2 Task Level Information and Task Level CPU Load

CPU	TASK NAME	TASK DESCRIPTION	TDA2XX CPU LOAD	TDA3XX CPU LOAD
IPU1-0	Stat Collector	Statistics collector	4.0%	2.4%
	Capture	Capture frames from sensor via VIP port	0.6%	0.5%
	DUP	Duplicate frame to send to display without scaling as well as to VPE to scale	0.2%	0.2%
	Display	Display frames via DSS	0.3%	0.3%
	ALGORITHM0		9.1%	3.6%
	UNKNOWN	This is unaccounted CPU load after subtracting the individual task load from total CPU Load	2.1%	1.6%
	IPC OUT	To send frame to another processor	1.4%	1.3%
	IPC IN	To receive frames from another processor	0.2%	0.2%
DSP1	IPC + ALG Object Detect	IPC + Object detection algorithm	38.3%	39.0%

CPU	TASK NAME	TASK DESCRIPTION	TDA2XX CPU LOAD	TDA3XX CPU LOAD
	UNKNOWN	This is unaccounted CPU load after subtracting the individual task load from total CPU Load	0.2%	0.2%
DSP2	IPC + ALG Lane Detect	IPC + multiple algorithms	22.5%	43.1%
	UNKNOWN	This is unaccounted CPU load after subtracting the individual task load from total CPU Load	0.2%	0.3%
EVE1	IPC + Feature plane compute	Feature plane compute algorithm + IPC	75.1%	80.4%
	UNKNOWN	This is unaccounted CPU load after subtracting the individual task load from total CPU Load	0.3%	0.4%

NOTE: CPU load of 0.0% means the CPU load was so low it could not be measured with sufficient granularity in load calculations

NOTE: There could be minor variations of +/-0.1% CPU load in different runs of the same use-case

NOTE: Graphics Load is not accounted for in these measurements.

NOTE: Other than above tasks few additional tasks as listed below are active in each processor

- Message Q task: This task is used to listen to control messages sent by any other core. Normally at run-time very few control messages are sent hence this task does not appear in the task load print log
- Processor link task: This task is used to send generic non-link specific messages to another CPU. Normally at run-time very few messages are sent to this task hence this task does not appear in the task load print log
- Remote log client task (on IPU1-0 only): This task looks at the shared remote log buffer and outputs any strings to UART terminal. Normally during run-time prints are not done hence this task does not appear in the task load log

9.5 System Performance

COMPONENT	PARAMETER	TDA2XX	TDA3XX
Capture	Output fps	15fps	15fps
ALG – SOF (EVE1)	Output fps	15fps	15fps
	Avg time per frame	22.2ms	20.7ms
ALG – SFM (DSP2)	Output fps	15fps	15fps
	Avg time per frame	2.69ms	2.83ms
ALG_IMAGEPREPROCESS (EVE1)	Output fps	15fps	15fps
	Avg time per frame	6.72ms	6.65ms
ALG_IMG_PYRAMID	Output fps	15fps	15fps
	Avg time per frame	19.3ms	18.8ms

Lane Detect (DSP2)	Output fps	15fps	15fps
	Avg time per frame	2.37ms	2.35ms
ALG_CLR (DSP2)	Output fps	15fps	15fps
	Avg time per frame	4.67ms	11.6ms
Feature Plane Compute (EVE1)	Output fps	15fps	15fps
	Avg time per frame	20.5ms	22.7ms
Object Detect (DSP1)	Output fps	15fps	15fps
	Avg time per frame	24.1ms	30.1ms
Object classification (DSP2)	Output fps	15fps	15fps
	Avg time per frame	1.54ms	0.84ms
ALG_FCW (DSP2)	Output fps	15fps	15fps
	Avg time per frame	1.76ms	1.82ms
Object Draw (DSP2)	Output fps	15fps	15fps
	Avg time per frame	2.58ms	2.63ms
Display VID 1	Input fps	15fps	15fps
	VENC fps	60fps	60fps

NOTE: FPS numbers are rounded off to nearest integer
NOTE: The figures are for HDMI capture scenario.
NOTE: Performance data captured here is with OPP_NORM. Use OPP_HIGH MLO to get higher performance/FPS

9.6 System Memory Usage

9.6.1 Code/Data Memory Usage

Refer section 2.2 for common Code/Data Memory usage

9.6.2 Heap Memory Usage

CPU	MEMORY SECTION	MEMORY SIZE RESERVED	TDA2XX MEMORY SIZE USED	TDA3XX MEMORY SIZE USED
IPU1-0	Local Heap	256 KB	20 KB	13 KB
	HDVPSS Descriptor Mem	1MB/256 KB	114 KB	36 KB
DSP1	L2	221 KB	208 KB	208 KB
	Local Heap	512 KB	13 KB	9 KB
DSP2	L2	221 KB	0KB	0KB
	Local Heap	512 KB	45 KB	40 KB
EVE1	L2	24 KB	19 KB	19 KB
	Local Heap	256KB	45 KB	41 KB
Shared Memory	SR0	128 KB/1MB	36 KB	7 KB
	Frame Buffer (SR1)	350 MB/351 MB	166 MB	164 MB
	SR2 OCMC	0 KB	0 KB	0KB
	Remote Log Buffer	160 KB	158 KB	158 KB

9.6.3 DDR Bandwidth

PARAMETER	BANDWIDTH	TDA2XX	TDA3XX
EMIF Read Only	Avg	876 MB/s	NA
	Peak	1394 MB/s	NA
EMIF Write Only	Avg	381 MB/s	NA
	Peak	949 MB/s	NA
EMIF Read + Write	Avg	1257 MB/s	1209 MB/s
	Peak	2217 MB/s	2184 MB/s

9.7 Other Benchmarks

9.7.1 Processing Latency

		TDA2XX LATENCY	TDA3XX LATENCY
Capture to Display Latency (Display VID 2)	Avg	122.6ms	131.3ms
	Min	101.5ms	86.6ms
	Max	161.2ms	168ms

NOTE:

- This latency is as measured inside the system by software.
- There will an additional 1/(capture rate) added on top of this from sensor/receiver itself.
- There will an additional 1/(display rate) added on top of this for the frame to actually get displayed on the screen.
- Thus e.g. in a scenario of display at 60fps and capture at 30fps - 16.67ms + 33.33ms needs to be added to latency figures in above table to get true capture to display latency

9.7.2 Boot Time

PARAMETER	TDA2XX DURATION	TDA3XX DURATION
SBL to App main() (QSPI Boot) The boot time will change based on the mode of boot – SD, NOR flash or QSPI.	1.599s	1.636s
main() to Use-case create	0.340s	0.222s
Use-case create start to Live preview on display	0.575s	0.689s
Total Boot time	**2.514s**	**2.547s**

QSPI Boot time measurement done with TDA2xx ES2.0 samples

GUI and Sensor initialization time not accounted for.

10 Multi-channel LVDS 2D Surround view on TDA2xx & TDA2Ex

10.1 Overview

This use case consists of capture from multiple OV10635 camera's. The camera's are connected to TDA2Ex via FPD link with serializer and de-serializers in between. This configuration demonstrates a 2D Surround View on 4 Channels input. Only HDMI display is supported by this use-case.

10.2 Data Flow

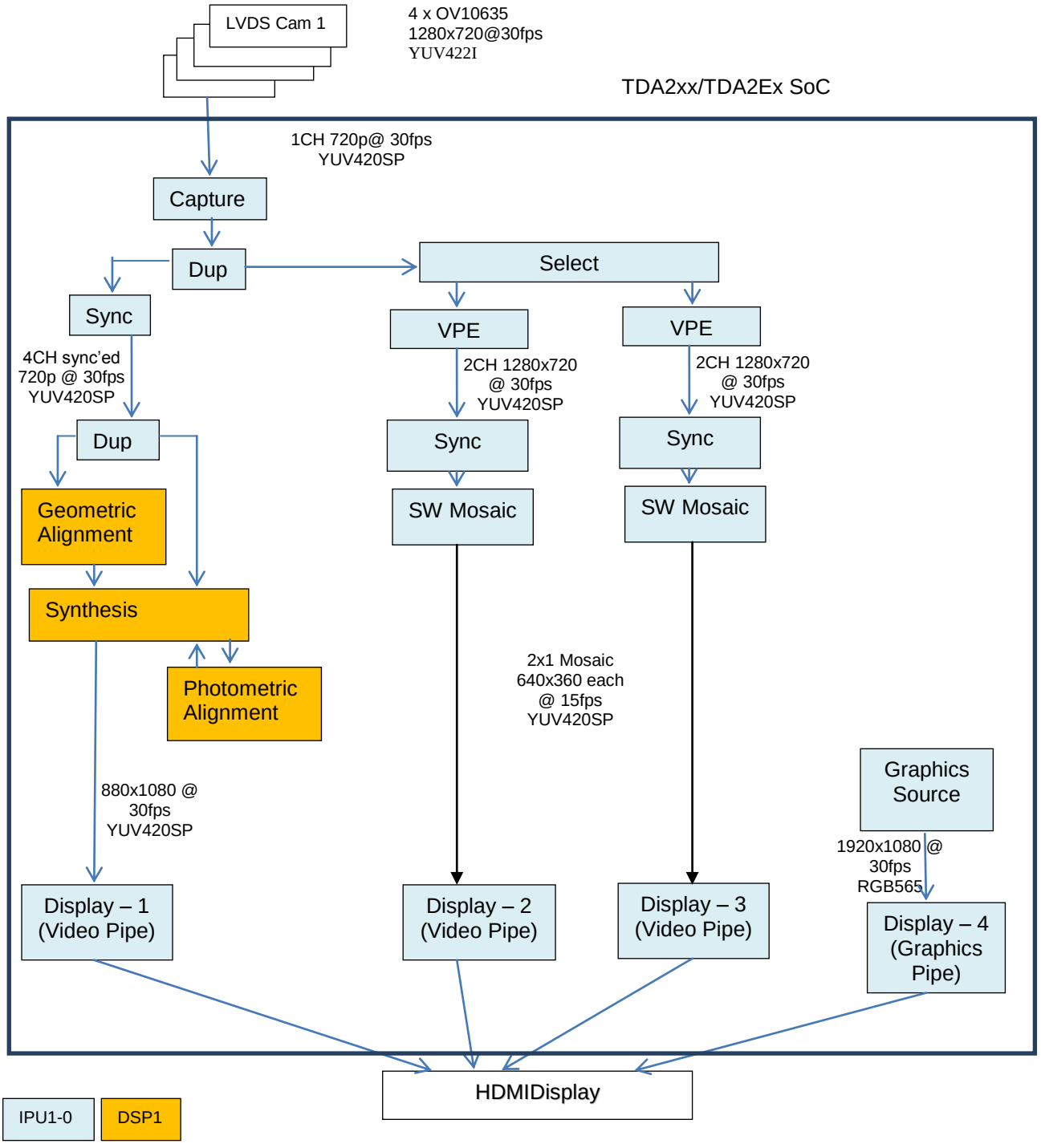
10.2.1 4CH LVDS capture, 2D Surround View demonstration

In this configuration we capture 4 Channel video from 4 OV1063x sensors @ 720p 30fps.

This 4 Channel data is duped. Using Select, VPE, Sync and Mosaic links the original data is downscaled and displayed as two 2x1 Mosaics.

The 4 Channels data via second path on DUP is sent to Sync Link where these captured frames are synced based on time stamps. After syncing we get a "group of sync'ed frames", one frame from each camera. This "group of sync'ed frames" areDup'ed. One set is passed on to algorithm links of Geometric alignment and synthesis link. Geometric alignment link provides look up table for geometric alignment among multiple views. Further Photometric alignment provides look up table for pixel transformations to compensate for the difference in lighting among different cameras. Based on these two look up tables and original 4 Ch Data, the Synthesis stage generates 2D surround view which is shown on the display.

Please note in dataflow diagram below IPC IN/OUT blocks are left-out to improve readability. Please assume these whenever CPU changes in the flow.



**IPC IN/OUT blocks are left-out to improve readability.

10.3 System Parameters (TDA2xx/ TDA2Ex)

Refer section 2.1 for common system parameters.

The parameters in this section are computed for HDMI display.

10.4 CPU Loading and Task Info (TDA2xx/TDA2Ex)

10.4.1 Total CPU Load

CPU	LOAD TYPE	TDA 2XX CPU LOAD	TDA 2EX CPU LOAD
IPU1_0	HWI	5.1%	5.1%
	SWI	1.2%	1.1%
	Total	**28.7%**	**25.1%**
DSP1	HWI	0.6%	0.5%
	SWI	0.2%	0.1%
	Total	**49.8%**	**47.4%**

10.4.2 Task Level Information and Task Level CPU Load

CPU	TASK NAME	TASK DESCRIPTION	TDA 2XX CPU LOAD	TDA 2EX CPU LOAD
IPU1_0	Capture	Capture frames from sensor via VIP port	1.0%	0.9%
	Display (4 links)	Display frames/graphics via DSS	1.7%	1.4%
	VPE (2 links)	Scale frames	4.7%	4.1%
	SYNC (3 links)	Sync frames based on timestamp from multiple channels	2.8%	2.4%
	DUP (2 links)	Duplicate frame to send to display without scaling as well as to VPE to scale	1.1%	1.0%
	Select	Selects specific channel data from i/p queue	0.5%	0.4%
	SW Mosaic (2 links)	Composite synced frames from multiple channels to form a single composite frame	1.5%	1.3%
	UNKNOWN	This is unaccounted CPU load after subtracting the individual task load from total CPU Load	2.3%	1.8%
	IPC OUT (2 links)	To send frame to another processor	1.3%	1.3%
	IPC IN	To receive frames from another processor	0.3%	0.3%
DSP1	IPC +GAlign+PAlign+Synthesis +	All DSP1 Processing algorithms	48.8%	46.5%
	UNKNOWN	This is unaccounted CPU load after subtracting the individual task load from total CPU Load	0.2%	0.3%

*NOTE: On DSP and similarly on EVE all links run in a single thread.

NOTE: CPU load of 0.0% means the CPU load was so low it could not be measured with sufficient granularity in load caclulations

NOTE: There could be minor variations of +/-0.1% CPU load in different runs of the same use-case

NOTE: Graphics load is not accounted for in these measurements

NOTE: Other than above tasks few additional tasks as listed below are active in each processor

- Message Q task: This task is used to listen to control messages sent by any other core. Normally at run-time very few control messages are sent hence this task does not appear in the task load print log
- Processor link task: This task is used to send generic non-link specific messages to another CPU. Normally at run-time very few messages are sent to this task hence this task does not appear in the task load print log
- Remote log client task (on IPU1-0 only): This task looks at the shared remote log buffer and outputs any strings to UART terminal. Normally during run-time prints are not done hence this task does not appear in the task load log

10.5 System Performance (TDA2xx/TDA2Ex)

COMPONENT	PARAMETER	SRV 4CH FOR *Capture to Display1 path ONLY*	SRV 4CH FOR *Capture to Display1 path ONLY*
Capture	Output fps	30fps each on 4 Channels for SV	30fps each on 4 Channels for SV
ALG Synthesis (DSP1)	Output fps	30fps	30fps
	Avg time per frame	13.9ms	13.1ms
ALG – Photometric Align(DSP1)	Output fps	30fps	30fps
	Avg time per frame	1.05ms	1.03ms
Display VID 1	Input fps	30fps	30fps
	VENC fps	60fps	60fps

NOTE: FPS numbers are rounded off to nearest integer
NOTE: The above figures are for HDMI display.

10.6 System Memory Usage (TDA2xx)

10.6.1 Code/Data Memory Usage

Refer section 2.2 for common Code/Data Memory usage.

10.6.2 Heap Memory Usage

CPU	MEMORY SECTION	MEMORY SIZE RESERVED	TDA 2XX MEMORY SIZE USED	TDA 2EX MEMORY SIZE USED
IPU1-0	Local Heap	256 KB	21 KB	17 KB
	HDVPSS Descriptor Mem	1MB	1MB	1MB
DSP1	L2	221 KB	128 KB	128 KB
	Local Heap	512 KB	11 KB	6 KB
Shared Memory	SR0	128 KB	36 KB	7 KB
	Frame Buffer (SR1)	350 MB	151 MB	151 MB
	SR2 OCMC	0KB	0 KB	0 KB
	Remote Log Buffer	160 KB	158 KB	158 KB

10.6.3 DDR Bandwidth

PARAMETER	TDA 2XX BANDWIDTH		TDA 2EX BANDWIDTH
EMIF1 Read Only	Avg	1001 MB/s	962 MB/s
	Peak	1846 MB/s	1946 MB/s
EMIF1 Write Only	Avg	319 MB/s	303 MB/s
	Peak	516 MB/s	557 MB/s
EMIF1 Read + Write	Avg	1319 MB/s	1266 MB/s
	Peak	2340 MB/s	2386 MB/s

10.7 Other Benchmarks (TDA2xx)

10.7.1 Processing Latency

		TDA 2XX LATENCY	TDA 2EX LATENCY
Capture to Display Latency (Display VID 1)(SV)	Avg	32.6ms	18.8ms
	Min	32.01ms	18.5ms
	Max	33.1ms	19.3ms

NOTE:

- This latency is as measured inside the system by software.
- There will an additional 1/(capture rate) added on top of this from sensor/receiver itself.
- There will an additional 1/(display rate) added on top of this for the frame to actually get displayed on the screen.
- Thus e.g. in a scenario of display at 60fps and capture at 30fps - 16.67ms + 33.33ms needs to be added to latency figures in above table to get true capture to display latency

10.7.2 Boot Time

PARAMETER	TDA 2XX VALUE	TDA 2EX VALUE
SBL to App main() (QSPI Boot) The boot time will change based on the mode of boot – SD, NOR flash or QSPI.	1.599s	1.461s
main() to Use-case create	0.340s	0.849s
Use-case create start to Live preview on display	2.546s	2.428s
Total Boot time	**4.485s**	**4.738s**

QSPI Boot time measurement done with TDA2xx ES2.0 samples

GUI and Sensor initialization time not accounted for.

11 Multi-channel AVB 2D Surround view Use case on TDA2xx & TDA2ex

11.1 Overview

This use case consists of AVB capture (Ethernet based input).The received data is in MJPEG format and decoded. This configuration demonstrates a 2D Surround View on 4 Channels input and Edge Detect on single channel in parallel. Only HDMI display is supported by this use-case.

11.2 Data Flow

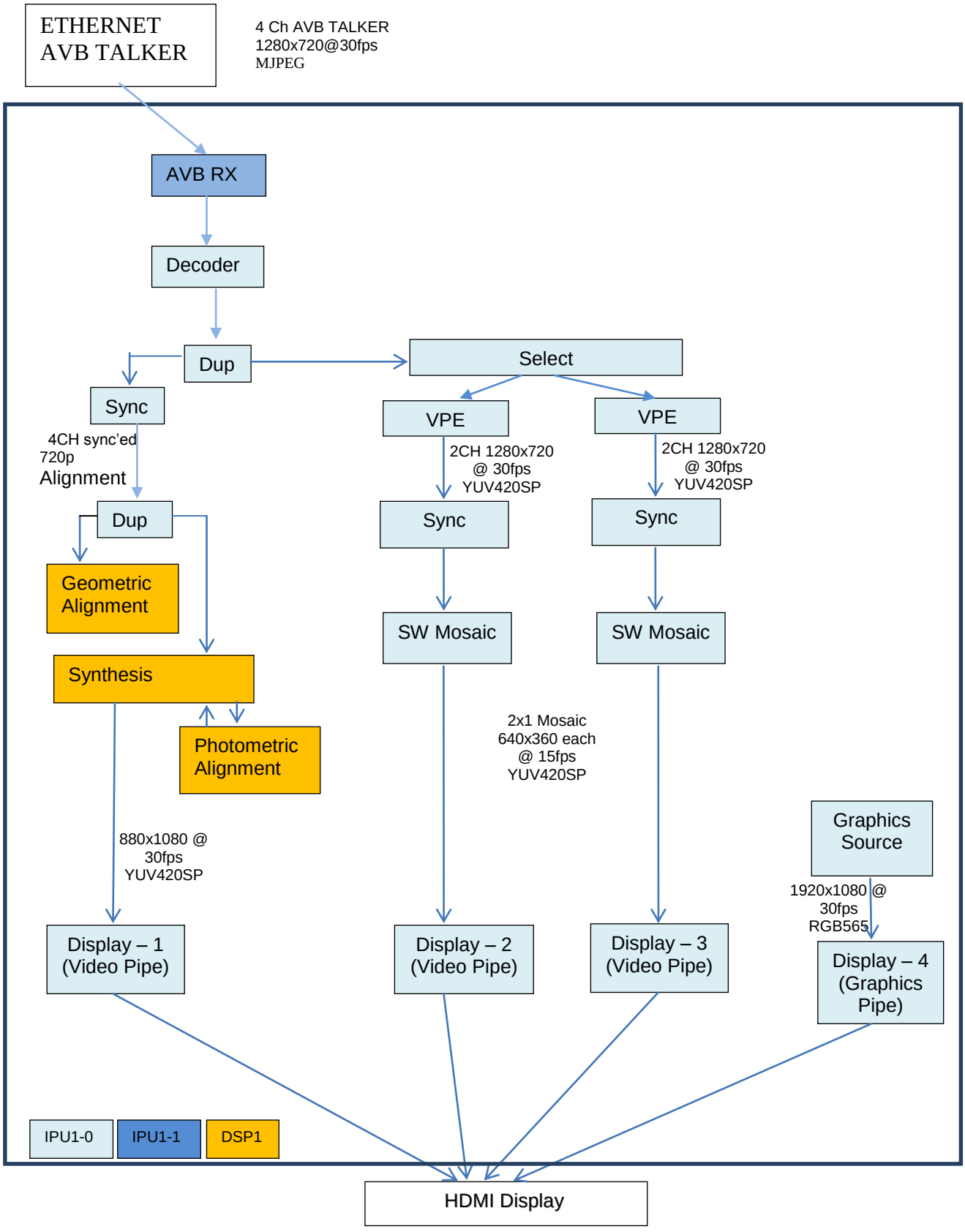
11.2.1 Configuration 10: 4CH AVB capture, 2D Surround View demonstration

In this configuration we receive 4 Channel video from AVB Talker @ 720p 30fps per channel. These streams are decoded using MJPEG decoder. The original image from this channel is then Merged, Synced and displayed onto HDMI as a 2x1 Mosaic.

This 4 Channel data is duped. Using Select, VPE, Sync and Mosaic links the original data is downscaled and displayed as two 2x1 Mosaics.

The 4 Channels data via second path on DUP is sent to Sync Link where these captured frames are synced based on time stamps. After syncing we get a "group of sync'ed frames", one frame from each camera. This "group of sync'ed frames" are Dup'ed. One set is passed on to algorithm links of Geometric alignment and synthesis link. Geometric alignment link provides look up table for geometric alignment among multiple views. Further Photometric alignment provides look up table for pixel transformations to compensate for the difference in lighting among different cameras. Based on these two look up tables and original 4 Ch Data, the Synthesis stage generates 2D surround view which is shown on the display.

Please note in dataflow diagram below IPC IN/OUT blocks are left-out to improve readability. Please assume these whenever CPU changes in the flow.


ETHERNET AVB TALKER
4 Ch AVB TALKER
1280x720@30fps
MJPEG
AVB RX
Decoder
Dup
Select
Sync
VPE
VPE
4CH sync'ed 720p Alignment
2CH 1280x720 @ 30fps YUV420SP
2CH 1280x720 @ 30fps YUV420SP
Dup
Sync
Sync
Geometric Alignment
SW Mosaic
SW Mosaic
Synthesis
Photometric Alignment
2x1 Mosaic 640x360 each @ 15fps YUV420SP
Graphics Source
880x1080 @ 30fps YUV420SP
1920x1080 @ 30fps RGB565
Display – 1 (Video Pipe)
Display – 2 (Video Pipe)
Display – 3 (Video Pipe)
Display – 4 (Graphics Pipe)
IPU1-0
IPU1-1
DSP1
HDMI Display

11.3 System Parameters (TDA2xx)

Refer section 2.1 for common system parameters.

The parameters in this section are computed for HDMI display scenario.

All cores are operating with OPP_HIGH

Core	TDA2xx (MHz)	TDA2Ex (MHz)
MPU	1176. 0	800.0
IPU1_0	212.8	212.8
IPU1_1	212.8	212.8
IPU2	212.8	212.8
DSP1	748. 0	748. 0
DSP2	748. 0	
EVE1	650. 0	
EVE2	650. 0	
EVE3	650. 0	
EVE4	650. 0	
IVA	532. 0	532.0

11.4 CPU Loading and Task Info (TDA2xx)

11.4.1 Total CPU Load

CPU	LOAD TYPE	CPU LOAD TDA2XX (%)	CPU LOAD TDA2EX (%)
IPU1-0	HWI	3.8%	3.3%
	SWI	1.8%	1.6%
	Total	**29.3%**	**27.2%**
IPU1-1	HWI	6.3%	5.2%
	SWI	1.0%	0.8%
	Total	**28.0%**	**24.4%**
DSP1	HWI	0.3%	0.5%
	SWI	0.1%	0.1%
	Total	**26.4%**	**43.6%**

11.4.2 Task Level Information and Task Level CPU Load

CPU	TASK NAME	TASK DESCRIPTION	CPU LOAD (SRV 4CH) TDA2XX	CPU LOAD (SRV 4CH) TDA2EX
IPU1-0	Stat Collector	Statistics collector	4.6%	2.3%
	Decoder	Decoder the mjpeg frame	2.2%	3.0%
	Display	Display frames	0.4%	0.5%

CPU	TASK NAME	TASK DESCRIPTION	CPU LOAD (SRV 4CH) TDA2XX	CPU LOAD (SRV 4CH) TDA2EX
	Sync	Sync frames based on timestamp from multiple channels	1.1%	1.6%
	DUP	Duplicate frame to send to display without scaling as well as to VPE to scale	0.1%	0.2%
	IPC OUT (3 links)	To send frame to another processor	2.2%	1.2%
	IPC IN (2 links)	To receive frames from another processor	1.1%	1.5%
	UNKNOWN	This is unaccounted CPU load after subtracting the individual task load from total CPU Load	2.1%	1.6%
IPU1-1	AVBTX	Receives frames from network	1.1%	0.4%
	IPC OUT	To send frame to another processor	1.4%	1.7%
	IPC IN	To receive frames from another processor	0.8%	0.3%
	UNKNOWN	This is unaccounted CPU load after subtracting the individual task load from total CPU Load	17.4%	16.7%
DSP1	IPC + ALG GALIGN + ALG PALIGN	IPC+ Alg processing	25.8%	42.8%
	UNKNOWN	This is unaccounted CPU load after subtracting the individual task load from total CPU Load	0.2%	0.2%

*NOTE: On EVE all links run in a single thread.

NOTE: CPU load of 0.0% means the CPU load was so low it could not be measured with sufficient granularity in load calculations

NOTE: There could be minor variations of +/-0.1% CPU load in different runs of the same use-case

NOTE: Graphics load is not accounted for in these measurements.

NOTE: Other than above tasks few additional tasks as listed below are active in each processor

- Message Q task: This task is used to listen to control messages sent by any other core. Normally at run-time very few control messages are sent hence this task does not appear in the task load print log
- Processor link task: This task is used to send generic non-link specific messages to another CPU. Normally at run-time very few messages are sent to this task hence this task does not appear in the task load print log

- Remote log client task (on IPU1-0 only): This task looks at the shared remote log buffer and outputs any strings to UART terminal. Normally during run-time prints are not done hence this task does not appear in the task load log

11.5 System Performance (TDA2xx and TDA2ex)

COMPONENT	PARAMETER	SRV 4CH FOR *Capture to Display1 path ONLY TDA2xx*	SRV 4CH FOR *Capture to Display1 path ONLY TDA2ex*
AVB (IPU1-1)	Output FPS	120fps over 4 channels	120fps over 4 channels
	Data Rate	360 Mbps	360 Mbps
Decoder	Output FPS	120fps over 4 channels	120fps over 4 channels
	Avg time per frame	17ms	20.2ms
ALG Synthesis (DSP1)	Output fps	30fps	30fps
	Avg time per frame	13.9ms	13.8ms
ALG – Photometric Align(DSP1)	Output fps	30fps	30fps
	Avg time per frame	0.7ms	0.93ms
Display	Input FPS	30fps	30fps
	VENC FPS	60fps	60fps

NOTE: Since a AVB talker is used instead of live camera feed the fps on each channel is not fixed
NOTE: Linux talker sends the data in burst of frames which leads to drop at sync and decoder
NOTE: Only numbers for the AVB Capture to Display 1 path i.e. path for Surround view is shown above
NOTE: FPS numbers are rounded off to nearest integer.
NOTE: The above figures are for HDMI display.

11.6 System Memory Usage (TDA2xx & TDA2ex)

11.6.1 Code/Data Memory Usage

Refer section 2.2 for common Code/Data Memory usage.

11.6.2 Heap Memory Usage TDA2xx & TDA2ex

CPU	MEMORY SECTION	MEMORY SIZE RESERVED	TDA 2XX MEMORY SIZE USED	TDA 2EX MEMORY SIZE USED
IPU1-0	Local Heap	256 KB	18 KB	13 KB
	HDVPSS Descriptor Mem	1MB	1MB	1MB
IPU1-1	Local Heap	640 KB	39 KB	35 KB
DSP1	L2	221KB	128 KB	128 KB
	Local Heap	512 KB	11 KB	6 KB
Shared	SR0	128KB	128 KB	128 KB

Memory	Frame Buffer (SR1)	350MB	181 MB	181 MB
	SR2 OCMC	0KB	0 KB	0 KB
	Remote Log Buffer	160 KB	158 KB	158 KB

11.6.3 DDR Bandwidth TDA2xx & TDA2ex

PARAMETER	BANDWIDTH	TDA2XX	TDA2EX
EMIF Read Only	Avg	718 MB/s	710 MB/s
	Peak	1783 MB/s	1303 MB/s
EMIF Write Only	Avg	553 MB/s	635 MB/s
	Peak	932 MB/s	855 MB/s
EMIF Read + Write	Avg	1270 MB/s	1344 MB/s
	Peak	2376 MB/s	2068 MB/s

11.7 Other Benchmarks (TDA2xx)

11.7.1 Processing Latency

This benchmark has not been measured for this configuration due to a known issue in Vision SDK stack where the latency figures are not initialized correctly.

11.7.2 Boot Time

PARAMETER	VALUE
SBL to App main() (QSPI Boot) The boot time will change based on the mode of boot – SD, NOR flash or QSPI.	1.599s
main() to Use-case create	1.30 s
Use-case create start to Live preview on display	2.23s (Talker should be started immediately)
Total Boot time	5.129s

QSPI Boot time measurement done with TDA2xx ES2.0 samples

GUI and Sensor initialization time not accounted for.

12 File Input/Output TI Deep Learning (TIDL) use case on TDA2XX

12.1 Overview

This use case reads the BGR planar input frames from the input file present on MMC/SD card applies the TIDL algorithm which is running on either EVE/DSP core and writes the output frame to the output file created on MMC/SD card.

The TIDL reads the 'network file' and 'parameter files' from the MMC/SD card which are the pre-requisites.

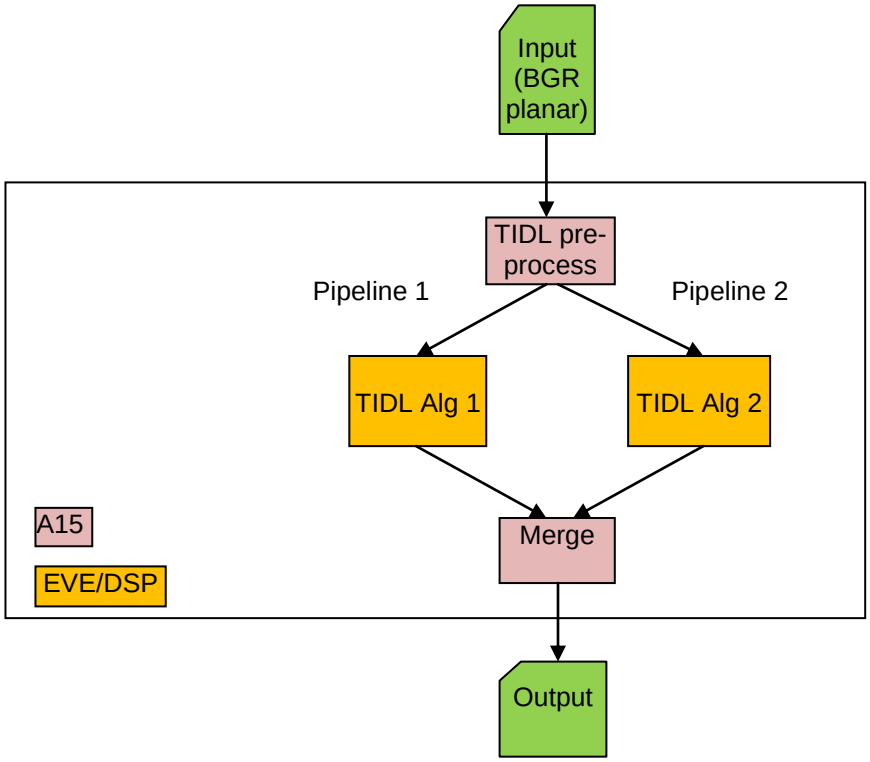
The TIDL generates an 8 bit class ID (0-4) for every input pixel. This class ID represents the segment into which the input pixel belongs to.

The FIVE segments supported are:

Class ID	Segment
0	None
1	Road
2	Pedestrian
3	Traffic Sign
4	Vehicle

12.2 Data Flow

The TIDL use case has one or more (up to 4 on EVE and up to 2 on DSP) processing pipelines which runs TIDL on the entire input frame. Every pipeline runs either on EVE core or DSP core.



12.3 TIDL performance

12.3.1 TIDL on DSP

DSP frequency = 600 MHz

Time taken to process one frame of resolution 1024x512 = 1006.07 ms

12.3.2 TIDL on EVE

EVE frequency = 535 MHz

Time taken to process one frame of resolution 1024x512 = 299.94 ms

13 ISS Capture Display Use case on TDA3xx

13.1 Overview

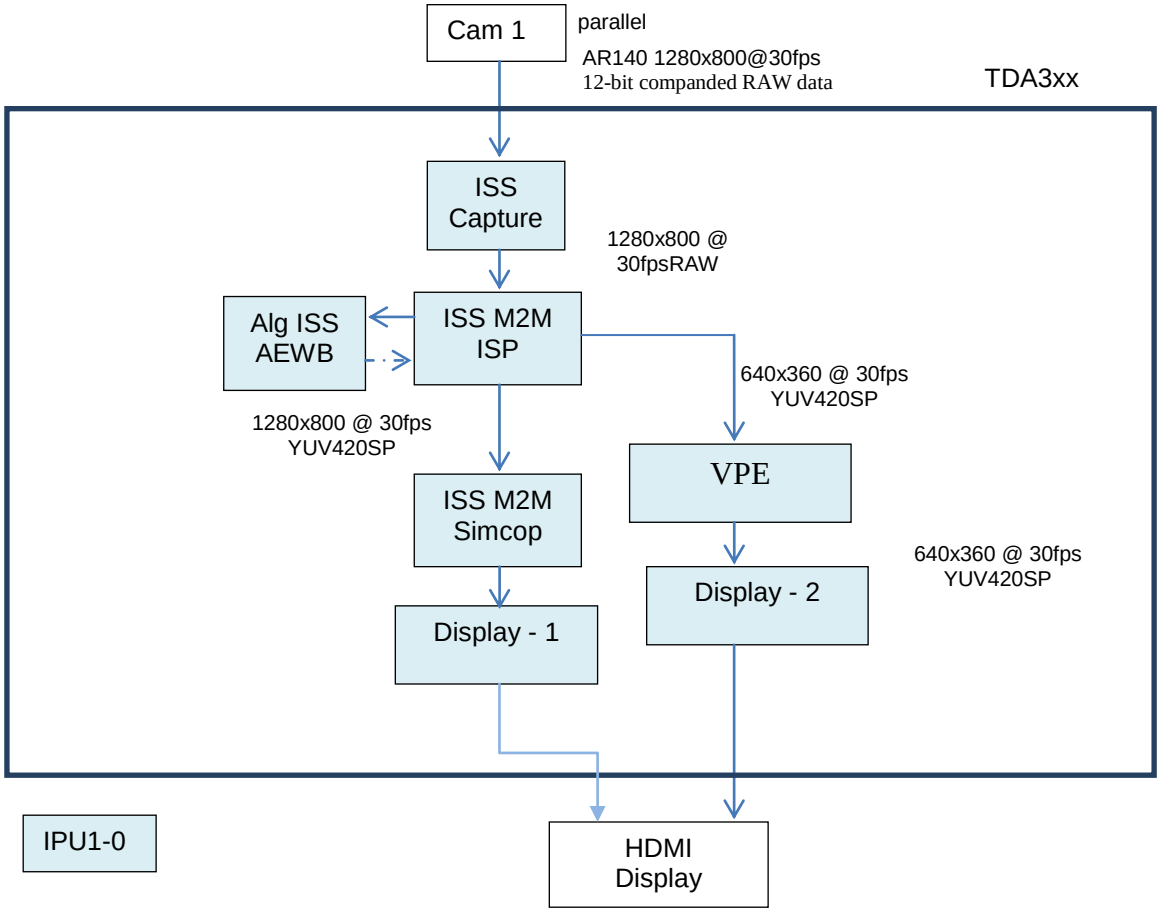
This configuration is used to demonstrate the ISS on TDA3xx.

13.2 Data Flow

13.2.1 ISS Capture Display example

In the ISS use-case, raw bayer data is captured from image sensor, like OV10640 or AR0140, by the ISS capture link. For OV10640 sensor capture is at 1280x720, whereas for AR140 it is at 1280x800. The sensor interface can be CSI2 or parallel. The bits/pixel of the raw data depends on the sensor and sensor mode being used, e.g. with AR140, 12-bit companded mode is used. The raw bayer data is fed to M2M (memory-to-memory) ISP (Image Signal Processor) link to convert it to YUV data. The ISP can operate in 2-pass WDR mode or 1-pass linear mode depending on sensor mode. There are two outputs from M2M ISP – Resizer A output of 1280x800 given to M2M SIMCOP, and Resizer B output of 640x360 sent to HDMI display. The M2M SIMCOP which performs optional LDC (Lens Distortion Correction) and/or VTNF (Video Temporal Noise Filter). The output of M2M SIMCOP is semt to HDMI display. The M2M ISP also outputs statistical data for the AE/AWB algorithm plugin. The AE/AWB algorithm feedback is applied to the M2M ISP link and/or sensor.

The data flow below shows HDMI display.



13.3 System Parameters (TDA3xx)

Refer to section 5.1 for common system parameters.

The benchmarks in this section are computed for AR0140 Parallel sensor and HDMI display (1080p60) scenario.

13.4 CPU Loading and Task Info (TDA3xx)

13.4.1 Total CPU Load

CPU	LOAD TYPE	CPU LOAD
IPU1_0	**HWI**	2.9%
	SWI	0.5%
	Total	**20.4%**
ISP		**17.6%**

13.4.2 Task Level Information and Task Level CPU Load

CPU	TASK NAME	TASK DESCRIPTION	CPU LOAD
IPU1_0	ISS Capture	ISS Capture	0.2%
	ISSM2MISP	ISS memory to memory ISP	2.0%
	ISSM2MSIM COP	ISS memory to memory LDC+VTNF	0.7%
	ISS-Resizer0	ISS-Resizer0	1.4%
	Display	Display via DSS	0.7%
	Alg ISS AEWB	ISS Auto White Balance	5.7%
	Stat Collector	Statistics collector	2.2%
	UNKNOWN	This is unaccounted CPU load after subtracting the individual task load from total CPU Load	1.3%

NOTE: CPU load of 0.0% means the CPU load was so low it could not be measured with sufficient granularity in load caclulations

NOTE: There could be minor variations of +/-0.1% CPU load in different runs of the same use-case

NOTE: Graphics load is not accounted for in these measurements.

NOTE: Other than above tasks few additional tasks as listed below are active in each processor

- Message Q task: This task is used to listen to control messages sent by any other core. Normally at run-time very few control messages are sent hence this task does not appear in the task load print log
- Processor link task: This task is used to send generic non-link specific messages to another CPU. Normally at run-time very few messages are sent to this task hence this task does not appear in the task load print log

- Remote log client task (on IPU1-0 only): This task looks at the shared remote log buffer and outputs any strings to UART terminal. Normally during run-time prints are not done hence this task does not appear in the task load log

13.5 System Performance (TDA3xx)

COMPONENT	PARAMETER	
ISS Capture	Output fps	30fps
ISS M2M ISP	Input fps	30fps
	Output fps	30fps
	Avg time per frame	5.88ms
ISS M2M SIMCOP	Input fps	30fps
	Output fps	30fps
	Avg time per frame	5.27ms
ISS Resizer	Input fps	30fps
	Output fps	30fps
	Avg time per frame	2.46ms
Algorithm AEWB	Input fps	30fps
	Output fps	30fps
	Avg time per frame	1.98ms
Display	Input fps	30fps
	VENC fps	60fps

NOTE: FPS numbers are rounded off to nearest integer

13.6 System Memory Usage (TDA3xx)

13.6.1 Code/Data Memory Usage

Refer section 5.2 for common Code/Data Memory usage

13.6.2 Heap Memory Usage

CPU	MEMORY SECTION	MEMORY SIZE RESERVED	MEMORY SIZE USED
IPU1-0	Local Heap	256 KB	13 KB
	HDVPSS Descriptor Mem	256 KB	36 KB
Shared Memory	SR0	1MB	0MB
	Frame Buffer (SR1)	351 MB	29 MB
	Remote Log Buffer	160 KB	158 KB

13.7 Other Benchmarks (TDA3xx)

13.7.1 Processing Latency

		LATENCY
Capture to Display Latency (Display VID 1)	Avg	8.95ms
	Min	8.87ms
	Max	10.49ms

NOTE:

- This latency is as measured inside the system by software.
- There will an additional 1/(capture rate) added on top of this from sensor/receiver itself.
- There will an additional 1/(display rate) added on top of this for the frame to actually get displayed on the screen.
- Thus e.g. in a scenario of display at 60fps and capture at 30fps - 16.67ms + 33.33ms needs to be added to latency figures in above table to get true capture to display latency

13.7.2 DDR Bandwidth

PARAMETER	BANDWIDTH	
EMIF Read + Write	Avg	715 MB/s
	Peak	1608 MB/s

13.7.3 Boot Time

PARAMETER	DURATION
SBL to App main() (QSPI Boot) The boot time will change based on the mode of boot – SD, NOR flash or QSPI.	1.636s
main() to Use-case create	0.222s
Use-case create start to Live preview on display	0.581s
Total Boot time	**2.439s**

QSPI Boot time measurement done with TDA3xx ES2.0 samples

GUI and Sensor initialization time not accounted for.

14 3D Surround View on TDA3xx

14.1 Overview

This usecase demonstrates a 4 channel 3D Surround View on TDA3x. 4 Channels of video is captured from four IMI/TIDA00262 sensors aggregated using UB960 and transmitted over CSI2 interface, CAL is used receive multiplexed video stream via CSI2 interface, ISP is used to convert from Bayer to YUV, DeWarp and Synthesis algorithms are used to generate 3D SRV. Please refer the TDA3xx user guide for required hardware setup. Only HDMI display is supported by this use-case.

14.2 Data Flow

14.2.1 4Ch capture Surround view demonstration

This usecase captures 4 Channel video from 4 IMI (OV10640) /AR0140 sensors @ 1280x720 / 1280x800 @30fps over CSI2 interface in Bayer Format (RAW12)

The ISP is used convert Bayer to YUV420 format, Select link is used provide H3A output channel 0 of ISP output to AEWB algorithm. AEWB algorithm will use this channel to determine exposure, and white balance. All processed channel are provided to synchronization link.

The Synchronization link will ensure all video streams are in same time line and provide synchronized output DeWarp Algorithm.

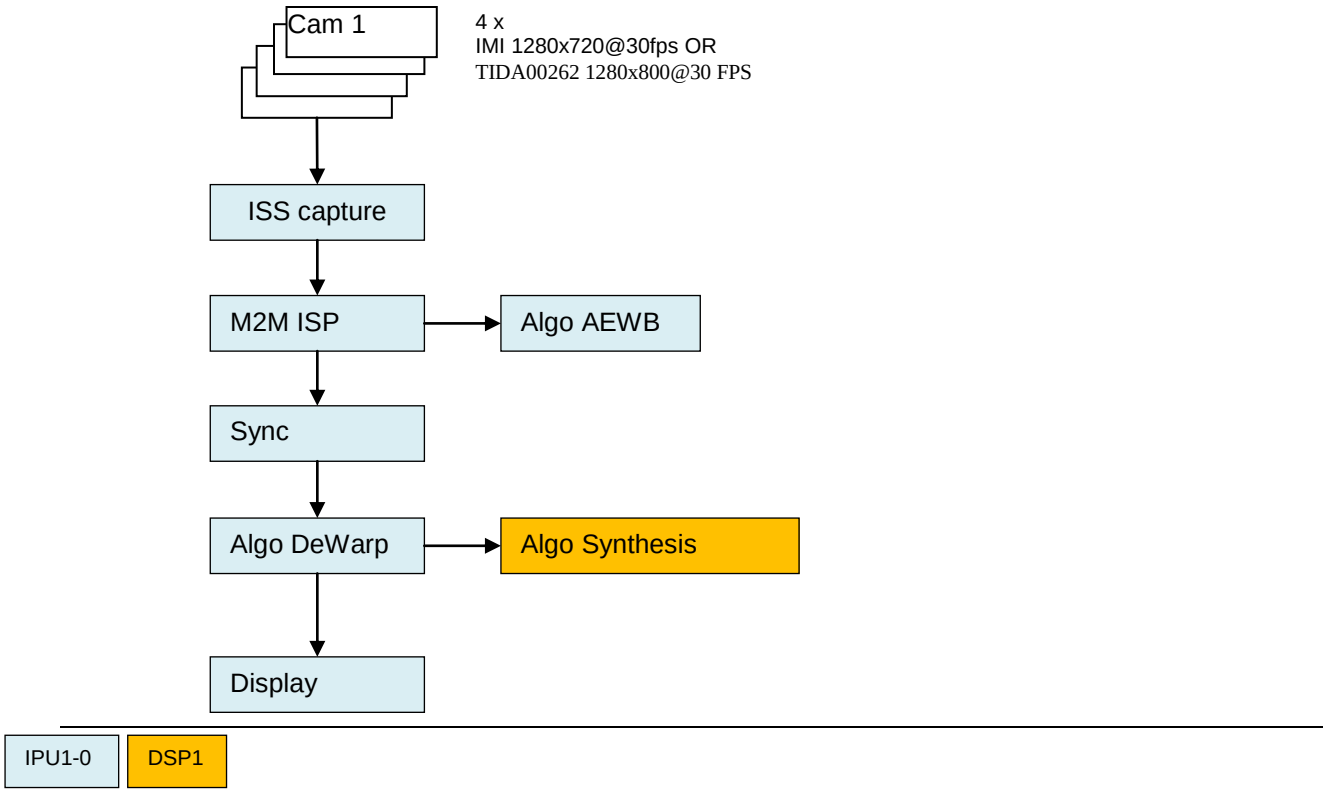
The DeWarp algorithm will use application provided (media thread) configuration and project 3D world points onto 2D plane and provide video frames for all channels to synthesis link. 3D world points are provided by (media thread)

The synthesis algorithm receives 4 channels of video and stiches them to provide a surround view.

Media Thread is used to read 3D world points (LDC LUTs) from mmc/sd card. In the boot up sequence, media thread reads LDC LUT for 1 view points and allows usecase creation to proceed and initiate read of remaining LDC LUTs while creation is in progress.

Once all the LDC LUTs are read from mmc/sd card, LDC LUTs are switched at capture frame rate to achieve smooth 3D transitions.

Please note in dataflow diagram below IPC IN/OUT blocks are left-out to improve readability. Please assume these whenever CPU changes in the flow.



14.3 System Parameters (TDA3xx)

Refer to section 5.1 for common system parameters. In addition following are the additional parameters for this particular usecase

- Camera Module : IMI (OV10640 sensor 1280x720 @ 30 FPS)
- Display Resolution : 1920 X 1080 @ 60 FPS
- MMC/SD Card Used : Sandisk micro sd, HC 1, class 10, 8 GB.

14.4 CPU Loading and Task Info (TDA3xx)

14.4.1 Total CPU Load

CPU	LOAD TYPE	CPU LOAD
IPU1_0	**HWI**	5.9%
	SWI	0.7%
	Total	**30.6%**
DSP1	**HWI**	0.4%
	SWI	0.1%
	Total	**36.6%**
ISP		**64.5%**

14.4.2 Task Level Information and Task Level CPU Load

CPU	TASK NAME	TASK DESCRIPTION	CPU LOAD (%)
IPU1_0	ISS Capture	Capture frames from sensor on CSI2 of ISS port	0.4%
	ISS M2M ISP	ISP M2M Processing	6.9%
	SYNC (1 link)	Sync frames based on timestamp from multiple channels	0.6%
	Algorithm0	AEWB algorithm	3.6%
	Algorithm1		6.0%
	UNKNOWN	This is unaccounted CPU load after subtracting the individual task load from total CPU Load	1.4%
	IPC OUT	To send frame to another processor	0.5%
	IPC IN	To receive frames from another processor	0.3%
	Display	Display of video and GRPX frames	0.5%
	Stat Coll	Statistics Collector	2.6%
DSP1	IPC +PAlign+ Synthesis	All DSP1 Processing algorithms	35.8%
	UNKNOWN	This is unaccounted CPU load after subtracting the individual task load from total CPU Load	0.1%

*NOTE: On DSP and similarly on EVE all links run in a single thread.

NOTE: CPU load of 0.0% means the CPU load was so low it could not be measured with sufficient granularity in load caclulations

NOTE: There could be minor variations of +/-0.1% CPU load in different runs of the same use-case

NOTE: Graphics load is not accounted for in these measurements

NOTE: Other than above tasks few additional tasks as listed below are active in each processor

- Message Q task: This task is used to listen to control messages sent by any other core. Normally at run-time very few control messages are sent hence this task does not appear in the task load print log
- Processor link task: This task is used to send generic non-link specific messages to another CPU. Normally at run-time very few messages are sent to this task hence this task does not appear in the task load print log
- Remote log client task (on IPU1-0 only): This task looks at the shared remote log buffer and outputs any strings to UART terminal. Normally during run-time prints are not done hence this task does not appear in the task load log

14.5 System Performance (TDA3xx)

COMPONENT	PARAMETER	SRV 5CH FOR *Capture to Display1 path ONLY*
ISS Capture	Output fps	30fps each on 4 Channels for SV
ISS M2M ISP	Output fps	30fps each on 4 Channels for SV
	Avg time per a frame	5.37ms
AEWB	Output Fps	30fps
	Avg time per a frame	7.3ms
DeWarp	Output Fps	30fps
	Avg time per a frame	10.8ms
ALG Synthesis (DSP1)	Output fps	30fps
	Avg time per frame	10.7ms
Display VID 1 (1080P@60)	Input fps	30fps
	VENC fps	60fps

NOTE: FPS numbers are rounded off to nearest integer
NOTE: The above figures are for HDMI display.

14.5.1 Code/Data Memory Usage

Refer section 5.2 for common Code/Data Memory usage

14.5.2 Heap Memory Usage

CPU	MEMORY SECTION	MEMORY SIZE RESERVED	MEMORY SIZE USED
IPU1-0	Local Heap	256 KB	111 KB
	HDVPSS Descriptor Mem	256 KB	36 KB
DSP1	L2	221 KB	128 KB
	Local Heap	512 KB	5 KB
Shared Memory	Frame Buffer (SR1)	351 MB	238 MB
	SR2 OCMC	0KB	0KB
	Remote Log Buffer	160 KB	158 KB

14.6 Other Benchmarks (TDA3xx)

14.6.1 Processing Latency

		LATENCY
Capture to Display Latency (Display VID 1)(SV)	Avg	46.2ms
	Min	44.9ms
	Max	49.1ms

NOTE:

- This latency is as measured inside the system by software.
- There will an additional 1 / (capture rate) added on top of this from sensor/receiver itself.

- There will an additional 1 / (display rate) added on top of this for the frame to actually get displayed on the screen.
- Thus e.g. in a scenario of display at 60fps and capture at 30fps - 16.67ms + 33.33ms needs to be added to latency figures in above table to get true capture to display latency

14.6.2 DDR Bandwidth

PARAMETER	BANDWIDTH	
EMIF Read + Write	Avg	1531 MB/s
	Peak	1988 MB/s

14.6.3 Boot Time

PARAMETER	VALUE
Use-case create start to live preview on display	6.04s
3D Transitions start (90 view points)	12.8s

Boot time measurement done with TDA3x ES2.0 samples.

14.6.4 Capture to Display Latency

The capture to display (Glass to Glass) latency for 3D Surround view is measured to be **110 msec**.

14.6.5 3D Surround View Fast Boot Use Case on TDA3x:

This use case is same as 3D Surround View use case with the speeded up boot sequence. Pl. refer to the VisionSDK_UserGuide_TDA3xx.pdf for steps to build for 3D Surround view fast boot.

Below are the boot times (EVM power ON to the first display frame queued) under different boot modes:

- **QSPI_SD : 5.3 seconds**
- **QSPI : 2.40 seconds**

14.6.6 Memory requirement per '*view point*' of 3D Surround View use case:

The 3D Surround View shows multiple view points of the stitched Surround View, and every view point uses the following data and LUTs which are stored into MMC/SD card or QSPI. The view point data and LUTs are read into DDR buffers at the beginning of the 3D surround view use case. The number of viewpoints that can be supported depends on the amount of DDR memory available to hold the view point data and LUTs.

DATA TYPE	SIZE
View point header (view point parameters)	1 KB
Car Image	200 KB
LDC LUTs	350 KB
Synthesis Blend Table	1 byte per surround view output pixel = 758016 bytes for (752 x 1008) output.
TOTAL	**~1300 KB per view point**

14.6.7 LZ4 Compression & Decompression Performance Data:

Decompression of LUTs (4 x LDC LUT + Blend Table)			
No. of View Points	**Compressed Size***	**Decompressed Size***	**Time(ms)**
1	114939	1766400	15
29	3366662	51225600	471
30	3524676	52992000	503

Compression of LUTs (4 x LDC LUT + Blend Table)			
No. of View Points	**Decompressed Size***	**Compressed Size***	**Time(ms)**
1	1116928	112381	52
29	32390912	3290440	1498
30	33507840	3436973	1565

Note:

Running on DSP CLK = 500.0MHz
*datasize in bytes

15 Fast boot ISS Capture + Object Detect + Display

15.1 Over view

This usecase demonstrates fast boot feature that can be applied for any usecase in vision_sdk. This section mentions performance numbers achieved for fast boot usecase from the boot time split perspective.

15.2 Dataflow

The usecase dataflow same as the object detect data flow motioned in section 11.2

More details about boot time optimization techniques can be found in VisionSDK_DevelopmentGuide.pdf

15.3 Usecase configuration for boot timer measurement

Please note following build configuration parameters for boot time measurement.

```
#
# Build Config is [ tda3xx_evm_bios_all ]
# Build Config file is @
/adasuser/surya/PDK/vision_sdk/configs/tda3xx_evm_bios_all/cfg.mk
# Build Config .h file is @
/adasuser/surya/PDK/vision_sdk/links_fw/include/config/apps/tda3xx_evm_bios_all/system
_cfg.h
# Build CPUs is @ all
#
# CPUs included in application,
# PROC_IPU1_0_INCLUDE=yes
# PROC_IPU1_1_INCLUDE=no
# PROC_IPU2_INCLUDE=no
# PROC_DSP1_INCLUDE=yes
# PROC_DSP2_INCLUDE=no
# PROC_EVE1_INCLUDE=yes
# PROC_EVE2_INCLUDE=no
# PROC_EVE3_INCLUDE=no
# PROC_EVE4_INCLUDE=no
# PROC_A15_0_INCLUDE=no
#
# Platform config,
# VSDK_BOARD_TYPE=TDA3XX_EVM [options: TDA2XX_EVM TDA2EX_EVM TDA3XX_EVM
TDA3XX_RVP]
# PLATFORM=tda3xx-evm
# DUAL_A15_SMP_BIOS=no
# DDR_MEM=DDR_MEM_512M [options: DDR_MEM_128M DDR_MEM_512M
DDR_MEM_1024M]
# NDK_PROC_TO_USE=none [options: a15_0 ipu1_0 ipu1_1 ipu2 none]
# NSP_TFDTP_INCLUDE=no [options: yes no]
# FATFS_PROC_TO_USE=ipu1_0 [options: ipu1_0 none]
# RADAR_BOARD=none [options: TDA3XX_AR12_ALPS TDA3XX_AR12_VIB_DAB_BOOSTER
TDA3XX_RADAR_RVP none]
#
# Build config,
# BUILD_OS=Linux [options: Windows_NT Linux]
# BUILD_DEPENDENCY_ALWAYS=no
```

```
# BUILD_ALGORITHMS=no
# BUILD_INFOADAS=no
# PROFILE=release [options: debug release]
# KW_BUILD=no
# CPLUSPLUS_BUILD=no
# IPU_PRIMARY_CORE=ipu1_0 [options: ipu1_0 ipu2]
# IPU_SECONDARY_CORE=ipu2 [options: ipu1_0 ipu2]
# A15_TARGET_OS=Bios [options: Bios Linux Qnx]
# BSP_STW_PACKAGE_SELECT=all [options: all vps-iss-dss-only vps-vip-vpe]
#
# Safety Module config,
# RTI_INCLUDE=no
# ECC_FFI_INCLUDE=no
# DCC_ESM_INCLUDE=no
#
# Video Module config,
# IVAHD_INCLUDE=no
# VPE_INCLUDE=no
# CAL_INCLUDE=yes
# ISS_INCLUDE=yes
# ISS_ENABLE_DEBUG_TAPS=no
# WDR_LDC_INCLUDE=yes
# DSS_INCLUDE=yes
#
# Open Compute config,
# OPENCL_INCLUDE=no
# TARGET_ROOTDIR=/adasuser/surya/PDK/vision_sdk/apps/src/rtos/opencl
# ENABLE_OPENCV=no
# ENABLE_OPENCV_TESTS=no
# OPENVX_INCLUDE=no
#
# Log config,
# ENABLE_UART_LOG=yes
# ENABLE_NETWORK_LOG=no
# ENABLE_CCS_LOG=no
# CIO_REDIRECT=yes
#
# IPC config,
# WORKQ_INCLUDE=no
# IPC_LIB_INCLUDE=no
#
# Surround View config,
# SRV_FAST_BOOT_INCLUDE=no
#
# Other Module config,
# AVB_INCLUDE=no
# DCAN_INCLUDE=no
# RADAR_INCLUDE=no
# CPU_IDLE_ENABLED=yes
# FAST_BOOT_INCLUDE=yes
# DATA_VIS_INCLUDE=no
# HS_DEVICE=no
# ULTRASONIC_INCLUDE=no
```

```
#
# Linux config,
# DEFAULT_UBOOT_CONFIG=dra7xx_evm_vision_config
# DEFAULT_KERNEL_CONFIG=omap2plus_defconfig
# DEFAULT_DTB=dra7-evm-infoadas.dtb
# CMEM_INCLUDE=no
# IPUMM_INCLUDE=no
# IPU1_EVELOADER_INCLUDE=no
# ROBUST_RVC_INCLUDE=no
# BUILD_ADAM_CAR=no
#
# Alg plugins included in build,
# ALG_autocalibration ALG_autoremap ALG_census ALG_clr ALG_crc ALG_denseopticalflow
ALG_deWarp ALG_disparityhamdist ALG_dmaSwMs ALG_edgedetection ALG_framecopy
ALG_lanedetection ALG_objectdetection ALG_remapmerge ALG_safe_framecopy
ALG_sceneobstruction ALG_sfm ALG_sparseopticalflow ALG_stereo_postprocessing
ALG_subframecopy ALG_surroundview ALG_stereo_app ALG_openvx ALG_iss_aewb
#
# Use-cases included in build,
# UC_fast_boot_iss_capture_isp_simcop_pd_display UC_iss_capture_isp_simcop_display
UC_iss_mult_capture_isp_2d_3d_sv_tda3x UC_iss_mult_capture_isp_dewarp_3dsv_tda3xx
UC_iss_mult_capture_isp_dewarp_3dsv_rearview_tda3xx
UC_iss_mult_capture_isp_dewarp_stereo_tda3xx
UC_iss_mult_capture_isp_dewarp_stereoplus_tda3xx
UC_iss_mult_capture_isp_simcop_stereo_tda3xx
UC_iss_mult_capture_isp_simcop_sv_tda3xx
UC_iss_mult_capture_isp_stereo_autocalib_tda3xx UC_srv_calibration
UC_lvds_vip_multi_cam_view_tda3xx UC_lvds_vip_sv_tda3xx UC_saveDisFrame
UC_vip_single_cam_analytics2 UC_vip_single_cam_dense_optical_flow
UC_vip_single_cam_edge_detection UC_vip_single_cam_frame_copy
UC_vip_single_cam_frame_copy_safety UC_vip_single_cam_lane_detection
UC_vip_single_cam_object_detection2 UC_vip_single_cam_sfm
UC_vip_single_cam_sparse_optical_flow UC_vip_single_cam_subframe_copy
UC_vip_single_cam_tlr UC_vip_single_cam_view UC_vip_single_cam_view_dsswb
UC_vip_single_cam_display_metadata UC_csi2_cal_multi_cam_view
UC_csi2_cal_sv_standalone UC_vip_single_cam_openvx
#
#
# CPUs that are NOT required but included in config [ tda3xx_evm_bios_all ],
#
# WARNING: IPU1_1 can be excluded from application
#
# CPUs that are required but not included in config [ tda3xx_evm_bios_all ],
#
#
# Edit /adasuser/surya/PDK/vision_sdk/build/configs/tda3xx_evm_bios_all/cfg.mk to
include or exclude CPUs in an application
#
```

Binary size:
AppImage_UcEarly_BE – 8.12MB
AppImage_UcLate_BE - 7.63MB
Boot media – QSPI
Capture – AR140P
Display – LCD (10 inch)
Algorithm – Object Detect

15.4 Boot time

15.4.1 POR to Display time split

No.	Description	Time
1.	SBL	324 ms
2.	Sensor initialization time with I2C 400 KHz	190 ms
3.	Time take by Framework	269 ms
	Power On Reset to Display Time	**783 ms**

As far as boot time is considered POR on to reset split is important which is mentioned above. If carefully observed measure time is spent in sensor initialization.

This can be further reduced by programming resister only needed, thus by reducing I2C read writes.

Overall vision_sdk takes 324 + 269 = **593 ms** only for capture + display usecase

15.4.2 POR to Object Detect

No.	Description	Time
1.	Power On to reset to Object Detect	**1894 ms**

This is the time when full Object Detect Usecase is functional since POR.

15.5 System Parameters (TDA3xx)

Refer to section 5.1 for common system parameters.

The benchmarks in this section are computed with AR140P sensor and LCD10inch display (1080p60).

15.6 CPU Loading and Task Info (TDA3xx)

15.6.1 Total CPU Load

CPU	LOAD TYPE	CPU LOAD	LOW POWER
IPU1_0	**HWI**	3.4%	**1.7%**
	SWI	0.7%	
	Total	**28.5%**	
DSP1	**HWI**	0.4%	**69.0%**
	SWI	0.1%	
	Total	**30.2%**	
EVE1	**HWI**	0.7%	**21.1%**
	SWI	0.2%	
	Total	**76.7%**	

15.6.2 Task Level Information and Task Level CPU Load

CPU	TASK NAME	TASK DESCRIPTION	CPU LOAD (%)
IPU1_0	ISS Capture	Capture frames from sensor on CSI2 of ISS port	0.2%
	ISS M2M ISP	ISP M2M Processing	3.3%
	SYNC (1 link)	Sync frames based on timestamp from multiple channels	0.7%
	Merge (2 links)	Merge frames from multiple channels	0.5%
	Algorithm0	AEWB algorithm	5.8%
	Algorithm1		3.3%
	UNKNOWN	This is unaccounted CPU load after subtracting the individual task load from total CPU Load	1.6%
	IPC OUT	To send frame to another processor	0.5%
	IPC IN	To receive frames from another processor	0.3%
	Display	Display of video and GRPX frames	0.8%
	Stat Coll	Statistics Collector	2.0%
DSP1	IPC +PAlign+Synthesis	All DSP1 Processing algorithms	29.4%
	UNKNOWN	This is unaccounted CPU load after subtracting the individual task load from total CPU Load	0.3%
EVE1	IPC + Algorthim	All EVE1 Processing algorithms	75.5%
	UNKNOWN	This is unaccounted CPU load after subtracting the individual task load from total CPU Load	0.3%

*NOTE: On DSP and similarly on EVE all links run in a single thread.

NOTE: CPU load of 0.0% means the CPU load was so low it could not be measured with sufficient granularity in load caclulations

NOTE: There could be minor variations of +/-0.1% CPU load in different runs of the same use-case

NOTE: Graphics load is not accounted for in these measurements

NOTE: Other than above tasks few additional tasks as listed below are active in each processor

- Message Q task: This task is used to listen to control messages sent by any other core. Normally at run-time very few control messages are sent hence this task does not appear in the task load print log

- Processor link task: This task is used to send generic non-link specific messages to another CPU. Normally at run-time very few messages are sent to this task hence this task does not appear in the task load print log
- Remote log client task (on IPU1-0 only): This task looks at the shared remote log buffer and outputs any strings to UART terminal. Normally during run-time prints are not done hence this task does not appear in the task load log

15.7 System Performance (TDA3xx)

COMPONENT	PARAMETER	SRV 5CH FOR *Capture to Display1 path ONLY*
ISS Capture	Output fps	30fps
ISS M2M ISP	Output fps	30fps
	Avg time per a frame	11.7ms
AEWB	Output Fps	30fps
	Avg time per a frame	2.12ms
ISS M2M SIMCOP	Output Fps	30fps
	Avg time per a frame	10.1ms
ISS Resizer	Output Fps	30fps
	Avg time per a frame	8.4ms
FP compute	Output fps	30fps
	Avg time per frame	24.7ms
Object detect	Output fps	30fps
	Avg time per frame	9.7ms
Object draw	Output fps	30fps
	Avg time per frame	1.3ms
Display VID 1 (720P@60)	Input fps	30fps
	VENC fps	60fps

NOTE: FPS numbers are rounded off to nearest integer
NOTE: The above figures are for HDMI display.

15.7.1 Code/Data Memory Usage

Refer section 5.2 for common Code/Data Memory usage

15.7.2 DDR Bandwidth

PARAMETER	BANDWIDTH	
EMIF Read + Write	Avg	1220 MB/s
	Peak	2302 MB/s

15.7.3 Heap Memory Usage

CPU	MEMORY SECTION	MEMORY SIZE RESERVED	MEMORY SIZE USED
IPU1-0	Local Heap	256 KB	103 KB
	HDVPSS Descriptor Mem	256 KB	36 KB
DSP1	L2	221 KB	208 KB
	Local Heap	512 KB	7 KB
Shared Memory	SR0	1MB	1MB
	Frame Buffer (SR1)	351 MB	43 MB
	SR2 OCMC	0KB	0KB
	Remote Log Buffer	160 KB	158 KB

16 Inter processor communication (IPC) latency

This section lists the latency measured when doing inter processor communication in Vision SDK

16.1 System Parameters (TDA2xx)

Refer to section 2.1 for common system parameters. The benchmarks in this section are computed for OV10635 capture (720p30) and LCD display scenario.

Other important system parameters are listed below

COMPONENT	PROPERTY	VALUE
IPC	Interrupt mechanism	Notify with SHM transport
	Information exchange mechanism	Non-Cache shared region in DDR (SR0)
Measurement mechanism	Timer used	CLK32KHZ
	Measurement unit	usecs
	Duration of Measurement	30 secs
	Number of frame exchanges over which results are averaged	30*30 = 900

16.2 IPC Latency measurements

In order to measure latency from all CPUs to all CPUs, three use-cases were run as shown below. The color in measurement table shows the use-case in which the IPC latency was measured.

Usecase 1	Capture(IPU1_0) ->IPU1_0->DSP1->EVE1->EVE2->DSP2->EVE3->A15_0->EVE4->IPU1_1->IPU1_0 -> Display(IPU1_0)
Usecase 2	Capture(IPU1_0) ->IPU1_0->A15_0->DSP1->DSP2->IPU1_1->EVE1->IPU1_0 -> Display(IPU1_0)
Usecase 3	Capture(IPU1_0) ->IPU1_0->DSP1->A15_0->IPU1_0 -> Display(IPU1_0)

16.2.1 IPC Buffer Passing Latency measurement (TDA2xx)

This measures the time taken from the point a new buffer is received by IPC OUT link on SRC CPU to the point in IPC IN link on DST CPU where the buffer is given to the next link in the processing chain.

Roughly this corresponds to the IPC Notify latency + the time taken to copy / translate buffer information from one CPU to another CPU via shared memory

The IPC buffer passing latency is shown below (All numbers in units of **micro-secs**)

DST \ SRC	A15	DSP	IPU	EVE
A15	NA	34	74	126
DSP	33	35	77	142
IPU	98	145	156	232
EVE	223	227	264	343

16.2.2 IPC Notify Latency Measurement (TDA2xx)

This measures the time taken from the point just before Notify_sendEvent() API is called on SRC CPU (in IPN OUT link) to the point (in IPC IN link) when SYSTEM_CMD_NEW_DATA command is received on DST CPU (NOTE: Notify callback (ISR) on DST CPU sends SYSTEM_CMD_NEW_DATA to IPC IN link on DST CPU).

Roughly this corresponds to IPC Notify send + Notify ISR + Task switch overhead.

The IPC Notify latency is shown below (All numbers in units of **micro-secs**)

DST \ SRC	A15	DSP	IPU	EVE
A15	NA	23	45	54
DSP	20	21	45	57
IPU	66	109	135	134
EVE	152	159	179	201

17 Revision History:

Version	Date	Revision History
1.00	1 Oct 2013	Updated for Vision SDK release v2.01
2.00	10 Mar 2014	Updated for Vision SDK release v2.02
2.01	27 Mar 2014	Add section on IPC latency measurement
2.02	4th April 2014	Added Multi-channel AVB Surround view, Edge Detect Use case
2.03	31st July 2014	Updated for Vision SDK release v2.03
2.04	14th Nov 2014	Updated for Vision SDK release v2.05 for TDA2x and TDA3x use cases
2.06	4th March 2015	Updated for Vision SDK release v2.06 for TDA2x and TDA3x, TDA2Ex, TDA2x-MC use cases
2.07	7th July 2015	Updated for Vision SDK release v2.07 for TDA2x and TDA3x, TDA2Ex, TDA2x-MC use cases
2.08	15th Oct 2015	Updated for Vision SDK release v2.08
2.09	21st Mar 2016	Updated for Vision SDK release v2.09 Perform Datasheet cleanup for below: Removed Sparse optical flow, object detect & lane detect usecase Merged Analytics usecase of TDA2x & 3x Merged Multi channel LVDS usecase of TDA2x & 2Ex Rename Multichannel surround view usecase of TDA 3x to 3D surround view usecase
2.10	7th July 2016	Updated for Vision SDK release v2.10 3D fast boot surround view readings are added
2.11	1st Nov 2016	Updated for Vision SDK release v2.11
2.12	6th Feb 2017	Updated for Vision SDK release v2.12
3.0	5th July 2017	Updated for Vision SDK release v3.0 Removed XCAM related data readings
3.1	16th Oct 2017	Updated for Vision SDK release v3.1
3.2	21st Dec 2017	Updated for Vision SDK release v3.2 TDA2Px system parameters are added
3.3	5th April 2018	Updated for Vision SDK release v3.3
3.4	2nd July 2018	Updated for Vision SDK release v3.4