PROCESSOR SDK Radar on RTOS (v03.05.00)

Data Sheet

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Table of Contents

1 Introduction

IMPORANT NOTE:

- This datasheet has performance and feature information about use-cases running on TDA3xx with AWR1243 sensor to capture and process Radar data.

1.1 Framework features

- Compile and build for all CPUs
  - TDA3xx system (IPU1-0, IPU1-1, DSP1, DSP2, EVE1).
  - TDA2xx system (IPU1-0, IPU1-1, DSP1, DSP2, EVE1/2/3/4).
- Debug and release build profiles.
- Single place to setup memory map
  - Default 128MB DDR TDA3xx
  - Default 512 MB DDR TDA2xx
- Ability to create and control links on any CPU.
- Remote log feature with ability to print logs from all CPUs to UART controlled by IPU1-0.
- CPU load profiling for all cores.
- Memory usage log for all cores.
- Run time use-cases performance statistics like frame-rate, latency, frame-drop.
- Exception handler log for IPU, EVE and DSP.
- EDMA support on all cores, wherever applicable
  - IPU uses system EDMA (via EDMA3LLD library)
  - DSP uses system EDMA or local EDMA (via EDMA3LLD library)
  - EVE uses local EDMA (via EDMA3LLD library and/or EVE SW library)
- Global timestamp to keep track of common time across all CPUs.
- Buffer allocation APIs for DDR, OCMC memory, L2 memory (DSP/EVE).
- Use-Case Auto Generation tool which generates C code for Processor SDK Radar use-cases from txt based config file.

1.2 Supported Links

No.	Links	TDA3xx
Framework Related Links		
1	VIP Capture	YES
2	Display	YES
3	Display controller	YES
4	IPC OUT/IN	YES
5	Dup	YES
6	Merge	YES
7	Sync	YES
8	Select	YES
9	Network Tx	YES
10	Network Rx Source	YES
11	ISS Capture	YES
12	ISS M2M ISP	YES
13	ISS M2M Simcop	YES
14	Gate	YES
Other Sample link's		
1	Graphics Source	YES
2	Network Ctrl	YES
Algorithm plugin's		
1	Alg plugin for Radar Processing	YES
Algorithm Functions		
1	Alg Fxn for Radar Frame Copy	YES
2	Alg Fxn for Radar Range and Doppler FFT	YES
3	Alg Fxn for drawing the Range and Doppler FFT output as a Heat Map	YES
4	Alg Fxn for Radar Peak Detection	YES
5	Alg Fxn for Radar Beam Forming	YES
6	Alg Fxn for drawing the Object Detection	YES
7	Alg Fxn for DSP based Radar Object Detection	YES
Work Queue		
1	Alg Fxn for FFT implemented with work queue	YES
2	Alg Fxn for Peak Detection implemented with	YES

No.	Links	TDA3xx
	work queue	
3	Alg Fxn for Beam Forming implemented with work queue	YES

2 TDA3xx + AWR12 Capture, Object Detection, Network Tx

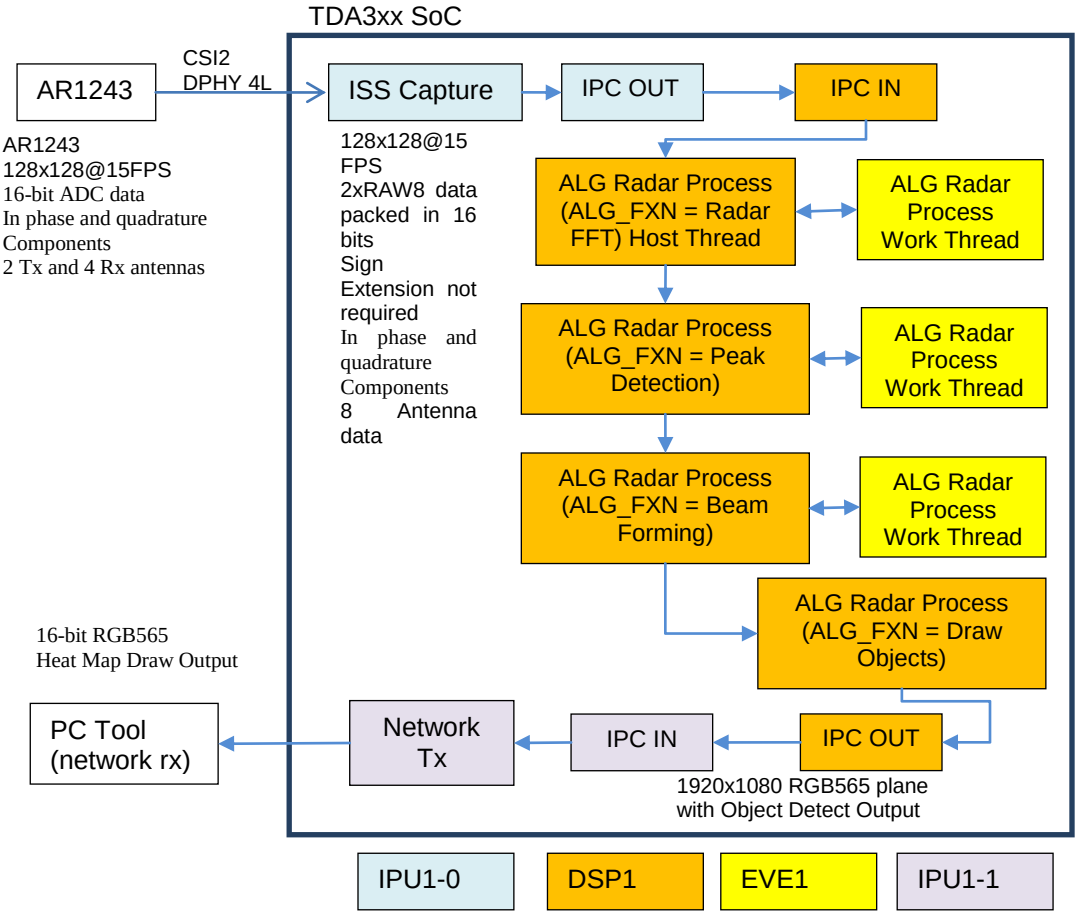
2.1 Overview

This use case consists of continuous capture of AWR12xx radar sensor data from CSI using the IPU as CSI2 host CPU for buffer management. This is followed by the Range and Doppler FFT computation of the input data corresponding to the N input antennae on the EVE. This is achieved using work queue infrastructure with the host thread on the DSP and the work thread on the EVE. The output of the 2D-FFT is passed through the peak detection and the beam forming stages in the EVE (again implemented via workQ). The detected objects are then plotted in a graph which indicates the range and the angle of the object. The color of the object indicates the relative velocity of the objects.

Capture is done for 128 samples per chirp and 128 chirps per frame @ 15 FPS 8 Antennae using the CSI2.

2.2 Data Flow

This usecase demonstrates the EVE object detection computation. The data flow below shows a radar data capture for a configuration of 128 samples per chirp and 128 chirps per frame @ 15 FPS for 4 Rx Antenna and 2 Tx Antenna.



2.3 System Parameters

Refer to section 5.1 for common system parameters.

The benchmarks in this section are computed for 128x128@15 FPS 8 Antenna radar data capture.

2.4 CPU Loading and Task Info

2.4.1 Total CPU Load

Note: The DSP Heat map visualization is a visual aid to interpret the FFT computation output drawn at a 3x3 pixel for each data sample magnitude. No DSP optimizations have been applied to the draw logic. Hence the CPU load for DSP can seem higher.

CPU	LOAD TYPE	CPU LOAD
IPU1-0	HWI	0.6%
	SWI	0.3%
	Total	**3.6%**
EVE1	HWI	0.4%
	SWI	0.1%
	Total	**6.5%**
DSP1	HWI	0.3%
	SWI	0.1%
	Total	**6.1%**
IPU1-1	HWI	3.2%
	SWI	0.6%
	Total	**30.7%**

2.4.2 Task Level Information and Task Level CPU Load

CPU	TASK NAME	TASK DESCRIPTION	CPU LOAD
IPU1-0	Stat Collector	Statistics collector	1.70%
	ISS Capture	Capture frames via CSI2	0.10%
	UNKNOWN	This is unaccounted CPU load after subtracting the individual task load from total CPU Load	0.90%
	IPC OUT	To send frame to another processor	0.20%
EVE1	ALG Range and Doppler FFT + Peak Detection + Beam Forming	Range and Doppler FFT + Peak Detection + Beam Forming	6.0%
	UNKNOWN	This is unaccounted CPU load after subtracting the individual task load from total CPU Load	0.10%
DSP1	*IPC + ALG Draw Objects + WorkQ Host Thread	Draw Objects + IPC + Forward processing request to EVE	5.70%
	UNKNOWN	This is unaccounted CPU load after subtracting the individual task load from total CPU Load	0.40%
IPU1-1	NETWORK TX	Network Tx Link reception of draw output and forward to network	0.40%
		To receive frame from DSP1	0.20%

	Networking and Miscellaneous	This takes into account the networking task and stack operation. This is with the network PC tool running. This includes unaccounted CPU load after subtracting the individual task load from total CPU Load.	26.30%

*NOTE: On DSP all links run in a single thread.

NOTE: CPU load of 0.0% means the CPU load was so low it could not be measured with sufficient granularity.

NOTE: There could be minor variations of +/-0.1% CPU load in different runs of the same use-case

NOTE: Other than above tasks few additional tasks as listed below are active in each processor

- Message Q task: This task is used to listen to control messages sent by any other core. Normally at run-time very few control messages are sent hence this task does not appear in the task load print log
- Processor link task: This task is used to send generic non-link specific messages to another CPU. Normally at run-time very few messages are sent to this task hence this task does not appear in the task load print log
- Remote log client task (on IPU1-1 and IPU1-0 only): This task looks at the shared remote log buffer and outputs any strings to Network console terminal. Normally during run-time prints are not done hence this task does not appear in the task load log

2.5 System Performance

COMPONENT	PARAMETER	CONFIG
ISS Capture	Output FPS	15
ALG Radar Process (ALG_FXN = Range and Doppler FFT) (EVE)	Output FPS	15
	Avg process time per frame	1.541 ms
ALG Radar Process (ALG_FXN = Peak Detection) (EVE)	Output FPS	15
	Avg process time per frame	1.181ms
ALG Radar Process (ALG_FXN = Beam Forming) (EVE)	Output FPS	15
	Avg process time per frame	0.268 ms
ALG Radar Process (ALG_FXN = Draw Objects) (DSP)	Output FPS	15
	Avg process time per frame	7.998 ms
Network Tx (Network)	Input FPS	15
	Output Transmit FPS*	15

NOTE: FPS numbers are rounded off to nearest integer
NOTE: The above benchmarks are computed for 128x128 @ 15 fps 8 Antenna capture and network transmit of 2D-FFT Object position (1080p60)
* NOTE: The output FPS from the NETWORK TX link is determined by the network throughput. With a Windows PC connected to a 1Gbps Ethernet switch we see the network bandwidth of ~550 Mbps to transmit RGB565 raw 1080p buffer output by the DSP at 15 FPS using TFDTP. When using TCP/IP the FPS of transmit of the raw frame is ~1.5 FPS.

2.6 System Memory Usage

2.6.1 Code/Data Memory Usage

Refer section 5.2 for common Code/Data Memory usage.

2.6.2 Heap Memory Usage

CPU	MEMORY SECTION	MEMORY SIZE RESERVED	MEMORY SIZE USED
IPU1-0	Local Heap	256 KB	5 KB
EVE1	L2	22 KB	12 KB
	Local Heap	256KB	2 KB
DSP1	L2	221KB	0 KB
	Local Heap	512 KB	87 KB
Shared Memory	SR1 Frame Buffer	74MB	49 MB
	SR Non-Cached	100KB	4.5 KB

2.7 Other Benchmarks

2.7.1 Processing Latency

		LATENCY
Capture to Network Tx Latency	Average	13.233 ms

NOTE:

- This latency is as measured inside the system by software.
- There will an additional 1/(capture rate) added on top of this from sensor/receiver itself.

2.7.2 Boot Time

SL NO.	PARAMETER		VALUE
1	SBL to App main() (QSPI Boot) The boot time will change based on the mode of boot – SD, NOR flash or QSPI.		0.37 s
2	main() to Use-case menu		1.15 s
3	Network Initialization		4.94 s
4	Use-case create start to output		0.35 s
4	a	AWR1243 Reset and Boot time	0.22 s
4	b	AWR1243 Firmware Load Time (Pre-flashed)	0 s
4	c	AWR1243 Configuration Time	0.015 s
4	d	Other Links Start and Create	0.115 s
5	**Total Boot time**		**6.81 s**

2.7.3 AWR12 Firmware Flash Time

The time taken to erase the AWR12 flash and program the MSS and BSS firmware is as below:

Sl. No.	Action	Size	Time
1.	Erase Flash	4MB	11.82 s
2.	Flash the BSS Firmware	193 KB	41.32 s
3.	Flash the MSS Firmware	97 KB	21.03 s
4.	Flash the Configuration Structure	164 B	0.41 s

3 TDA3x EVM + AWR12 Capture, Object Detect, display

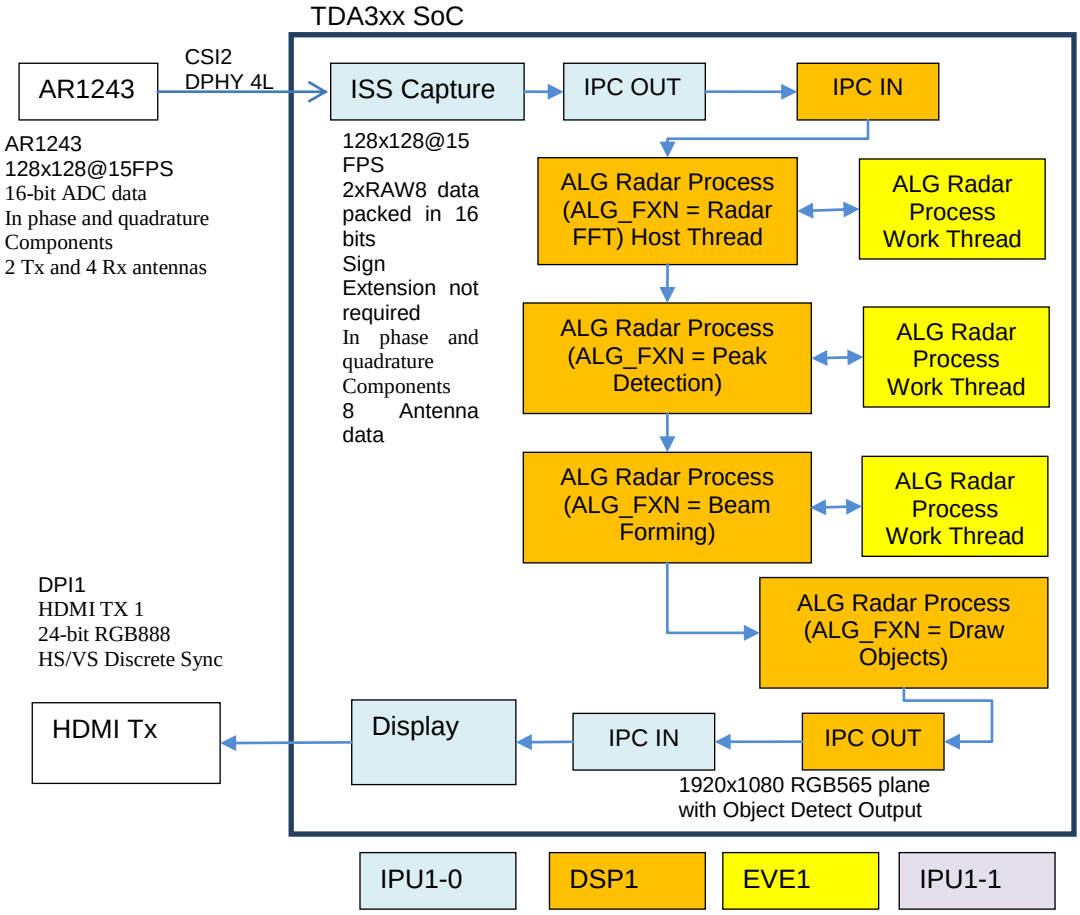
3.1 Overview

This use case consists of continuous capture of AWR12xx radar sensor data from CSI using the IPU as CSI2 host CPU for buffer management. This is followed by the Range and Doppler FFT computation of the input data corresponding to the N input antennae on the EVE. This is achieved using work queue infrastructure with the host thread on the DSP and the work thread on the EVE. The output of the 2D-FFT is passed through the peak detection and the beam forming stages in the EVE (again implemented via workQ). The detected objects are then plotted in a graph which indicates the range and the angle of the object. The color of the object indicates the relative velocity of the objects.

Capture is done for 128 samples per chirp and 128 chirps per frame @ 15 FPS 8 Antennae using the CSI2. Display is used to show the percentage loading of all the CPUs in the TDA device and the 2D-FFT heat map to show detected objects.

3.2 Data Flow

This usecase demonstrates the EVE FFT computation in the range and Doppler dimensions. The data flow below shows a radar data capture for a configuration of 128 samples per chirp and 128 chirps per frame @ 15 FPS for 4 Rx Antenna and 2 Tx Antenna.



3.3 System Parameters

Refer to section 5.1 for common system parameters.

The benchmarks in this section are computed for 128x128@15 FPS 8 Antenna radar data capture.

3.4 CPU Loading and Task Info

3.4.1 Total CPU Load

Note: The DSP Heat map visualization is a visual aid to interpret the FFT computation output drawn at a 3x3 pixel for each data sample magnitude. No DSP optimizations have been applied to the draw logic. Hence the CPU load for DSP can seem higher.

CPU	LOAD TYPE	CPU LOAD
IPU1-0	HWI	1.2%
	SWI	0.4%
	Total	**7.4%**
EVE1	HWI	0.5%
	SWI	0.2%
	Total	**5.1%**
DSP1	HWI	0.3%
	SWI	0.1%
	Total	**5.2%**

3.4.2 Task Level Information and Task Level CPU Load

CPU	TASK NAME	TASK DESCRIPTION	CPU LOAD
IPU1-0	Stat Collector	Statistics collector	1.6%
	ISS Capture	Capture frames via CSI2	0.1%
	Graphics	Graphics update for the CPU load	2.7%
	Display	Display Objects	0.2%
	UNKNOWN	This is unaccounted CPU load after subtracting the individual task load from total CPU Load	2.5%
	IPC OUT	To send frame to another processor	0.2%
	IPC IN	To receive frames from another processor	0.1%
EVE1	ALG 2D FFT + Peak detection + beam forming	2D FFT + Peak detection + beam forming Work Thread	4.4%
	UNKNOWN	This is unaccounted CPU load after subtracting the individual task load from total CPU Load	0.7%

CPU	TASK NAME	TASK DESCRIPTION	CPU LOAD
DSP1	*IPC + ALG Draw + FFT WorkQ Host Thread	Draw Object + IPC + Forward processing request to EVE	4.8%
	UNKNOWN	This is unaccounted CPU load after subtracting the individual task load from total CPU Load	0.4%

*NOTE: On DSP all links run in a single thread.

NOTE: CPU load of 0.0% means the CPU load was so low it could not be measured with sufficient granularity.

NOTE: There could be minor variations of +/-0.1% CPU load in different runs of the same use-case

NOTE: Other than above tasks few additional tasks as listed below are active in each processor

- Message Q task: This task is used to listen to control messages sent by any other core. Normally at run-time very few control messages are sent hence this task does not appear in the task load print log
- Processor link task: This task is used to send generic non-link specific messages to another CPU. Normally at run-time very few messages are sent to this task hence this task does not appear in the task load print log
- Remote log client task (on IPU1-0 only): This task looks at the shared remote log buffer and outputs any strings to UART terminal. Normally during run-time prints are not done hence this task does not appear in the task load log

3.5 System Performance

COMPONENT	PARAMETER	CONFIG
ISS Capture	Output FPS	15
ALG Radar Process (ALG_FXN = Range and Doppler FFT) (EVE)	Output FPS	15
	Avg process time per frame	1.572 ms
ALG Radar Process (ALG_FXN = Peak Detection) (EVE)	Output FPS	15
	Avg process time per frame	1.257 ms
ALG Radar Process (ALG_FXN = Beam Forming) (EVE)	Output FPS	15
	Avg process time per frame	0.28 ms
ALG Radar Process (ALG_FXN = Draw Objects) (DSP)	Output FPS	15
	Avg process time per frame	9.34 ms
Display	Input FPS	15
	VENC FPS	60

NOTE: FPS numbers are rounded off to nearest integer
NOTE: The above benchmarks are computed for 128x128 @ 15 fps 8 Antenna capture and HDMI display of graph with detected objects (1080p60)

3.6 System Memory Usage

3.6.1 Code/Data Memory Usage

Refer section 5.2 for common Code/Data Memory usage.

3.6.2 Heap Memory Usage

CPU	MEMORY SECTION	MEMORY SIZE RESERVED	MEMORY SIZE USED
IPU1-0	Local Heap	256 KB	5 KB
EVE1	L2	22 KB	12 KB
	Local Heap	256KB	2 KB
DSP1	L2	221KB	0 KB
	Local Heap	512 KB	87 KB
Shared Memory	SR1 Frame Buffer	74MB	51 MB
	SR Non-Cached	94KB	4.5 KB

3.7 Other Benchmarks

3.7.1 Processing Latency

		LATENCY
Capture to Display Latency	Avg	13.088 ms

NOTE:

- This latency is as measured inside the system by software.
- There will an additional 1/(capture rate) added on top of this from sensor/receiver itself.

3.7.2 Boot Time

SL NO.	PARAMETER		VALUE
1	SBL to App main() (QSPI Boot) The boot time will change based on the mode of boot – SD, NOR flash or QSPI.		0.36 s
2	main() to Use-case create		1.14 s
3	Use-case create start to display		4.16 s
3	a	AWR1243 Reset and Boot time	0.35 s
3	b	AWR1243 Firmware Load Time	0.22 s
3	c	AWR1243 Configuration Time	1.84 s
3	d	GRPX Link Create Time	1.55 s
3	e	Other Links Start and Create	0.2 s
4	**Total Boot time**		**5.66 s**

4 TDA2x EVM + 4 AWR12 Cascade Capture, Object Detect, display

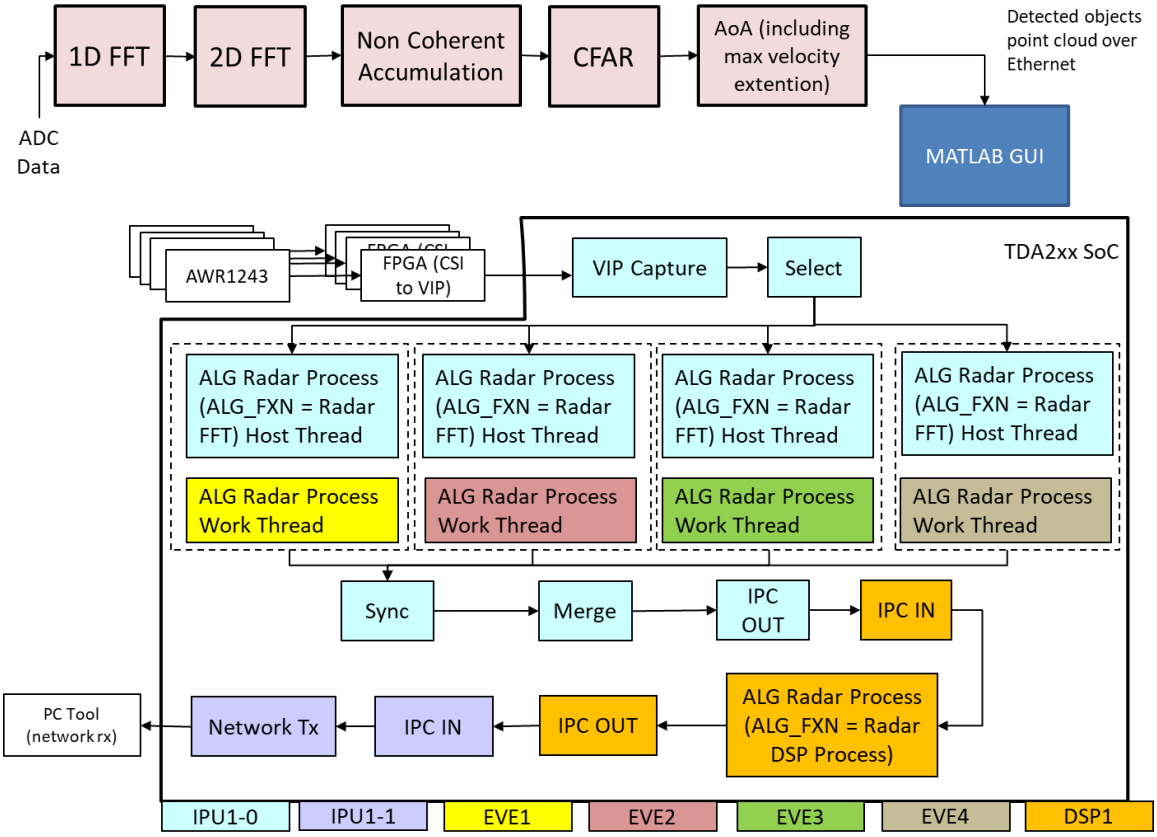
4.1 Overview

This use case consists of continuous capture of 4 chip cascade AWR12xx radar sensor data from VIP using the IPU for buffer management. This is followed by the Range FFT computation of the input data corresponding to the N input antennae on the EVE. This is achieved using work queue infrastructure with the host thread on the IPU and the work thread on each of the 4 EVEs. The output of the 1D-FFT is passed through 2D FFT, peak detection and the beam forming stages in the DSP. The detected objects are then sent out via Ethernet to be displayed using a Matlab script.

Capture is done for 256 samples per chirp and 64 chirps per frame @ 15 FPS 16 Rx antenna (4 Rx per sensor) and 8 Tx Antennae using the VIP2.

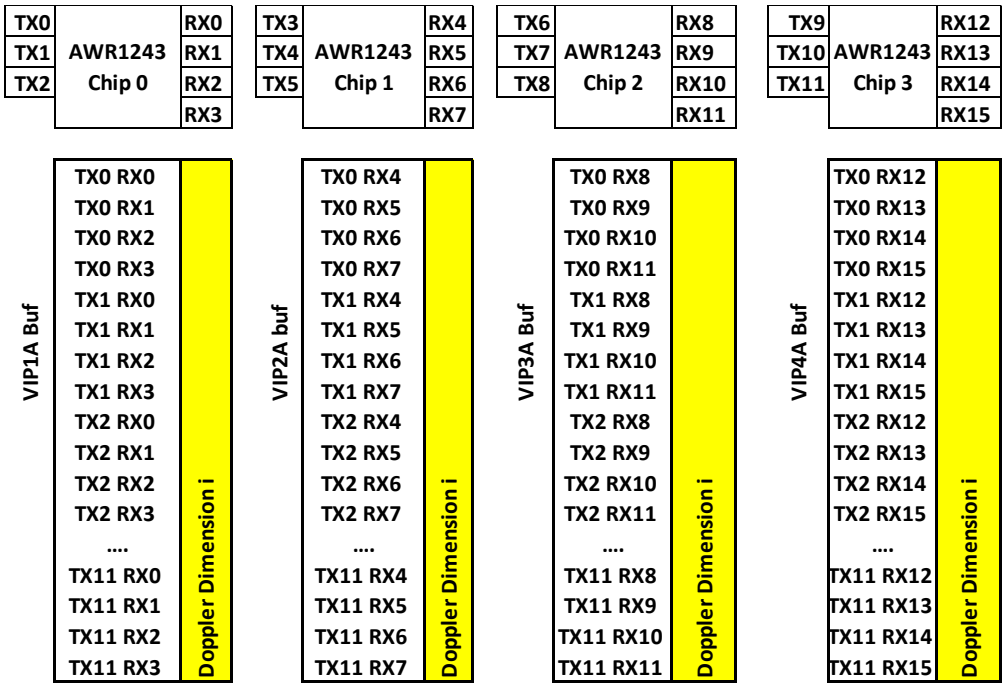
4.2 Data Flow

The overall usecase processing is as shown below:

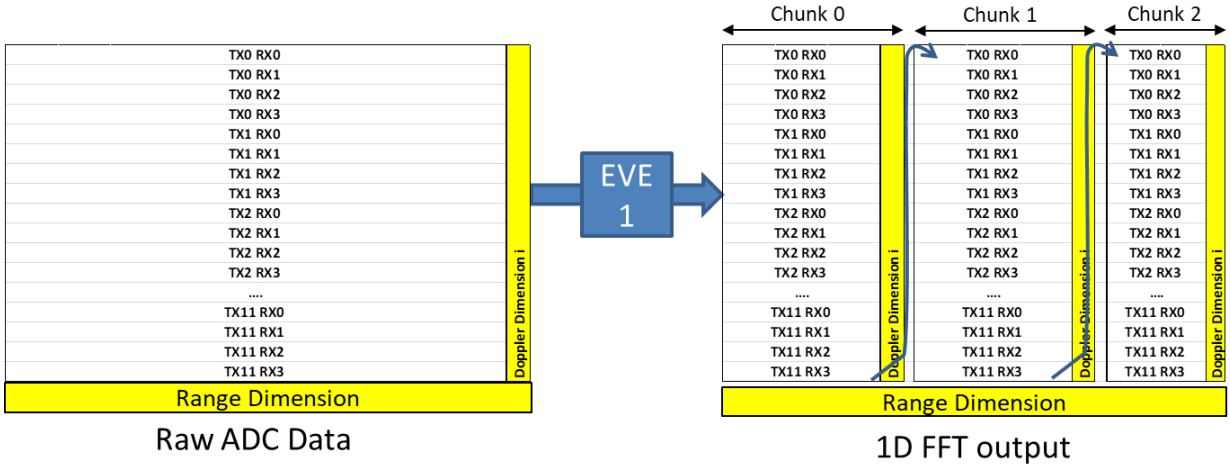


The data from the AWR1243 sensors is sent out through the CSI interface. An FPGA (LIFMD-6000) is used to convert the CSI stream to a parallel 16 bit VIP using VSYNC and ACTVID based capture. The FPGA image is capable of capturing data rates of 600 Mbps 4 Lane and 300 Mbps 4 Lane.

Once the raw ADC data is captured, the data in the DDR is as shown below. Note the chirps are captured in non-interleaved format. So every row Tx_nRx_m shown below has 16 bit I and 16 bit Q data for all the ADC samples in a given frame. The width of the frame is given by the 4 Bytes x Range Dimension x Num Rx Antenna per sensor. The height of the frame is Num of TDMA Tx antenna x Doppler Dimension.



The output of each EVE 1D FFT output in DDR is as shown below:



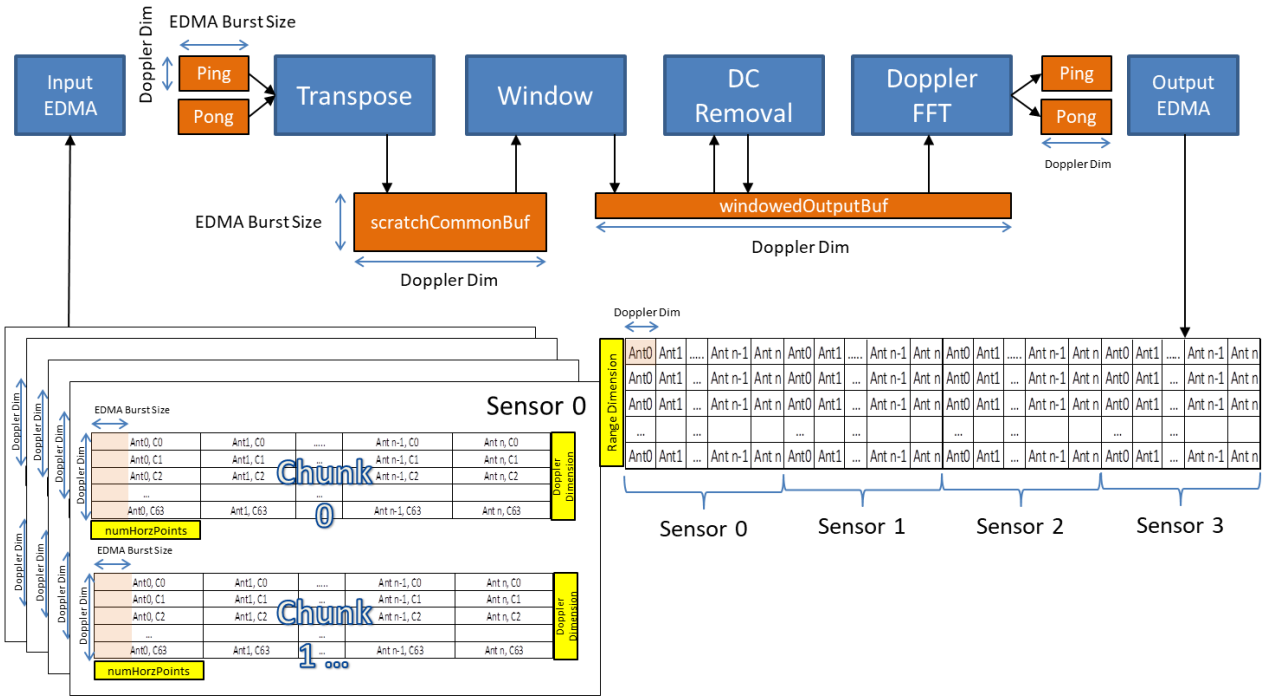
Each chunk of the EVE FFT output can be visualized as below where each Tx_nRx_m pair creating a virtual Antenna (Ant).

Chunk 0:

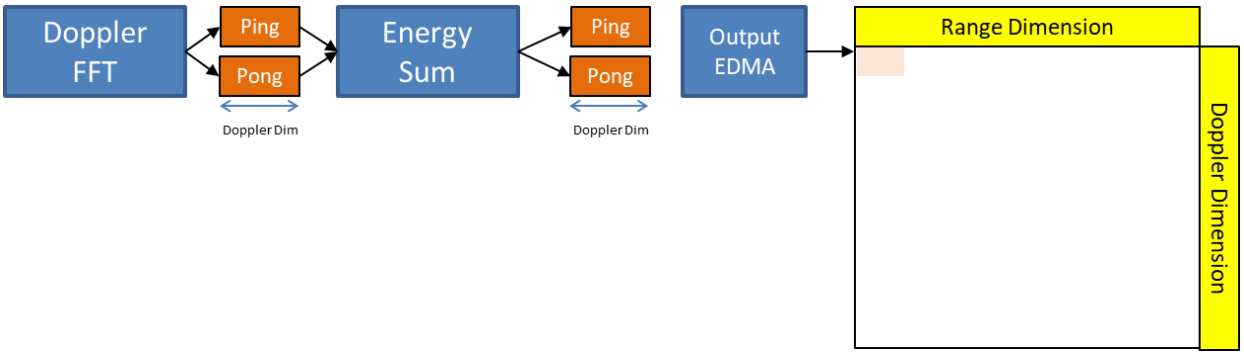
Ant0, C0	Ant1, C0	.....	Ant n-1, C0	Ant n, C0	Doppler Dimension
Ant0, C1	Ant1, C1	...	Ant n-1, C1	Ant n, C1	
Ant0, C2	Ant1, C2	...	Ant n-1, C2	Ant n, C2	
...		...			
Ant0, C63	Ant1, C63	...	Ant n-1, C63	Ant n, C63	
numHorzPoints					

Once the data output from all 4 EVEs corresponding to each sensor is received the sync link is used to synchronize and share all the 4 buffers to DSP for the further processing.

The first stage in the DSP processing is 2D 32 bit FFT. The Orange boxes in the figures below correspond to buffers in the DSP L2 RAM.

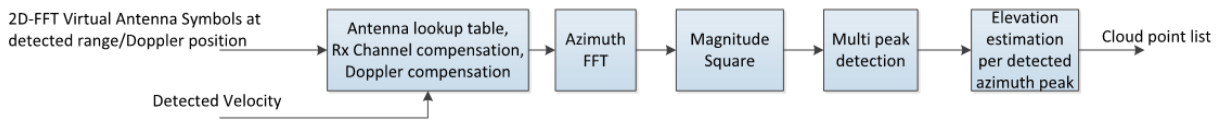


This is followed by an energy sum calculation which non-coherently adds up the FFT magnitude. The buffer which is generated out of this non-coherent accumulation is written out to DDR.

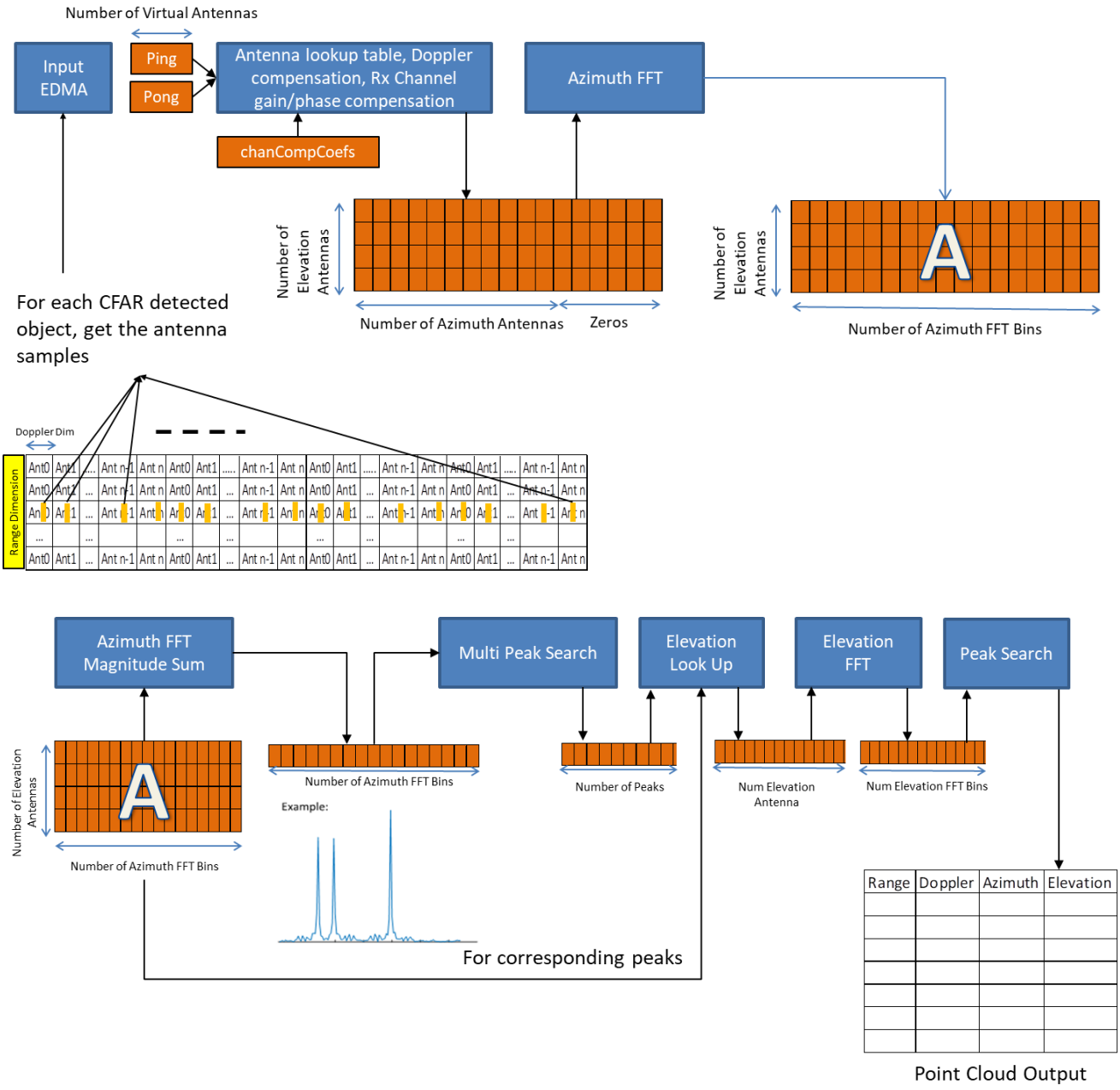


The energy sum output is passed through the peak detection CFAR algorithm which gives the final detected points.

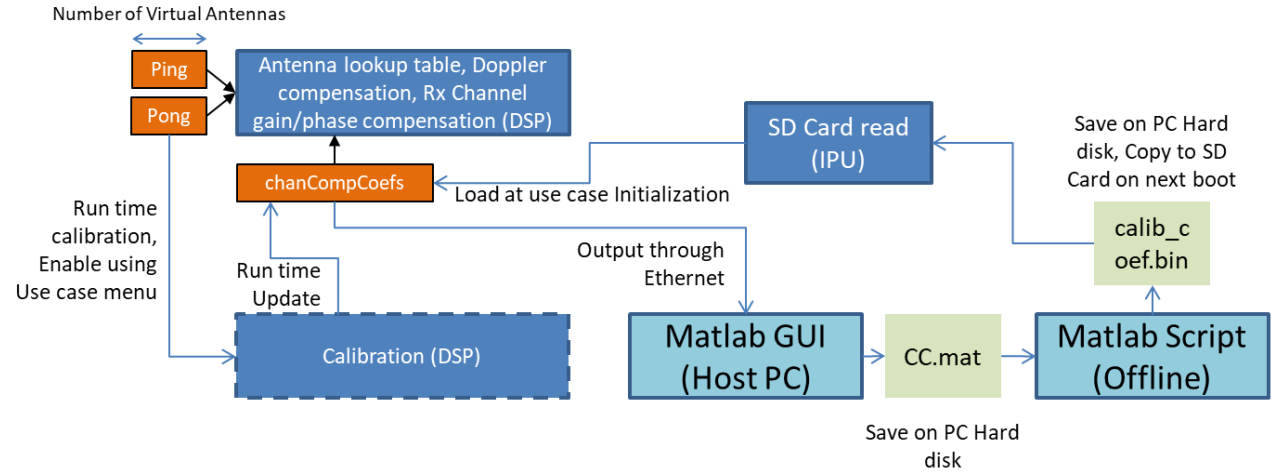
The next stage of the processing chain is the Angle of arrival estimation. Based on the CFAR detected objects the antenna data is extracted from DDR and then after Doppler compensation and gain and phase compensation the azimuth FFT is performed. The top level simplified flow is as show below:



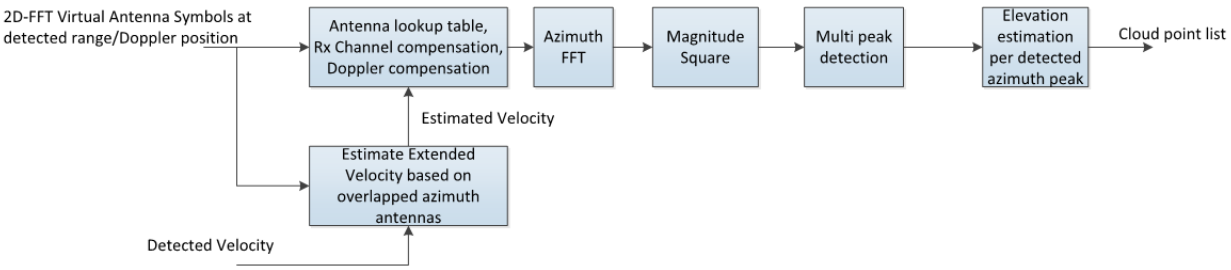
A more detailed flow of data in the angle of arrival (AoA) computation is as show below:



The AoA processing also includes the calibration of the compensation coefficients. The flow for the calibration is as show below:



In addition to this the algorithm also enables calculation of the extended velocity based on the overlapped azimuth antennas. The top level flow for the same is as shown below.



4.3 System Parameters

Refer to section 5.1 for common system parameters.

The benchmarks in this section are computed for 128x128@15 FPS 8 Antenna radar data capture.

4.4 CPU Loading and Task Info

4.4.1 Total CPU Load

Note: The DSP Heat map visualization is a visual aid to interpret the FFT computation output drawn at a 3x3 pixel for each data sample magnitude. No DSP optimizations have been applied to the draw logic. Hence the CPU load for DSP can seem higher.

CPU	LOAD TYPE	CPU LOAD
IPU1-0	HWI	1.6%
	SWI	0.6%
	Total	**10.8%**
EVE1	HWI	0.4%
	SWI	0.2%
	Total	**14.5**
EVE2	HWI	0.4%
	SWI	0.2%
	Total	**14.6%**
EVE3	HWI	0.4%
	SWI	0.1%

	Total	**14.7%**
EVE4	HWI	0.4%
	SWI	0.1%
	Total	**14.0%**
DSP1	HWI	0.3%
	SWI	0.1%
	Total	**84.0%**

4.4.2 Task Level Information and Task Level CPU Load

CPU	TASK NAME	TASK DESCRIPTION	CPU LOAD
IPU1-0	Stat Collector	Statistics collector	3.2%
	Capture	Capture frames via VIP	0.2%
	FFT WorkQ Host	Host for all 4 EVE work Q host	2.2%
	Merge	Merge Link for all sensors	0.2%
	Sync	Sync Link for all sensors	0.6%
	Select	Select link to direct sensor output to individual EVEs	0.1%
	UNKNOWN	This is unaccounted CPU load after subtracting the individual task load from total CPU Load	3.8%
	IPC OUT	To send frame to another processor	0.4%
	IPC IN	To receive frames from another processor	0.1%
EVE1	ALG 1D FFT	1D FFT Work Thread	14%
	UNKNOWN	This is unaccounted CPU load after subtracting the individual task load from total CPU Load	0.5%
EVE2	ALG 1D FFT	1D FFT Work Thread	14%
	UNKNOWN	This is unaccounted CPU load after subtracting the individual task load from total CPU Load	0.6%
EVE3	ALG 1D FFT	1D FFT Work Thread	14.2%
	UNKNOWN	This is unaccounted CPU load after subtracting the individual task load from total CPU Load	0.5%
EVE4	ALG 1D FFT	1D FFT Work Thread	13.5%
	UNKNOWN	This is unaccounted CPU load after subtracting the individual task load from total CPU Load	0.5%
DSP1	ALG_RADAR DSP Process	Doppler FFT + Peak Detection + Angle of Arrival	83.4%

CPU	TASK NAME	TASK DESCRIPTION	CPU LOAD
	UNKNOWN	This is unaccounted CPU load after subtracting the individual task load from total CPU Load	0.2%

*NOTE: On DSP all links run in a single thread.

NOTE: CPU load of 0.0% means the CPU load was so low it could not be measured with sufficient granularity.

NOTE: There could be minor variations of +/-0.1% CPU load in different runs of the same use-case

NOTE: Other than above tasks few additional tasks as listed below are active in each processor

- Message Q task: This task is used to listen to control messages sent by any other core. Normally at run-time very few control messages are sent hence this task does not appear in the task load print log
- Processor link task: This task is used to send generic non-link specific messages to another CPU. Normally at run-time very few messages are sent to this task hence this task does not appear in the task load print log
- Remote log client task (on IPU1-0 only): This task looks at the shared remote log buffer and outputs any strings to UART terminal. Normally during run-time prints are not done hence this task does not appear in the task load log

4.5 System Performance

COMPONENT	PARAMETER	CONFIG
Capture (4 Channel)	Output FPS	15
ALG Radar Process (ALG_FXN = Range and Doppler FFT) (EVE)	Output FPS	15
	Avg process time per frame per sensor	9.44 ms
Sync Link (IPU)	Output FPS	15
	Avg process time per frame per sensor	0.5 ms
ALG Radar DSP Process	Output FPS	15
	Avg process time per frame	56.481 ms
Network Tx (Network)	Input FPS	15
	Output Transmit FPS*	15

NOTE: FPS numbers are rounded off to nearest integer
* NOTE: The output FPS from the NETWORK TX link is determined by the network throughput. With a Windows PC connected to a 1Gbps Ethernet switch we see the network bandwidth of ~550 Mbps.

4.6 System Memory Usage

4.6.1 Code/Data Memory Usage

Refer section 5.2 for common Code/Data Memory usage.

4.6.2 Heap Memory Usage

CPU	MEMORY SECTION	MEMORY SIZE RESERVED	MEMORY SIZE USED

IPU1-0	Local Heap	256 KB	96 KB
IPU1-1	Local Heap	640 KB	26 KB
EVE1	L2	22 KB	5 KB
	Local Heap	256KB	1 KB
EVE1	L2	22 KB	5 KB
	Local Heap	256KB	1 KB
EVE1	L2	22 KB	5 KB
	Local Heap	256KB	1 KB
EVE1	L2	22 KB	5 KB
	Local Heap	256KB	1 KB
DSP1	L2	221KB	76 KB
	Local Heap	512 KB	25 KB
Shared Memory	SR1 Frame Buffer	350MB	98 MB
	SR Non-Cached	94KB	4.5 KB

4.7 Other Benchmarks

4.7.1 Processing Latency

		LATENCY
Capture to Network Tx Latency	Avg	68.208 ms

NOTE:

- This latency is as measured inside the system by software.
- There will an additional 1/(capture rate) added on top of this from sensor/receiver itself.

4.7.2 Boot Time

SL NO.	PARAMETER		VALUE
1	Use-case create start		4.16 s
2	a	AWR1243* and FPGA Reset and Boot time	1.22 s
2	b	AWR1243 Firmware Load Time	8.14 s
2	c	AWR1243 Configuration Time	0.06 s
2	e	Other Links Start and Create	4.44 s
3	**Total Boot time**		**18.02 s**

* Assume AWR1243 ES2.0

5 TDA3xx Common System Parameters

5.1 System Parameters

The system parameters mentioned below are common across all configurations unless specified otherwise.

COMPONENT	PROPERTY	VALUE
SOC	SOC Name	TDA3xx
	SOC revision	1.0
EVM	EVM Name	TI TDA3xx EVM
IPU	Clock	212.8Mhz

COMPONENT	PROPERTY	VALUE
	L1-P cache	ENABLED
	L1-D cache	ENABLED
	Code/Data Placement	DDR
DSP	Clock	500Mhz
	L1-P cache	32KB ENABLED
	L1 D cache	32KB ENABLED
	L2 P/D cache	32KB ENABLED
	Code/Data Placement	DDR
EVE	Clock	ARP32 250MHz VCOP 500Mhz
	L1-P cache	ENABLED
	DMEM	USED FOR IPC and ALG TASK STACK
	Code/Data Placement	DDR
DDR Config	Clock	532Mhz
	Bus Width	32-bit
	Number of EMIFs	1
	DDR size	512 MB
Sensor 1	Part number	AWR1243
	Data Format	RAW12 bit/RAW14 bit/2x RAW8 bit
HDMI TX 1	Part number	SII 9022A
	DCLK	148.5Mhz
	Resolution @ frame-rate	1920x1080 @ 60fps
	Data format	RGB888
	Bus width	24-bit
	Sync Type	HS/VS discrete sync
DSS Display	DSS pipe	VID1 VID2 GRPX Any or all of above used based on use-case
	DSS output port	DPI1 for LCD, HDMI (Off-Chip HDMI TX)
	DSS VENC	LCD1 for LCD and HDMI (Off-Chip HDMI TX) SDDAC for NTSC/PAL Display
	Inline scaling	ENABLED or DISABLED based on use-case

5.2 Code/Data Memory Usage

NOTE: Code/data memory for data structures is same for all use-cases since a single binary is used for all use-cases. These configurations are with respect to 128MB Memory map.

CPU	MEMORY SECTION	MEMORY SIZE RESERVED	MEMORY SIZE USED
IPU1-0	Initialized section (.text, .const)	7.5MB	2.79 MB

	Uninitialized section (.bss, .heap, .stack)	12MB	8.33 MB
IPU1-1	Initialized section (.text, .const)	2MB	0.27 MB
	Uninitialized section (.bss, .heap, .stack)	4.5MB	4.18 MB
DSP1	Initialized section (.text, .const)	1.5MB	0.25 MB
	Uninitialized section (.bss, .heap, .stack)	11MB	3.59 MB
EVE1	Initialized section (.text, .const)	2.5MB	0.26 MB
	Uninitialized section (.bss, .heap, .stack)	6MB	1.63 MB

5.3 App Image Size

PARAMETER	VALUE
App Image size (4 CPU images)	5.52 MB

This App Image contains images for all the 4 processors.

6 TDA2xx Common System Parameters

6.1 System Parameters

The system parameters mentioned below are common across all configurations unless specified otherwise.

COMPONENT	PROPERTY	VALUE
SOC	SOC Name	TDA2xx
	SOC revision	2.0
EVM	EVM Name	TI TDA2xx Cascade EVM
IPU	Clock	212.8Mhz
	L1-P cache	ENABLED
	L1-D cache	ENABLED
	Code/Data Placement	DDR
DSP	Clock	600Mhz
	L1-P cache	32KB ENABLED
	L1 D cache	32KB ENABLED
	L2 P/D cache	32KB ENABLED
	Code/Data Placement	DDR
EVE	Clock	ARP32 267MHz VCOP 535Mhz
	L1-P cache	ENABLED
	DMEM	USED FOR IPC and ALG TASK STACK
	Code/Data Placement	DDR
DDR Config	Clock	532Mhz
	Bus Width	32-bit
	Number of EMIFs	2
	DDR size	1024 MB

COMPONENT	PROPERTY	VALUE
Sensor 1	Part number	AWR1243
	Data Format	RAW12 bit/RAW14 bit/2x RAW8 bit

6.2 Code/Data Memory Usage

NOTE: Code/data memory for data structures is same for all use-cases since a single binary is used for all use-cases.

CPU	MEMORY SECTION	MEMORY SIZE RESERVED	MEMORY SIZE USED
IPU1-0	Initialized section (.text, .const)	10MB	2 MB
	Uninitialized section (.bss, .heap, .stack)	11MB	8 MB
IPU1-1	Initialized section (.text, .const)	2MB	0.293 MB
	Uninitialized section (.bss, .heap, .stack)	9MB	3.7 MB
DSP1	Initialized section (.text, .const)	4MB	0.27 MB
	Uninitialized section (.bss, .heap, .stack)	12MB	1.98 MB
EVE1	Initialized section (.text, .const)	2MB	0.289 MB
	Uninitialized section (.bss, .heap, .stack)	13MB	1.69 MB
EVE2	Initialized section (.text, .const)	2MB	0.289 MB
	Uninitialized section (.bss, .heap, .stack)	13MB	1.69 MB
EVE3	Initialized section (.text, .const)	2MB	0.289 MB
	Uninitialized section (.bss, .heap, .stack)	13MB	1.69 MB
EVE4	Initialized section (.text, .const)	2MB	0.289 MB
	Uninitialized section (.bss, .heap, .stack)	13MB	1.69 MB

6.3 App Image Size

PARAMETER	VALUE
App Image size (7 CPU images)	6.06 MB

This App Image contains images for the 7 (IPU1_0, IPU1_1, DSP1, EVE1/2/3/4) processors.

7 Revision History

Version	Date	Revision History
1.00	23rd Oct 2016	Document First Version for (Processor SDK Radar Release v2.11)
1.01	25th Oct 2016	Review Feedback updates
2.00	5th Feb 2017	Changes for Processor SDK Radar Release v2.12
3.00	30th June 2017	Changes for Processor SDK Radar Release v3.0
3.01	14th Oct 2017	Changes for Processor SDK Radar Release v3.01
3.02	20th Dec 2017	Changes for Processor SDK Radar Release v3.02
3.03	4th April 2018	Changes for Processor SDK Radar Release v3.03
3.04	24th June 2018	Changes for Processor SDK Radar Release v3.04