PROCESSOR SDK Radar on RTOS (v03.03.00)

Data Sheet

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

Table of Contents

1 Introduction

IMPORANT NOTE:

- This datasheet has performance and feature information about use-cases running on TDA3xx with AWR1243 sensor to capture and process Radar data.

1.1 Framework features

- Compile and build for all CPUs
  - TDA3xx system (IPU1-0, IPU1-1, DSP1, DSP2, EVE1).
- Debug and release build profiles.
- Single place to setup memory map
  - Default 128MB DDR
- Ability to create and control links on any CPU.
- Remote log feature with ability to print logs from all CPUs to UART controlled by IPU1-0. On the ALPS board the logs are printed using Network console.
- CPU load profiling for all cores.
- Memory usage log for all cores.
- Run time use-cases performance statistics like frame-rate, latency, frame-drop.
- Exception handler log for IPU, EVE and DSP.
- EDMA support on all cores, wherever applicable
  - IPU uses system EDMA (via EDMA3LLD library)
  - DSP uses system EDMA or local EDMA (via EDMA3LLD library)
  - EVE uses local EDMA (via EDMA3LLD library and/or EVE SW library)
- Global timestamp to keep track of common time across all CPUs.
- Buffer allocation APIs for DDR, OCMC memory, L2 memory (DSP/EVE).
- Use-Case Auto Generation tool which generates C code for Processor SDK Radar use-cases from txt based config file.

1.2 Supported Links

No.	Links	TDA3xx
Framework Related Links		
1	VIP Capture	YES
2	Display	YES
3	Display controller	YES
4	IPC OUT/IN	YES
5	Dup	YES
6	Merge	YES
7	Sync	YES
8	Select	YES
9	Null	YES
10	Null Source	YES
11	ISS Capture	YES
12	ISS M2M ISP	YES
13	ISS M2M Simcop	YES
14	Gate	YES
Other Sample link's		
1	Graphics Source	YES
2	Network Ctrl	YES
Algorithm plugin's		
1	Alg plugin for Radar Processing	YES
Algorithm Functions		
1	Alg Fxn for Radar Frame Copy	YES
2	Alg Fxn for Radar Range and Doppler FFT	YES
3	Alg Fxn for drawing the Range and Doppler FFT output as a Heat Map	YES
4	Alg Fxn for Radar Peak Detection	YES
5	Alg Fxn for Radar Beam Forming	YES
6	Alg Fxn for drawing the Object Detection	YES
Work Queue		
1	Alg Fxn for FFT implemented with work queue	YES
2	Alg Fxn for Peak Detection implemented with work queue	YES

No.	Links	TDA3xx
3	Alg Fxn for Beam Forming implemented with work queue	YES

2 TDA3xx + AR12 ALPS Capture, Object Detection, Null

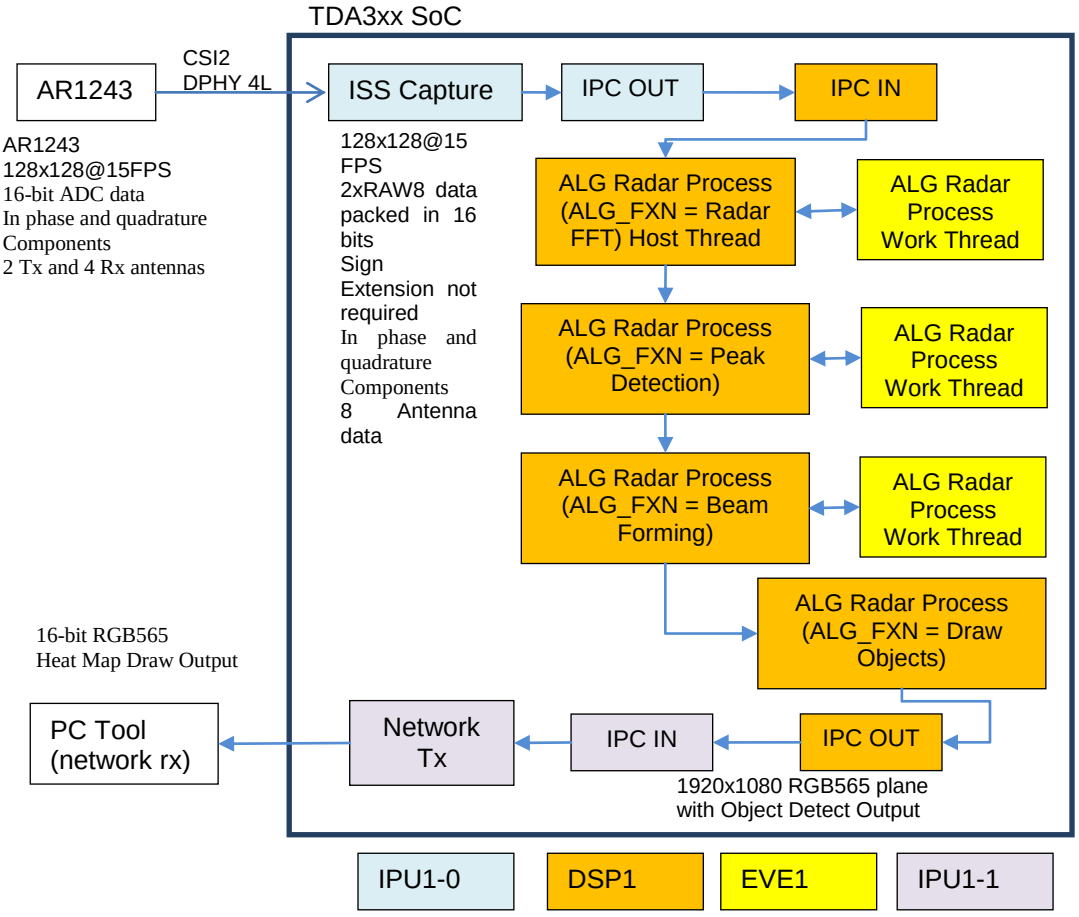
2.1 Overview

This use case consists of continuous capture of AWR12xx radar sensor data from CSI using the IPU as CSI2 host CPU for buffer management. This is followed by the Range and Doppler FFT computation of the input data corresponding to the N input antennae on the EVE. This is achieved using work queue infrastructure with the host thread on the DSP and the work thread on the EVE. The output of the 2D-FFT is passed through the peak detection and the beam forming stages in the EVE (again implemented via workQ). The detected objects are then plotted in a graph which indicates the range and the angle of the object. The color of the object indicates the relative velocity of the objects.

Capture is done for 128 samples per chirp and 128 chirps per frame @ 15 FPS 8 Antennae using the CSI2.

2.2 Data Flow

This usecase demonstrates the EVE object detection computation. The data flow below shows a radar data capture for a configuration of 128 samples per chirp and 128 chirps per frame @ 15 FPS for 4 Rx Antenna and 2 Tx Antenna.



2.3 System Parameters

Refer to section 4.1 for common system parameters.

The benchmarks in this section are computed for 128x128@15 FPS 8 Antenna radar data capture.

2.4 CPU Loading and Task Info

2.4.1 Total CPU Load

Note: The DSP Heat map visualization is a visual aid to interpret the FFT computation output drawn at a 3x3 pixel for each data sample magnitude. No DSP optimizations have been applied to the draw logic. Hence the CPU load for DSP can seem higher.

CPU	LOAD TYPE	CPU LOAD
IPU1-0	HWI	0.6%
	SWI	0.3%
	Total	**3.6%**
EVE1	HWI	0.4%
	SWI	0.1%
	Total	**6.5%**
DSP1	HWI	0.3%
	SWI	0.1%
	Total	**6.1%**
IPU1-1	HWI	3.2%
	SWI	0.6%
	Total	**30.7%**

2.4.2 Task Level Information and Task Level CPU Load

CPU	TASK NAME	TASK DESCRIPTION	CPU LOAD
IPU1-0	Stat Collector	Statistics collector	1.70%
	ISS Capture	Capture frames via CSI2	0.10%
	UNKNOWN	This is unaccounted CPU load after subtracting the individual task load from total CPU Load	0.90%
	IPC OUT	To send frame to another processor	0.20%
EVE1	ALG Range and Doppler FFT + Peak Detection + Beam Forming	Range and Doppler FFT + Peak Detection + Beam Forming	6.0%
	UNKNOWN	This is unaccounted CPU load after subtracting the individual task load from total CPU Load	0.10%
DSP1	*IPC + ALG Draw Objects + WorkQ Host Thread	Draw Objects + IPC + Forward processing request to EVE	5.70%
	UNKNOWN	This is unaccounted CPU load after subtracting the individual task load from total CPU Load	0.40%
IPU1-1	NULL	Null Link reception of draw output and forward to network	0.40%
		To receive frame from DSP1	0.20%

	Networking and Miscellaneous	This takes into account the networking task and stack operation. This is with the network PC tool running. This includes unaccounted CPU load after subtracting the individual task load from total CPU Load.	26.30%

*NOTE: On DSP all links run in a single thread.

NOTE: CPU load of 0.0% means the CPU load was so low it could not be measured with sufficient granularity.

NOTE: There could be minor variations of +/-0.1% CPU load in different runs of the same use-case

NOTE: Other than above tasks few additional tasks as listed below are active in each processor

- Message Q task: This task is used to listen to control messages sent by any other core. Normally at run-time very few control messages are sent hence this task does not appear in the task load print log
- Processor link task: This task is used to send generic non-link specific messages to another CPU. Normally at run-time very few messages are sent to this task hence this task does not appear in the task load print log
- Remote log client task (on IPU1-1 and IPU1-0 only): This task looks at the shared remote log buffer and outputs any strings to Network console terminal. Normally during run-time prints are not done hence this task does not appear in the task load log

2.5 System Performance

COMPONENT	PARAMETER	CONFIG
ISS Capture	Output FPS	15
ALG Radar Process (ALG_FXN = Range and Doppler FFT) (EVE)	Output FPS	15
	Avg process time per frame	1.541 ms
ALG Radar Process (ALG_FXN = Peak Detection) (EVE)	Output FPS	15
	Avg process time per frame	1.181ms
ALG Radar Process (ALG_FXN = Beam Forming) (EVE)	Output FPS	15
	Avg process time per frame	0.268 ms
ALG Radar Process (ALG_FXN = Draw Objects) (DSP)	Output FPS	15
	Avg process time per frame	7.998 ms
Null (Network)	Input FPS	15
	Output Transmit FPS*	15

NOTE: FPS numbers are rounded off to nearest integer
NOTE: The above benchmarks are computed for 128x128 @ 15 fps 8 Antenna capture and network transmit of 2D-FFT Object position (1080p60)
* NOTE: The output FPS from the NULL link is determined by the network throughput. With a Windows PC connected to a 1Gbps Ethernet switch we see the network bandwidth of ~550 Mbps to transmit RGB565 raw 1080p buffer output by the DSP at 15 FPS using TFDTP. When using TCP/IP the FPS of transmit of the raw frame is ~1.5 FPS.

2.6 System Memory Usage

2.6.1 Code/Data Memory Usage

Refer section 4.2 for common Code/Data Memory usage.

2.6.2 Heap Memory Usage

CPU	MEMORY SECTION	MEMORY SIZE RESERVED	MEMORY SIZE USED
IPU1-0	Local Heap	256 KB	5 KB
EVE1	L2	22 KB	12 KB
	Local Heap	256KB	2 KB
DSP1	L2	221KB	0 KB
	Local Heap	512 KB	87 KB
Shared Memory	SR1 Frame Buffer	74MB	49 MB
	SR Non-Cached	100KB	4.5 KB

2.7 Other Benchmarks

2.7.1 Processing Latency

		LATENCY
Capture to Null Latency	Average	13.233 ms

NOTE:

- This latency is as measured inside the system by software.
- There will an additional 1/(capture rate) added on top of this from sensor/receiver itself.

2.7.2 Boot Time

SL NO.	PARAMETER		VALUE
1	SBL to App main() (QSPI Boot) The boot time will change based on the mode of boot – SD, NOR flash or QSPI.		0.37 s
2	main() to Use-case menu		1.15 s
3	Network Initialization		4.94 s
4	Use-case create start to output		0.35 s
4	a	AWR1243 Reset and Boot time	0.22 s
4	b	AWR1243 Firmware Load Time (Pre-flashed)	0 s
4	c	AWR1243 Configuration Time	0.015 s
4	d	Other Links Start and Create	0.115 s
5	**Total Boot time**		**6.81 s**

2.7.3 AR12 Firmware Flash Time

The time taken to erase the AR12 flash and program the MSS and BSS firmware is as below:

Sl. No.	Action	Size	Time

1.	Erase Flash	4MB	11.82 s
2.	Flash the BSS Firmware	193 KB	41.32 s
3.	Flash the MSS Firmware	97 KB	21.03 s
4.	Flash the Configuration Structure	164 B	0.41 s

3 TDA3x EVM + AR12 Booster Pack Capture, Object Detect, display

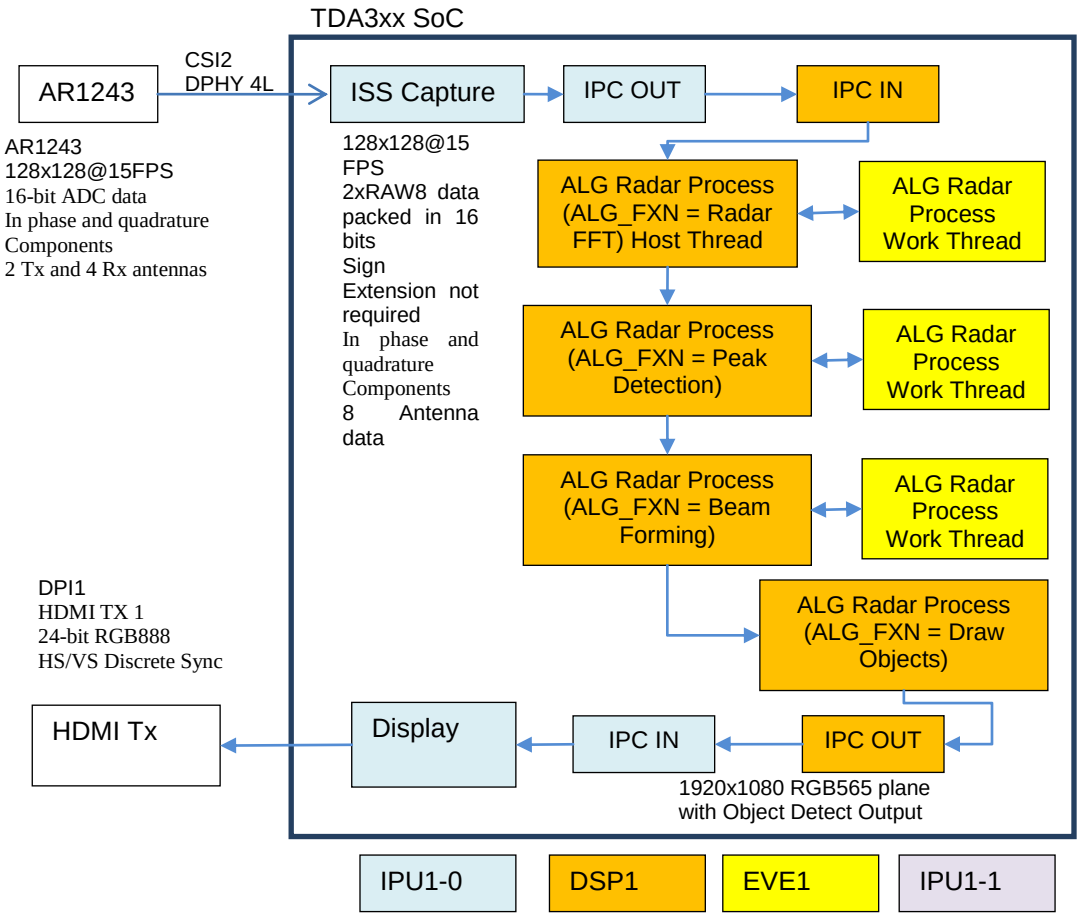
3.1 Overview

This use case consists of continuous capture of AWR12xx radar sensor data from CSI using the IPU as CSI2 host CPU for buffer management. This is followed by the Range and Doppler FFT computation of the input data corresponding to the N input antennae on the EVE. This is achieved using work queue infrastructure with the host thread on the DSP and the work thread on the EVE. The output of the 2D-FFT is passed through the peak detection and the beam forming stages in the EVE (again implemented via workQ). The detected objects are then plotted in a graph which indicates the range and the angle of the object. The color of the object indicates the relative velocity of the objects.

Capture is done for 128 samples per chirp and 128 chirps per frame @ 15 FPS 8 Antennae using the CSI2. Display is used to show the percentage loading of all the CPUs in the TDA device and the 2D-FFT heat map to show detected objects.

3.2 Data Flow

This usecase demonstrates the EVE FFT computation in the range and Doppler dimensions. The data flow below shows a radar data capture for a configuration of 128 samples per chirp and 128 chirps per frame @ 15 FPS for 4 Rx Antenna and 2 Tx Antenna.



3.3 System Parameters

Refer to section 4.1 for common system parameters.

The benchmarks in this section are computed for 128x128@15 FPS 8 Antenna radar data capture.

3.4 CPU Loading and Task Info

3.4.1 Total CPU Load

Note: The DSP Heat map visualization is a visual aid to interpret the FFT computation output drawn at a 3x3 pixel for each data sample magnitude. No DSP optimizations have been applied to the draw logic. Hence the CPU load for DSP can seem higher.

CPU	LOAD TYPE	CPU LOAD
IPU1-0	HWI	1.2%
	SWI	0.4%
	Total	**7.4%**
EVE1	HWI	0.5%
	SWI	0.2%
	Total	**5.1%**
DSP1	HWI	0.3%
	SWI	0.1%
	Total	**5.2%**

3.4.2 Task Level Information and Task Level CPU Load

CPU	TASK NAME	TASK DESCRIPTION	CPU LOAD
IPU1-0	Stat Collector	Statistics collector	1.6%
	ISS Capture	Capture frames via CSI2	0.1%
	Graphics	Graphics update for the CPU load	2.7%
	Display	Display Objects	0.2%
	UNKNOWN	This is unaccounted CPU load after subtracting the individual task load from total CPU Load	2.5%
	IPC OUT	To send frame to another processor	0.2%
	IPC IN	To receive frames from another processor	0.1%
EVE1	ALG 2D FFT + Peak detection + beam forming	2D FFT + Peak detection + beam forming Work Thread	4.4%
	UNKNOWN	This is unaccounted CPU load after subtracting the individual task load from total CPU Load	0.7%

CPU	TASK NAME	TASK DESCRIPTION	CPU LOAD
DSP1	*IPC + ALG Draw + FFT WorkQ Host Thread	Draw Object + IPC + Forward processing request to EVE	4.8%
	UNKNOWN	This is unaccounted CPU load after subtracting the individual task load from total CPU Load	0.4%

*NOTE: On DSP all links run in a single thread.

NOTE: CPU load of 0.0% means the CPU load was so low it could not be measured with sufficient granularity.

NOTE: There could be minor variations of +/-0.1% CPU load in different runs of the same use-case

NOTE: Other than above tasks few additional tasks as listed below are active in each processor

- Message Q task: This task is used to listen to control messages sent by any other core. Normally at run-time very few control messages are sent hence this task does not appear in the task load print log
- Processor link task: This task is used to send generic non-link specific messages to another CPU. Normally at run-time very few messages are sent to this task hence this task does not appear in the task load print log
- Remote log client task (on IPU1-0 only): This task looks at the shared remote log buffer and outputs any strings to UART terminal. Normally during run-time prints are not done hence this task does not appear in the task load log

3.5 System Performance

COMPONENT	PARAMETER	CONFIG
ISS Capture	Output FPS	15
ALG Radar Process (ALG_FXN = Range and Doppler FFT) (EVE)	Output FPS	15
	Avg process time per frame	1.572 ms
ALG Radar Process (ALG_FXN = Peak Detection) (EVE)	Output FPS	15
	Avg process time per frame	1.257 ms
ALG Radar Process (ALG_FXN = Beam Forming) (EVE)	Output FPS	15
	Avg process time per frame	0.28 ms
ALG Radar Process (ALG_FXN = Draw Objects) (DSP)	Output FPS	15
	Avg process time per frame	9.34 ms
Display	Input FPS	15
	VENC FPS	60

NOTE: FPS numbers are rounded off to nearest integer
NOTE: The above benchmarks are computed for 128x128 @ 15 fps 8 Antenna capture and HDMI display of graph with detected objects (1080p60)

3.6 System Memory Usage

3.6.1 Code/Data Memory Usage

Refer section 4.2 for common Code/Data Memory usage.

3.6.2 Heap Memory Usage

CPU	MEMORY SECTION	MEMORY SIZE RESERVED	MEMORY SIZE USED
IPU1-0	Local Heap	256 KB	5 KB
EVE1	L2	22 KB	12 KB
	Local Heap	256KB	2 KB
DSP1	L2	221KB	0 KB
	Local Heap	512 KB	87 KB
Shared Memory	SR1 Frame Buffer	74MB	51 MB
	SR Non-Cached	94KB	4.5 KB

3.7 Other Benchmarks

3.7.1 Processing Latency

		LATENCY
Capture to Display Latency	Avg	13.088 ms

NOTE:

- This latency is as measured inside the system by software.
- There will an additional 1/(capture rate) added on top of this from sensor/receiver itself.

3.7.2 Boot Time

SL NO.	PARAMETER		VALUE
1	SBL to App main() (QSPI Boot) The boot time will change based on the mode of boot – SD, NOR flash or QSPI.		0.36 s
2	main() to Use-case create		1.14 s
3	Use-case create start to display		4.16 s
3	a	AWR1243 Reset and Boot time	0.35 s
3	b	AWR1243 Firmware Load Time	0.22 s
3	c	AWR1243 Configuration Time	1.84 s
3	d	GRPX Link Create Time	1.55 s
3	e	Other Links Start and Create	0.2 s
4	**Total Boot time**		**5.66 s**

4 TDA3xx Common System Parameters

4.1 System Parameters

The system parameters mentioned below are common across all configurations unless specified otherwise.

COMPONENT	PROPERTY	VALUE
SOC	SOC Name	TDA3xx
	SOC revision	1.0
EVM	EVM Name	TI TDA3xx EVM
IPU	Clock	212.8Mhz
	L1-P cache	ENABLED
	L1-D cache	ENABLED
	Code/Data Placement	DDR
DSP	Clock	500Mhz
	L1-P cache	32KB ENABLED
	L1 D cache	32KB ENABLED
	L2 P/D cache	32KB ENABLED
	Code/Data Placement	DDR
EVE	Clock	ARP32 250MHz VCOP 500Mhz
	L1-P cache	ENABLED
	DMEM	USED FOR IPC and ALG TASK STACK
	Code/Data Placement	DDR
DDR Config	Clock	532Mhz
	Bus Width	32-bit
	Number of EMIFs	1
	DDR size	512 MB
Sensor 1	Part number	AWR1243
	Data Format	RAW12 bit/RAW14 bit/2x RAW8 bit
HDMI TX 1	Part number	SII 9022A
	DCLK	148.5Mhz
	Resolution @ frame-rate	1920x1080 @ 60fps
	Data format	RGB888
	Bus width	24-bit
	Sync Type	HS/VS discrete sync
DSS Display	DSS pipe	VID1 VID2 GRPX Any or all of above used based on use-case
	DSS output port	DPI1 for LCD, HDMI (Off-Chip HDMI TX)
	DSS VENC	LCD1 for LCD and HDMI (Off-Chip HDMI TX) SDDAC for NTSC/PAL Display
	Inline scaling	ENABLED or DISABLED based on use-case

4.2 Code/Data Memory Usage

NOTE: Code/data memory for data structures is same for all use-cases since a single binary is used for all use-cases. These configurations are with respect to 128MB Memory map and ALPS board.

CPU	MEMORY SECTION	MEMORY SIZE RESERVED	MEMORY SIZE USED
IPU1-0	Initialized section (.text, .const)	7.5MB	2.79 MB
	Uninitialized section (.bss, .heap, .stack)	12MB	8.33 MB
IPU1-1	Initialized section (.text, .const)	2MB	0.27 MB
	Uninitialized section (.bss, .heap, .stack)	4.5MB	4.18 MB
DSP1	Initialized section (.text, .const)	1.5MB	0.25 MB
	Uninitialized section (.bss, .heap, .stack)	11MB	3.59 MB
EVE1	Initialized section (.text, .const)	2.5MB	0.26 MB
	Uninitialized section (.bss, .heap, .stack)	6MB	1.63 MB

4.3 App Image Size

PARAMETER	VALUE
App Image size (4 CPU images)	5.52 MB

This App Image contains images for all the 4 processors.

5 Revision History

Version	Date	Revision History
1.00	23rd Oct 2016	Document First Version for (Processor SDK Radar Release v2.11)
1.01	25th Oct 2016	Review Feedback updates
2.00	5th Feb 2017	Changes for Processor SDK Radar Release v2.12
3.00	30th June 2017	Changes for Processor SDK Radar Release v3.0
3.01	14th Oct 2017	Changes for Processor SDK Radar Release v3.01
3.02	20th Dec 2017	Changes for Processor SDK Radar Release v3.02
3.03	4th April 2018	Changes for Processor SDK Radar Release v3.03