# BIOS Driver (BSP) Overview

ADAS Driver Team
7th January 2015
V1.1

# Agenda

- TDA2xx/TDA3xx Hardware Overview
- BSP Software Overview
- Directory Structure
- Module Description
- Overview of Each IP
- Q&A

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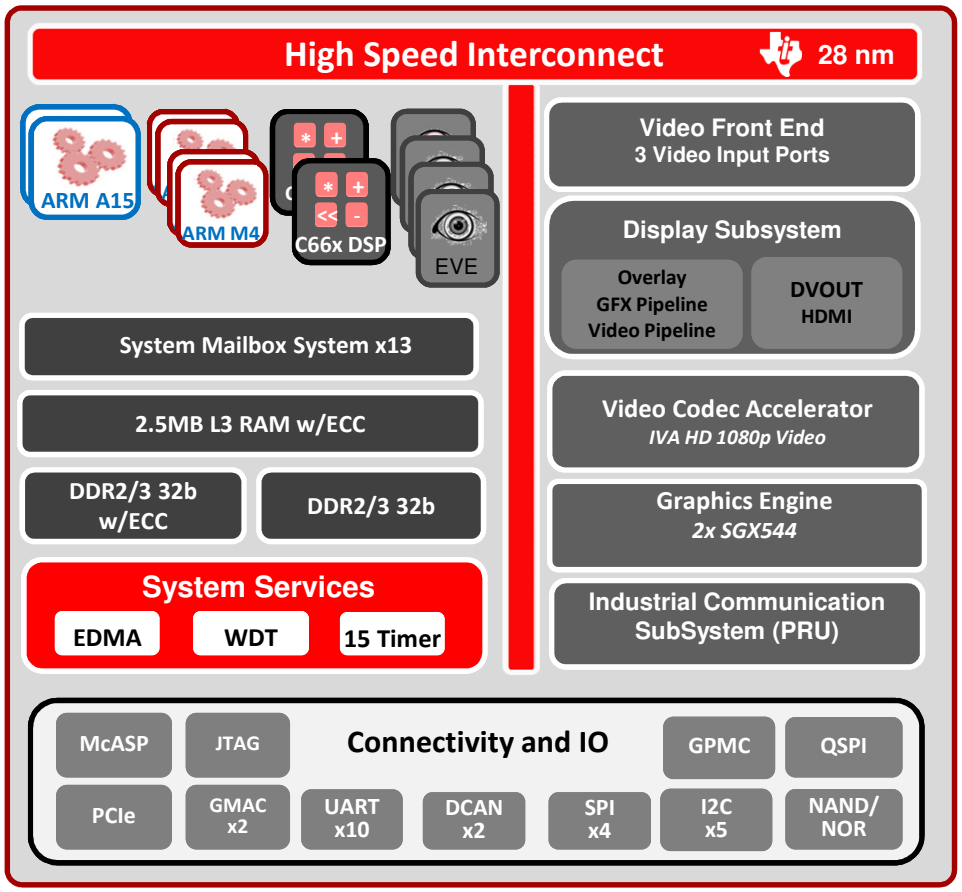
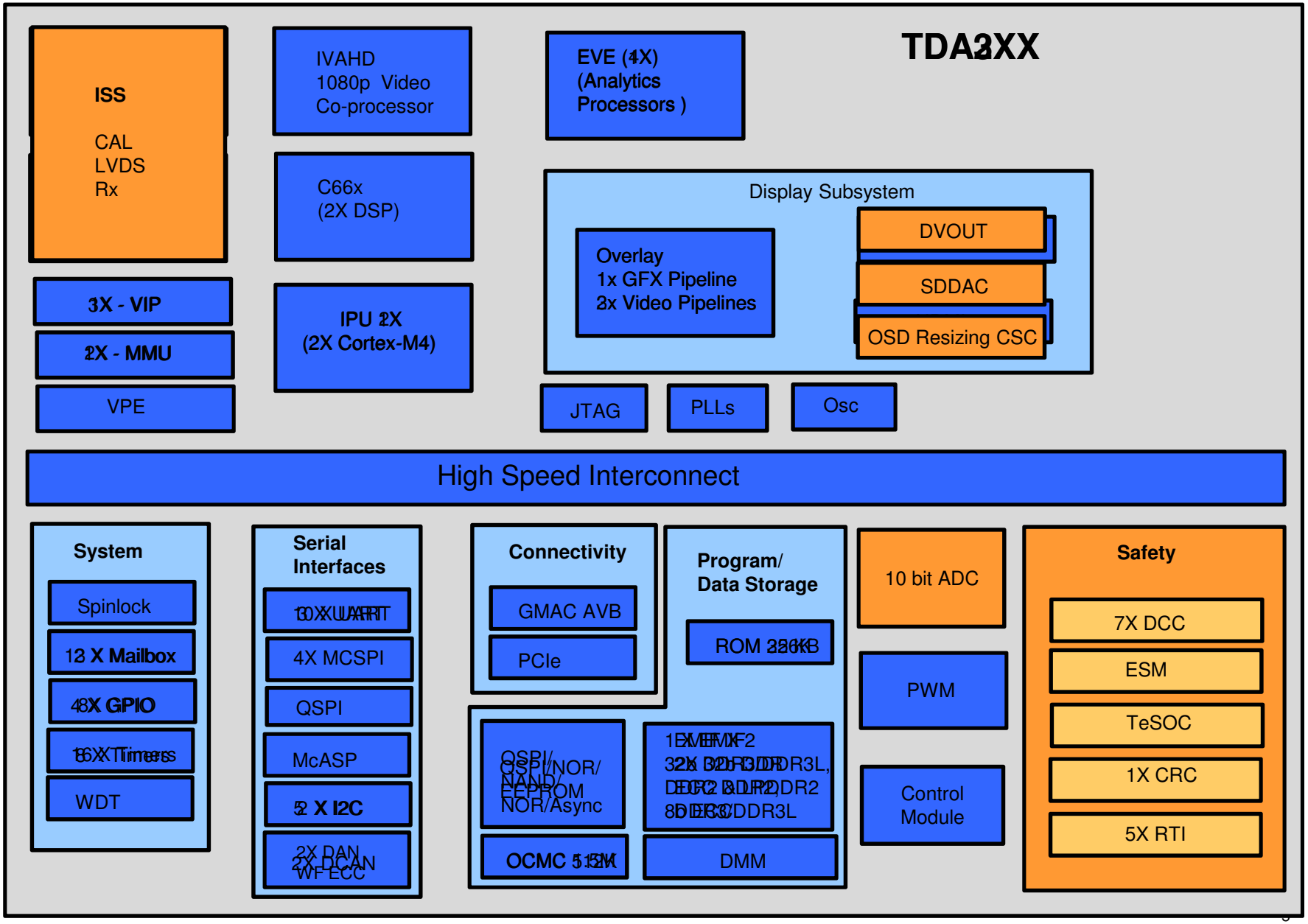
# TDA2x scalable family (superset)

- **Two Next Generation DSP Cores: C66x™**
  - Up to 750 MHz – 24GMACs / 12GFLOPs
  - Floating Point Extension
- **Dual ARM Cortex™ A15 Cores**
  - Up to 750MHz – 5250DMIPs
  - NEON Vector Floating point
- **Two dual ARM Cortex™ M4 Cores**
  - 200 MHz
- **Four Vision Accelerator Cores: EVE**
  - Each core has an 16MAC per cycle computing engine with up to 650 MHz (8bit or 16bit ) – 10.4GMACs per core
- **Video Codec Accelerator**
  - IVA-HD core running at up to 532MHz
- **Graphics Engine**
  - Dual SGX544 core delivering capability to render upto 170Mpoly/s / 5000MPixel/s / 34GFLOPs at 500Mhz
- **Internal Memory**
  - DSPs: each w/ 32 KB L1D, 32 KB L1P, unified 256 KB L2 Cache
  - ARM : 32 KB L1D, 32 KB L1P, combined 2 MB L2 Cache
  - On Chip L3 RAM: 2.5MB with ECC
- **Peripherals Highlights (1.8/ 3.3V IOs)**
  - Up to three Video input Ports, each with two 16 bit sub ports
  - Display system Digital Video Output
  - Two EMIFs: 2x 32bit wide DDR2/3/3L @ 532MHz, one with ECC
  - GPMC: general purpose memory controller
  - Support for NOR Flash
  - PRU Subsystem
  - PCIe, 2x Gbit EMAC with AVB support
  - 2x DCAN (High end CAN controller)
  - 10x UART, 5x I²C, 4x McSPI, Quad SPI, McASP, 15x Timers, WDT, GPIO




- **Package**
  - **23x23mm BGA (AAS)** -
  - **17x17mm BGA (AAS)** - reduced feature set


TDA3XX
ISS
CAL
LVDS
Rx
IVAHD
1080p Video
Co-processor
EVE (4X)
(Analytics
Processors )
C66x
(2X DSP)
Display Subsystem
Overlay
1x GFX Pipeline
2x Video Pipelines
DVOUT
SDDAC
OSD Resizing CSC
3X - VIP
2X - MMU
VPE
IPU 2X
(2X Cortex-M4)
JTAG
PLLs
Osc
High Speed Interconnect
System
Spinlock
12 X Mailbox
48X GPIO
16X Timers
WDT
Serial
Interfaces
10X UART
4X MCSPI
QSPI
McAsp
5 X I2C
2X DCAN
Connectivity
GMAC AVB
PCIe
Program/
Data Storage
ROM 256KB
QSPI/
NOR/
NAND/
EEPROM
NOR/Async
OCMC 1MB
DMM
10 bit ADC
PWM
Control
Module
Safety
7X DCC
ESM
TeSOC
1X CRC
5X RTI

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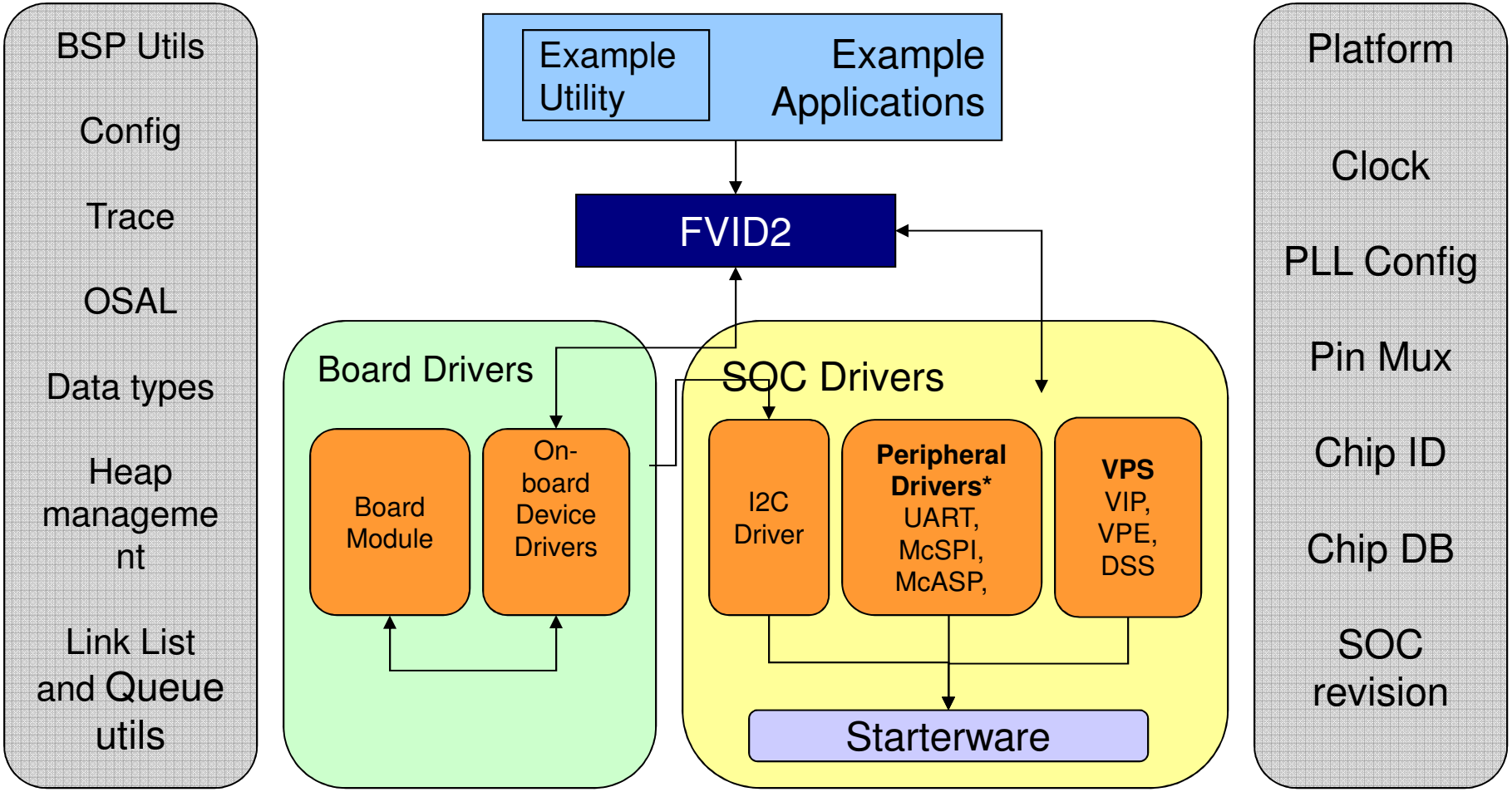
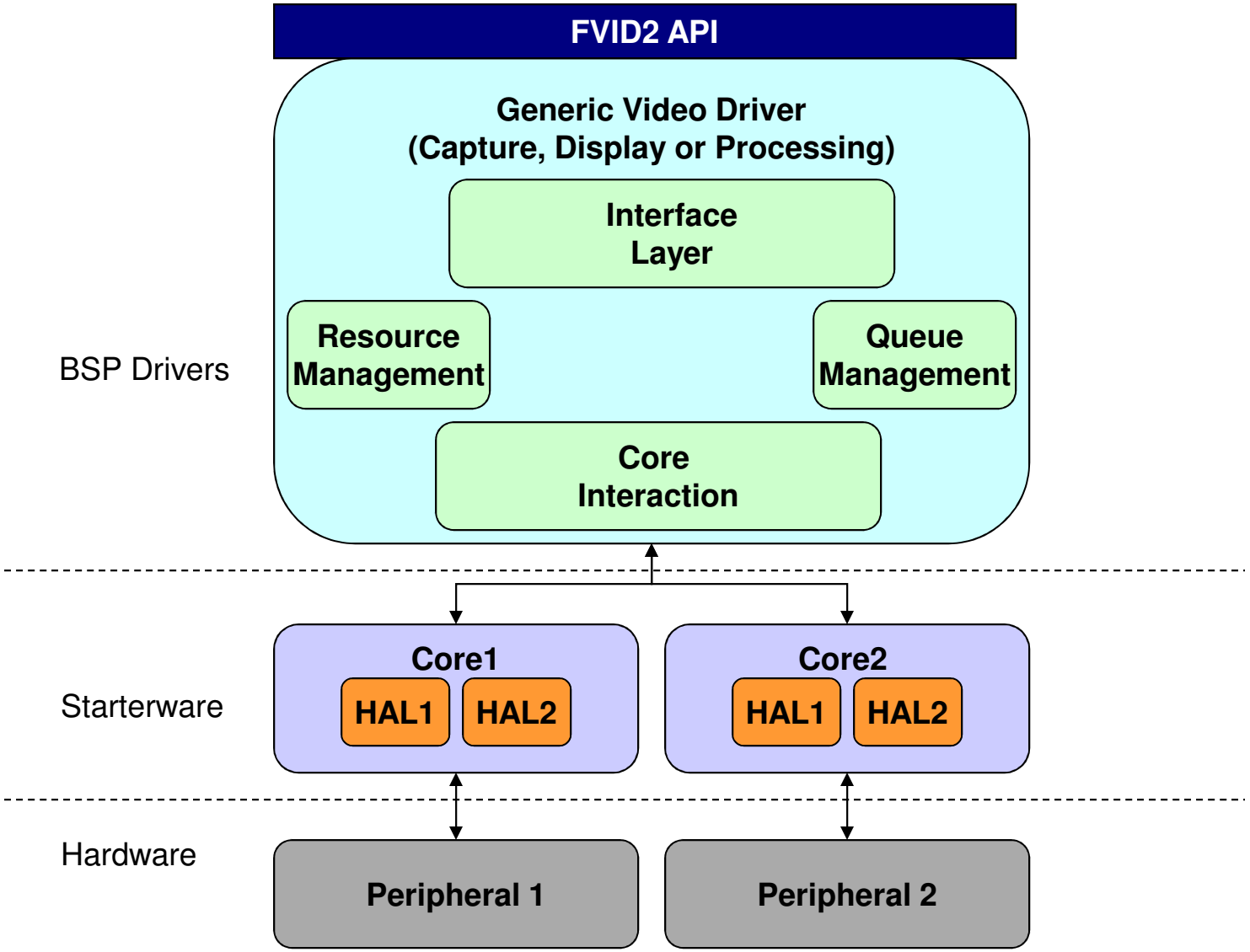
# What is BSP – BIOS Support Package?

- Video and Serial Drivers on SysBIOS based processors only
- Video Drivers supports VIP, VPE (Only in TDA2xx), ISS (Only in TDA3xx) and DSS IP's and provide FVID2-based Interface for following category of Drivers
  - Capture Driver
  - Video Processing Driver
  - Display Driver
- Serial Drivers supports
  - I2C
  - McASP
  - McSPI
  - UART
  - Audio and AIC31 codec IP's and (Only for TDA2xx)
  - GIO-based Interface for the drivers of these IP's

# BIOS Support Package (BSP) Block Diagram



# Video Driver Stack



# BSP Description

- BSP and platform layers are accessed by all the modules
- VPS drivers and on board device drivers are based on FVID2 interface
- Other peripheral drivers are based on GIO Interface
- Double arrow represents interactions between both modules – both the modules call each other functions
- Single arrow represents a hierarchy – One module calling the other and not the other way
- Board module contains board specific data like board level mux configuration, list of I2C devices present and any special board specific programming needs

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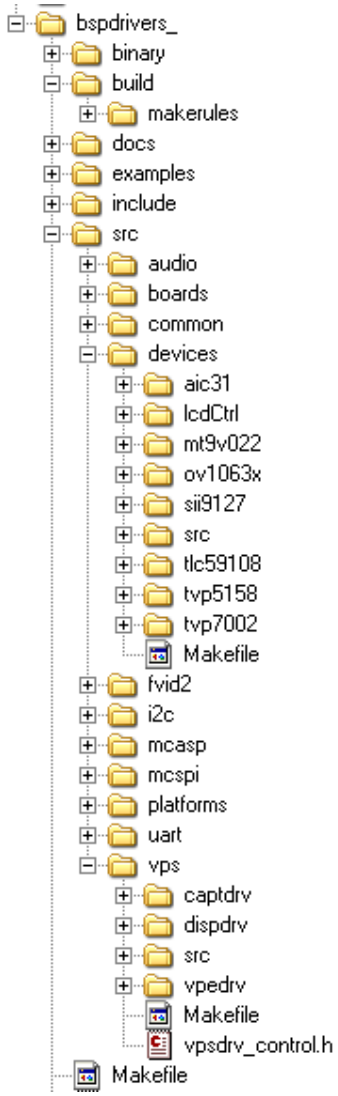
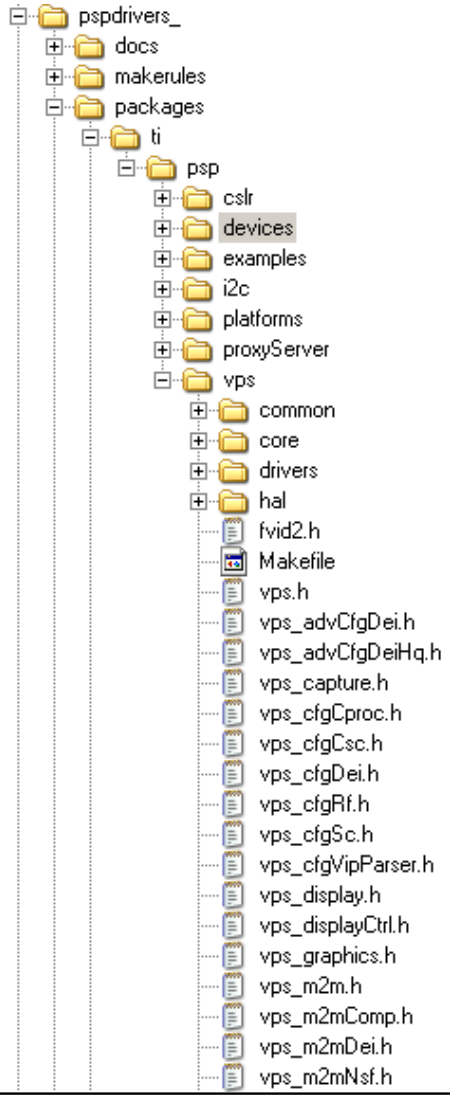
# Directory Structure

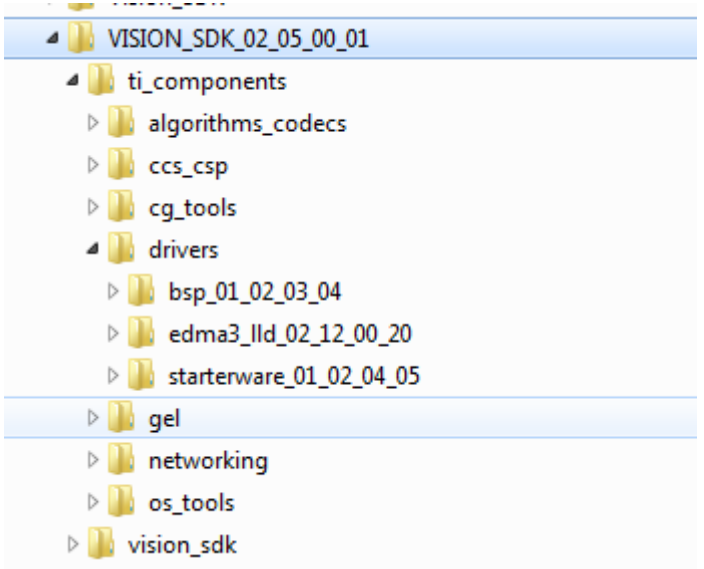
## TDAxxx BSP




## TI81xx HDVPSS




## Vision SDK



# Directory Structure Description

- **bspdrivers_**
  - Top level make file and Rules.make containing package paths
- **bsp\binary:**
  - All the build files and executables are generated here
- **bsp\build:**
  - Contains all build related make files
- **bsp\docs:**
  - Contains user guide, API guide, release notes, migration guide etc…
  - Contains Gel files for various platforms
  - Contains test image files
- **bsp\examples:**
  - Application level utility functions which could be used by customers as is or with minimal modification
  - Sample applications for various drivers
- **bsp\include:**
  - Contains the application interface header files for all the modules

# Directory Structure Description contd…

- **bsp\src\audio:**
  - Generic audio driver to stream data to/fro from application to actual audio transport stream drivers like McASP
- **bsp\src\board:**
  - List of on-board devices
  - Board auto-detect
  - Special board level programming
- **bsp\src\common:**
  - Trace functions
  - OS abstraction layer, Data types
  - Heap management like BSS memory and descriptor memory
  - Common utility functions like link list, queue etc…

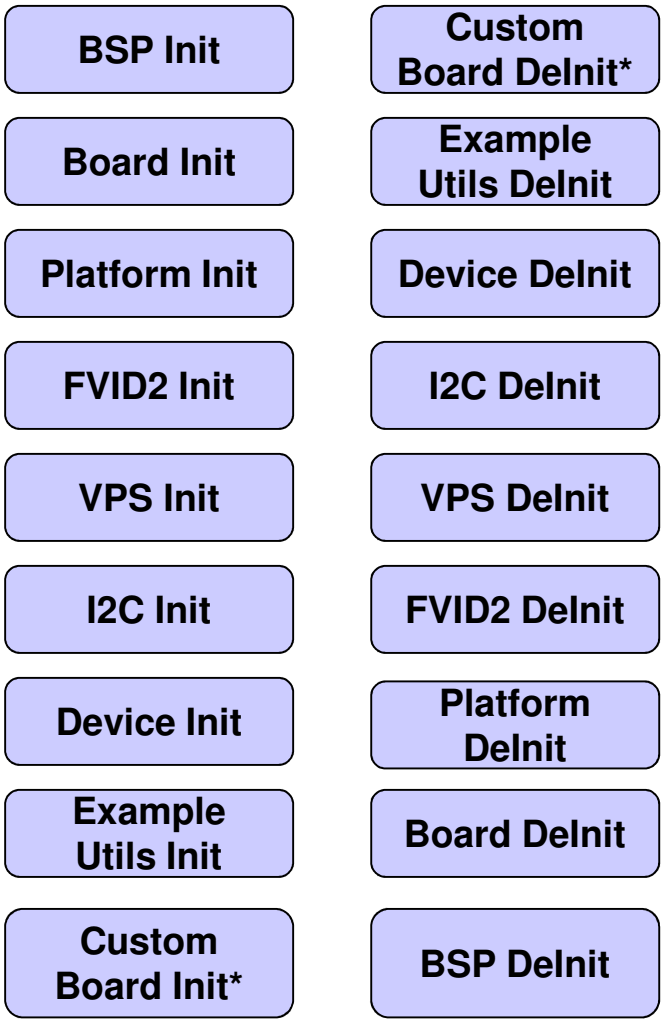
# Directory Structure Description contd…

- **bsp\src\devices:**
  - All on-board device drivers like video encoders, video decoders and sensors
- **bsp\src\fvid2:**
  - FVID2 driver API and driver level interface
- **bsp\src\i2c:**
  - I2C driver files
- **bsp\src\mcasp:**
  - McASP driver files
- **bsp\src\mcspi:**
  - McSPI driver files

# Directory Structure Description contd…

- **bsp\src\platforms:**
  - Top level directory for all supported platforms
- **bsp\src\uart:**
  - UART driver files
- **bsp\src\vps:**
  - Video driver package containing VIP, VPE, ISS and DSS drivers including FVID2 drivers, core drivers and HAL layer

# BSP Package Init/Deinit Sequence



# Init Deinit Sequence

- When using build without board dependent devices like in simulator or QT, device init and deinit shall not be called and I2C init and deinit need not be called
- Example utils init and deinit is an optional call in case customers are using their own applications without any reference to the example utils function. But they shall be called for building example applications provided by this package
- *Custom Board Init and deinit – This could be used by the customers to perform any init/deinit sequence as per their board requirement

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# BSP Common/Utils

- This module is the BSP level common utils and functions used by all the modules in the package. The init function of this module should be called first before calling any other module init function.
- This module contains the following
  - Basic data types
  - Trace and print functions
  - OS abstraction layer
  - BSP configurations
  - Generic utils
    - Heap management – Descriptor and BSS (global variables) heap. Frame buffer heap is maintained by the application level utility
    - Link list and queue functions

# Board Module

- This module takes care of all board specific configurations. This module internally depends on the device I2C read write APIs to detect board and configure board devices
- This module supports the following features and functionalities
  - Auto detection of board. Also supports manual override mode for custom boards support
  - Determining the base board and daughter card revisions
  - Defines the list of on-board devices present in a particular board
    - Each device in this list have information on which I2C bus it is connected to, I2C address and the SOC driver it is connected to
  - Board level power on/off, mux and switch configurations
  - Addition of custom boards is done by adding a device list table
  - Dependent Modules
    - Device – for I2C read/write APIs to detect board and configure board devices
    - Platform
  - BSP Common/Utils

# Platform Module

- This module takes care of platform specific configurations like
  - PRCM and clock control
  - PLL configuration
  - Default pin mux configuration
  - Chip ID
  - CPU revision identification
  - Dependent Modules
    - BSP Common/Utils

# FVID2 Module

- This module provides two set of functions
  - FVID2 APIs for the application
  - FVID2 driver manager APIs for the drivers to register and unregister the driver ops
  - For more details on FVID2 interface see **FVID2 Section**
- Dependent Modules
  - BSP Common/Utils

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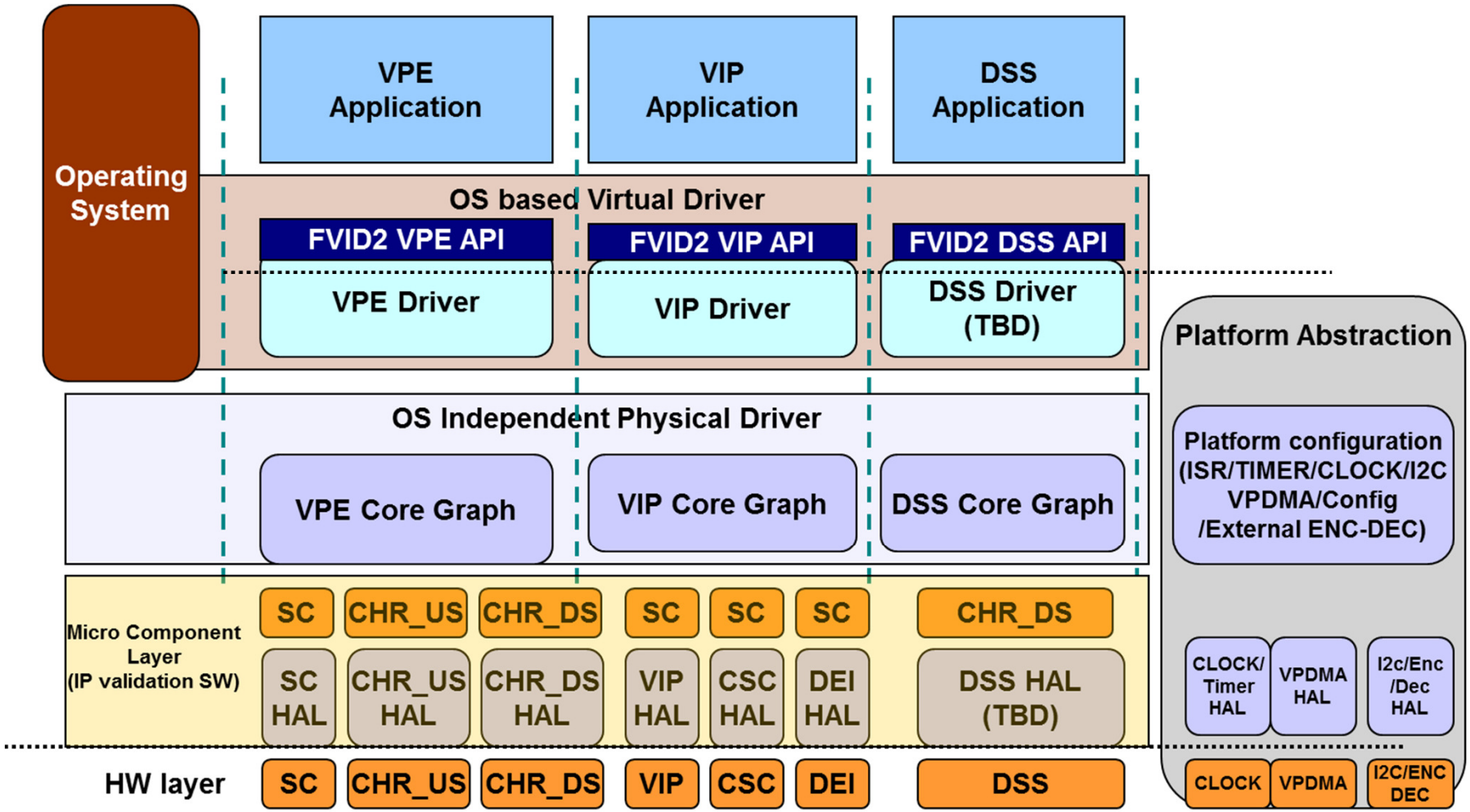
# TDAxx Video Drivers Architecture



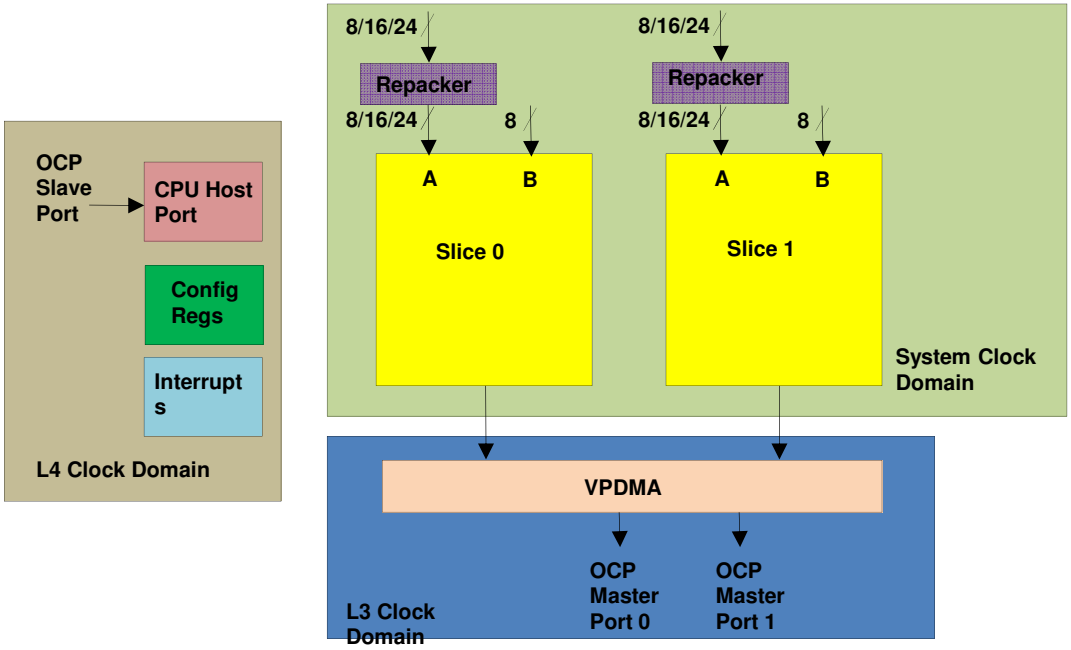
# Contd..

- The Video Driver stack on SysBIOS consists of:
  - OS-independent layers
  - OS-dependent layers
- OS-independent layers
  - The goal of the OS-independent layers is to enable maximum reuse across multiple software and functions:
    - As part of OS-specific driver software
    - To create independent test cases for verification & validation of the IP (AVV & DV)
    - To create simple tools/utilities for programming the IP
  - OS-Independent layers consists of
    - HAL (Hardware Abstraction Layer)
      - » Abstracts individual IPs and provides interfaces to program the IPs:
    - Core layer:
      - » Shields the driver layer from specifics of HALs and descriptor configuration

# Contd..

- OS-Dependent Layers
  - The OS-dependent layers shall provide drivers and interfaces to applications by making use of the OS-specific features such as synchronization, queuing interrupt handling etc.:
- Drivers: VIP, VPE, ISS and DSS drivers shall utilize OS features and provide a user-friendly interface to applications for usage of the hardware. The responsibilities include:
  - Queuing of input requests
  - De-queuing of completed requests
  - Allocation and freeing of resources (if applicable)
- Interfaces
  - FVID2 interface: Generic interface for using the drivers
  - Platform interface: SoC specific functionality
  - Board interface: Board-specific functionality
  - Decoder/Encoder interfaces: Interfaces to use different decoders or encoders

# VIP Sub-system Block



# VIP Block

- Vayu Supports 3 VIP Block with two ports Port A and Port B
  - VIP1/ VIP2 parser can operate as one 8/16/24 bit input port (Port A) or  two 8-bit ports (Port A, Port B).
  - VIP3 parser can operate as 16 bit input port (Port A)
- Separate pixel clock and framing signals for each port
- Each VIP block has two slices : VIP0 S0, VIP0 S1
- VIP Block is used to capture video data from external video sources like video decoders or sensors
- Typical Vayu system can be used for capture from four Mpixel imagers (1280x800) resolution at 30 FPS

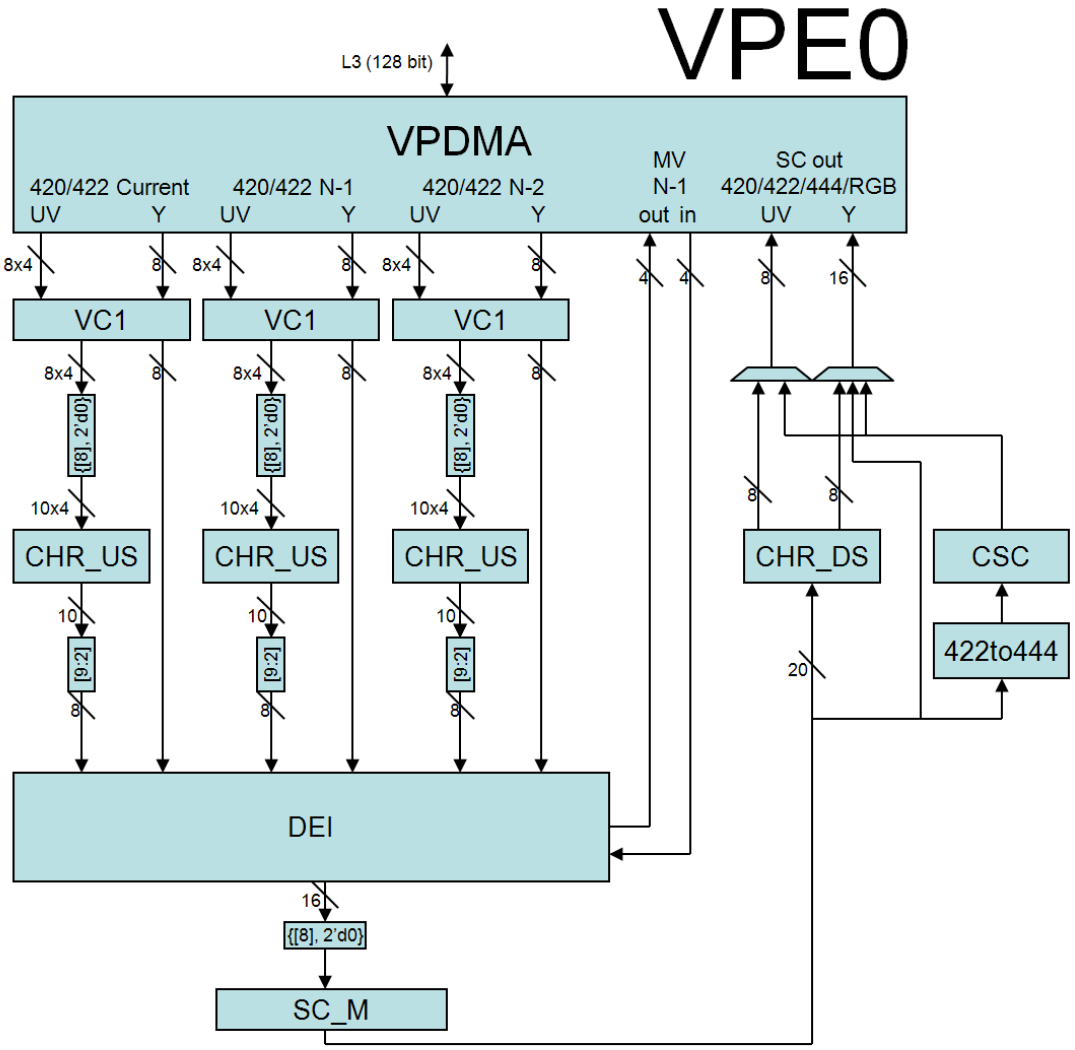
# VIP Features

- Format conversion
  - Inputs: YUV422I, YUV444, RGB888
  - Outputs: YUV422I, YUV420SP (Uses CHR_DS), YUV422SP, RGB888 (Uses CSC)
- Supports optional scaling from 1/8x to 2048 pixels, only down scaling supported
- Supports optional color space conversion
  - YUV to RGB color space conversion using CSC block
- Supports optional chroma downsampler
  - YUV422I to YUV420SP conversion using CHR_DS
- Supports up to 165 MHz clock (includes blanking)
- Video Interface width
  - 8/16/24 bit mode
  - Combination: PortA 8-bit and PortB 8-bit or PortA 16 or 24-bit

# Contd..

- Supports Embedded (BT.656/BT.1120 16/24b, BT.656 8b) or discrete (BT.601 style) sync
- Video Interface Mode
  - Discrete Sync
    - Single Channel non multiplexed mode with HSYNC and VBLK as control signals
    - Single Channel non multiplexed mode with HSYNC and VSYNC as control signals
    - Single Channel non multiplexed mode with AVID and VBLK as control signals
    - Single Channel non multiplexed mode with AVID and VSYNC as control signals
  - Embedded Sync
    - Single Channel non multiplexed mode
    - Multi-Channel pixel or line multiplexed mode

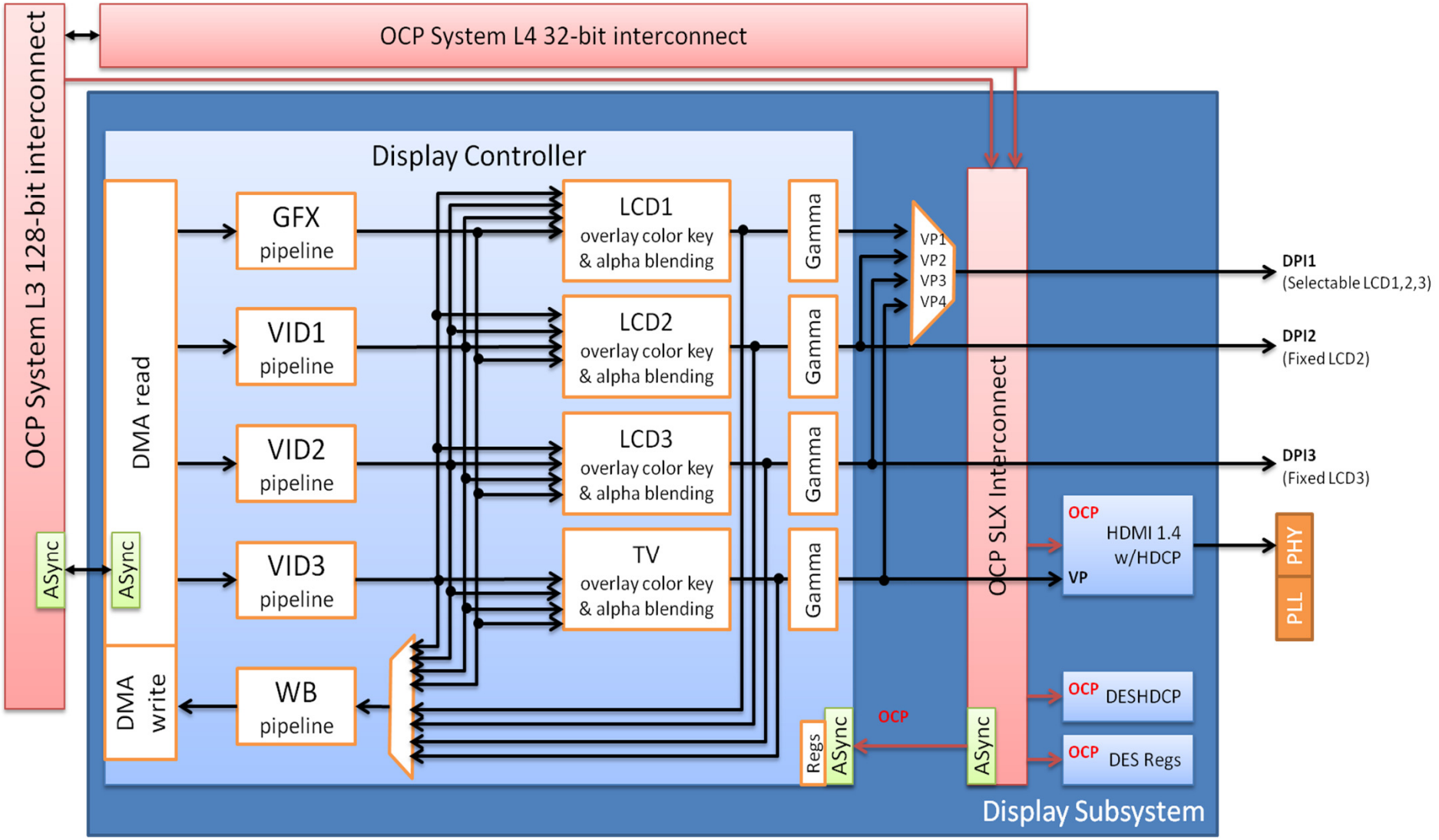
# VPE Block Diagram



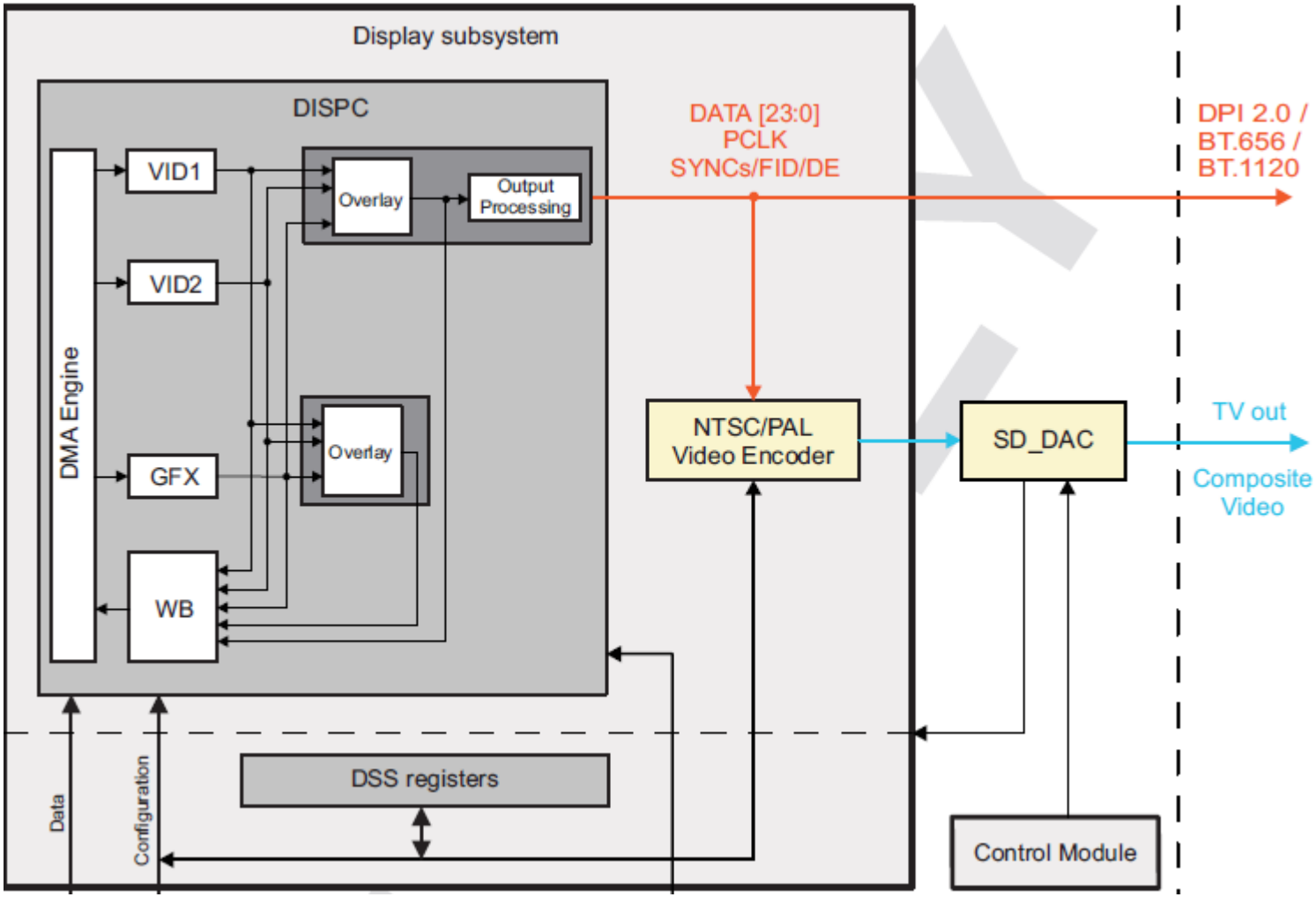
# VPE Features

- Format conversion
  - Inputs: YUV422I, YUV420SP (Uses CHR_US), YUV422SP
  - Outputs: YUV422I, YUV420SP (Uses CHR_DS), YUV422SP, RGB888 (Uses CSC), YUV444I
- Deinterlacing (interlaced to progressive)
  - 4 field motion based algorithm
  - up to two 1080i video sources
  - DEI can be bypassed in case of progressive input
- Scaling from 1/8x to 2048 pixels
- Color space conversion
  - YUV to RGB color space conversion using CSC block
- VC-1 Range Mapping and Range Reduction
- Supports up to 304 MHz clock
- Tiled (2D) input/output

# DSS Block Diagram for TDA2xx



# DSS Block Diagram for TDA3xx



# DSS Features for TDA2xx

- 4 Pipelines (3 Video and 1 Graphics)
- Write Back pipeline
- On the Fly Scaling (1/4x to 8x)
- On the Fly Color space Conversion
- Format Conversion
- 4 Overlay managers :
- Z-Order : App can set the Ordering of layers
- Transparency Color keys : Source and destination(can only be used with RGB and BITMAP formats)
- Alpha Blending : Global Alpha blending and pixel level alpha blending

# DSS Features for TDA3xx

- 3 Pipelines (2 Video and 1 Graphics)
- One Write Back pipeline with region based WB support.
- On the Fly Scaling (1/4x to 8x)
- On the Fly Color space Conversion
- Format Conversion
- 2 Overlay managers : One DPI output and One SD-Output
- Z-Order : App can set the Ordering of layers
- Transparency Color keys : Source and destination(can only be used with RGB and BITMAP formats)
- Alpha Blending : Global Alpha blending and pixel level alpha blending

# McSPI

- The MCSPI is a master/slave synchronous serial bus.
- There are four separate MCSPI modules (SPI1,SPI2, SPI3, and SPI4) in the device.
- All these four modules support up to four external devices (four chip selects) and are able to work as both master and slave.
- McSPI Features
  - Wide selection of SPI word lengths, ranging from 4 to 32 bits
  - Up to four master channels, or single channel in slave mode
  - Master multichannel mode:
    - Full duplex/half duplex
    - Transmit-only/receive-only/transmit-and-receive modes
    - Flexible input/output (I/O) port controls per channel
    - Programmable clock granularity
    - SPI configuration per channel. This means, clock definition, polarity enabling and word width

# McSPI Cont..

- Single interrupt line for multiple interrupt source events
- Power management through wake-up capabilities
- Enable the addition of a programmable start-bit for SPI transfer per channel (start-bit mode)
- Supports start-bit write command
- Supports start-bit pause and break sequence
- Programmable timing control between chip select and external clock generation
- Built-in FIFO available for a single channel

# UART

- The UART is a simple L4 slave peripheral that utilizes the DMA_SYSTEM or EDMA for data transfer or IRQ polling via CPU.
- There are 10 UART modules in the device. Only one UART supports IrDA features
- Each UART can be used for configuration and data exchange with a number of external peripheral devices or interprocessor communication between devices
- Features
  - 16C750 compatibility
  - 64-byte FIFO buffer for receiver and 64-byte FIFO for transmitter
  - Programmable interrupt trigger levels for FIFOs
  - Baud generation based on programmable divisors N (where N = 1…16,384) operating from a fixed

# McASP

- The McASP functions as a general-purpose audio serial port optimized to the requirements of various audio applications.
- The McASP modules can operate in both transmit and receive modes
- The McASP is useful for time- division multiplexed (TDM) stream, Inter-IC Sound (I2S) protocols reception and transmission as well as for an intercomponent digital audio interface transmission (DIT).
- The device have integrated 8 McASP modules (McASP1-McASP8) with
  - McASP1 and McASP2 modules supporting 16 channels with independent TX/RX clock/sync domain
  - McASP3 through McASP8 modules supporting 4 channels with independent TX/RX clock/sync domain
  - The McASP1 is instantiated in IPU power domain
  - McASP2 through McASP8 are part of the L4_PER2 peripheral power domain

# McASP Features

- Two modules (McASP1 and McASP2) supporting up to 16 channels each and independent TX/RX clock/sync domains.
- Six modules (McASP3, McASP4, McASP5, McASP6, McASP7 and McASP8) supporting up to 4 channels each and unified clock/sync domain.
- Independent serializer for each AXRx channel of each McASPx module.
- Independent transmit and receive modules, each includes:
  - Programmable clock and frame sync generator.
  - TDM streams from 2 to 32, and 384 time slots.
- Two independent clock generator modules for transmit and receive.
- Each of the Rx and Tx interrupts is propagated to different host processors via the device Interrupt Crossbar

# I2C

- Device contains five multimaster high-speed (HS) inter-integrated circuit (I2C) controllers
- Each of I2C instance provides an interface between a local host (LH), such as a digital signal processor (DSP), and any I2C-bus-compatible device.
- Each multimaster HS I2C controller can be configured to act like a slave or master I2C-compatible device.
- Features
  - Compliant with Philips I2C specification version 2.1
  - Supports a standard mode (up to 100 kbps) and fast mode (up to 400 kbps)
  - Supports HS mode for transfer up to 3.4 Mbps (only for I2C3, I2C4 and I2C5)
  - 7-bit and 10-bit device addressing modes

# I2C Features Cont..

- Multimaster transmitter/slave receiver mode
- Multimaster receiver/slave transmitter mode
- Combined master transmit/receive and receive/transmit mode
- Built-in configurable FIFOs (8, 16, 32, 64 bytes) for buffered read or write
- Module enable/disable capability
- Programmable multislave channel (responds to four separate addresses)
- Programmable clock generation

# Questions ???