Vision SDK

(v03.01.00)

Frequently Asked Questions (FAQs)

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1 Frequently Asked Questions

1.1 Hardware Board Related FAQs

Q. I selected a use-case and it hangs during initialization
Make sure you are running the SCV use-case on SCV hardware setup and LVDS use-case on LVDS hardware setup. For LVDS hardware use 12V and 7A supply only.
Q. Even after following all the steps I see a incorrect / distorted image on the LCD ?
The issue could be with the CPLD programming on the Vision Application Board. Contact TI local support for reprogramming the CPLD image. The CPLD controls the how the sensor data lines are routed to the VIP port of the SoC. By default CPLD is programmed for the SCV use-case.
Q. Sometimes I see a message "LCD not connected" on the UART console after running the use-case but I see normal display on the LCD
Ignore this message, the software / hardware is falsely reporting LCD is not connected.
Q. LVDS use-case init hangs on first try after power-cycle
Make sure all Sensors are connected as mentioned in earlier section. For LVDS hardware use 12V and 7A supply only.
Q. Sometimes LVDS setup hangs during use-case initialization second time after power-cycle
Suspecting this to be a board connectivity issue. Tighten the application / deserializer boards, Power cycle and retry. For LVDS hardware use 12V and 7A supply only.
Q. After CCS reload without power-cycle LVDS setup hangs during use-case initialization
Suspecting this to be a board connectivity issue. Power cycle, reset the board and retry.
Q. Sometimes when connecting to A15 via CCS we get a message "Router sub-path could not be accessed"
Power cycle, reset the board and JTAG emulator and retry.
Q. I select the LCD demo but I see only colors/color bar no display , logs show proper numbers
Please verify the LCD selected, is it 7" or 10". If its wrongly selected it LCD runs the default test.
Q. Sometimes application does not come to main menu after reloading from CCS
Power cycle before reloading application
Q. I selected a use-case and it displays green or blue color screen instead of video display on LCD
Please ensure you have selected proper display using 's' (setting option), Display

settings.
Q. On TDA3xx EVM my network application doesn't work when I enable FATFS through FATFS_PROC_TO_USE.
On TDA3xx due to pin mux configuration conflicts (same pins shared by SD and Ethernet), the SD and Ethernet can't be used simultaneously. To use Ethernet after NDK_PROC_TO_USE is set to, 'FATFS_PROC_TO_USE=none' should be also set and vice versa. The autorules_footer_cfg.mk makes sure the above is taken care. User should not override this configuration.
Q. When I use AR0140_TIDA00262 cameras on TDA3X/TDA2PX the image colors look unnatural and have purple cast.

If the AR0140_TIDA00262 camera modules are connected to UB964 revision 3 chip, then there is one line downshift is observed in the captured frame. To encounter the problem the bayer pattern should be changed from 'SYSTEM_DF_BAYER_GRBG' to 'SYSTEM_DF_BAYER_BGGR' in the "IssSensor_AR0140_TIDA_Init()" function defined in the \vision_sdk\apps\src\rtos\iss\src\sensor\ar0140\iss_sensor_ar0140.c file.
Change
info->dataFormat = SYSTEM_DF_BAYER_GRBG;
to
info->dataFormat = SYSTEM_DF_BAYER_BGGR;

Q. TDA3XX EVM:The ISS capture doesn't work with the UB960 EVM with 25 MHz crystal.
The CSI2 PHY clock should be set to 750 MHz. Pl. change the CSI PHY clock from 800 MHz to 750 MHz in '\vision_sdk\apps\src\rtos\iss\src\sensor\iss_sensor_tda3xx.c' file for either TIDA/IMI camera modules.

1.2 Stereo run related FAQs

Q: Output of the stereo usecase is noisy, what can be done?
Ans: Ensure you have calibrated stereo sensors for the unit that you have. Stereo algorithm works on right and left images captured from stereo sensors and calculates disparities. If cameras are not calibrated the entire output won't be a correct depth map.
Q: When I connect mini USB to USB to my PC, I don't see anything on TeraTerm/HyperTerminal
Ans: Most likely you have missed installing FDTI chip drivers refer section 2.2.1

1.3 Build, install, load, run related FAQs

Q. My build is failing when I use gmake –s –j depend. I see wired folder not found error even if folder path is present .
Please verify which gmake is used. You need to point to xdc gmake , Run which gmake for git bash / where gmake for cmd.
Q. How do I speed up build and load time ?
Refer VisionSDK_UserGuide_BuildSystem.pdf on tips to reduce build time.
Q. How can I change build option from release to debug for a processor core?

In file **\vision_sdk\apps\configs\$(MAKECONFIG)\cfg.mk**, there is an option to set build type for each processor core. For ex: For DSP1, PROFILE_c66xdsp_1 can be set as release as debug.
Q. While building linux I see the error IPU1 is not included in build which is needed?
For Linux build primary core is ipu2/ipu1. In this release we have primary core as IPU2, thus the scripts throw it as error. This can be ignored
Q. I am using Windows 7 and when I build I get errors no permission to generate batch file?
Please check all the steps to build are followed , Try running as administrator . Even if the issue exists there may be specific settings set for the PC. There would be some makefile changes to be done. CACLS $(DEST_ROOT)/maketemp_configuro_cmd_$(CORE).bat /E /P Everyone:F To be replaced by ICACLS $(DEST_ROOT)/maketemp_configuro_cmd_$(CORE).bat /grant Administrator:(OI)(CI)F This is to be changed in rules_m4.mk rules_a15.mk rules_66.mk rules_arp32.mk
Q. Can the version of tools or other components be changed? If yes, how?
Please check with the support team if this release can work with versions other than the ones present in the release package. If yes, then component install path can be controlled via the file \vision_sdk\tools_path.mk. Paths for several tools and components used are provided in this file.
Q. Is Linux based build supported?
Linux based build can be supported, but it needs linux based compiler tools (GCC, M4, DSP, EVE cgtools) and XDC to be installed. Two installer packages are for released - one for windows with windows compiler tools and other for linux with linux compiler tools. Make sure to install the appropriate one depending on the machine you wish to compile on.
Q. In Surround View Demo I don't see proper display, whereas video from sensor shows proper data.
Yes , This issue is observed if previous Surround view demo calibration tables are not written completely to qspi memory. You have to erase table from the qspi memory and recalibrate . Option is available runtime in the same demo.
Q. Is there any script to automate loading and running of cores via CCS
Yes, this is possible via CCS based debug server scripting (DSS). Refer to a sample script file located at \vision_sdk\build\rtos\scripts\launch_visionsdk_tdaNxx.js. Refer to comments in this file for customizing as required.
Q. How to ensure alignment when sharing data structures across cores
When data structures are accessed across cores, it's a good practice to ensure all elements are 32-bit – this ensures structures are 32-bit aligned. Alternately when defining data-structure programmer can take care of alignment by declaring 32-bit first, then 16-bit and later 8-bit data. This will ensure no packing.
Q. How to enable Dual A15 (SMP Bios) – TDA2xx ONLY

Set the build option "DUAL_A15_SMP_BIOS=yes" in **\vision_sdk\apps\configs\$(MAKECONFIG)\cfg.mk** to enable both A15 cores of TDA2xx. Refer Refer VisionSDK_UserGuide_BuildSystem.pdf for more details about this option.
Q. OCMC Ram1 heap is not usable in VISION_SDK by default. How it can be enabled
OCMC_CBUF based use-cases use OCMC_RAM1. When these are used, OCMC_RAM1 cannot be used as HEAP as the CBUF usage can destroy heap related data structures. If user wants to use, OCMC_RAM1 as heap, define UTILS_MEM_HEAP_OCMC_SIZE in utils_mem_cfg.h In that case, CBUF-based use-cases (SRV/DeWarp/Sub-FrameCopy) cannot be used.
Q. EVE self-branch instruction block - EVE1_VECS (Important Note – refer mem_segment_definition_512mb.xs)
In SBL, EVE self-branch instruction is inserted @ 0x80000000 if no AppImage for EVE (if EVE is not enabled in the build). This could overwrite the code/data loaded at 0x80000000. So Reserve a small memory block in the beginning of the DDR @0x8000 0000 for EVE self-branch instruction if no AppImage for EVE. If EVE is enabled, then the EVE VECS/DATA/CODE is placed @0x8000 0000, and hence we did not observe any issue. If EVE is disabled, then also DO NOT removes this EVE1_VECS section @0x80000000, which is used by SBL to place EVE self-branch instruction.
Q. AppImage flashing is failing for qspi in default configuration.
In default configuration the imae size is ~40MB. Whereas QSPI has support till 32 MB. In case of SRV usecase the LUT occupies some space. Hence disable unwanted usecase and rebuils
Q. VSDK when build on VM with -j option gets stuck some times.
Use –jn option instead of –j where 'n' is the number of PC cores used to build the executable.
Q. VSDK build fails on Windows with "vision_sdk_PATH" value not found.
Set the path as below and then try the build. set Path=C:\PROCESSOR_SDK_RADAR_<version>\ti_components\os_tools\windows\xdctools_<version>_core;C:\windows\system32;C:\windows;C:\windows\System32\Wbem;C:\windows\System32\WindowsPowerShell\v1.0\

1.4 PM and resource related FAQs

Q. How to Enable/Disable CPUIDLE functionality. How is it advantages using CPUIDLE.
CPUIDLE functionality helps in power saving, When the core is executing idle instruction the ip are put in sleep/Standby mode.
Q. I see the core is halted at IDLE/WFI instruction every time when I load the

symbols in release mode
This is because of Power Management and CPUIDLE enabled in Vision SDK. The core executes idle/wfi instruction when idle. It wakes up on interrupt and hence debug the code in release mode becomes difficult. When binaries are built in debug mode CPUIDLE is disabled.
Q. How can I debug when binaries are in release mode. The application doesn't step when in WFI/IDLE looks like hung state.
If in case debugging release mode binary is essential then, CPUIDLE needs to be disables for eliminating the WFI/IDLE issue, CPU_IDLE_ENABLED=no in \vision_sdk\apps\configs\$(MAKECONFIG)\cfg.mk file in vision_sdk
Q. A15 is a debug binary but still is see WFI instruction hit when we pause.
In case of Vision Sdk, A15 is build as debug binary; The PROFILE used to build is Release so PM will be included. The Build Profile needs to debug to remove CPU_IDLE from the build.
Q. Does Vision Sdk use GP timer in their configurations which are those?
Yes, Vision Sdk does use the timers. Timer 1,2 5,6 9,11 are been used by SDK .
Q. Interrupts used by temperature utils
Vision Sdk uses interrupt no 61 for temperature Temperature Sensor Interrupt. A hot and cold events are triggered to the assigned interrupt number. Temperature hot and cold threshold can be set using api in utils_temperature.h
Q. Timers used by CPU cores to allow CPU load and BIOS Tick when CPUs are powered down
Vision SDK uses GP Timers for the cores (2 per ISA) to use a proxies for the BIOS Tick and TimeStampProvider. To know which timers are used for which CPU core on which device refer the VisionSDK_DevelopmentGuide Chapter 7.1.2
Q. The TDA2xx Vision SDK log on typing 'p' shows the following message: [IPU1-0] Name | Bus (mV) | Res (mOhm) | Shunt (uV) | Current (mA) | Power (mW) [IPU1-0] ---------- [IPU1-0] UTILS_PRCM_STATS: Reading the regulator data failed [IPU1-0] UTILS_PRCM_STATS: PM INA226 Power Read Failed !!
This is a harmless message which basically means the power measurement from TDA2xx to access INA226 registers has failed. If your intention is to measure power from TDA2xx, kindly make sure that the TDA2xx EVM is modified with the changes mentioned in VisionSDK_UserGuide_TDA2xx.pdf
Q. Where can I get the vision SDK demo clips
Vision SDK demo clips are available at https://cdds.ext.ti.com/ematrix/common/emxNavigator.jsp?objectId=28670.42872.30602.25095

2 Revision History

Version	Date	Revision History
1.0	25 Aug 2016	Initial Version. Collated FAQs from different user guides in a single file
1.1	2nd Nov 2016	Updated for Release 2.11.00
1.2	7th Feb 2017	Updated for Release 2.12.00
1.3	29th Mar 2017	Updated for Release 2.12.02
1.4	28th June	Updated for Release 3.0.0
1.5	16th Oct 2017	Updated for Release 3.01.0

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