

CP3CN17

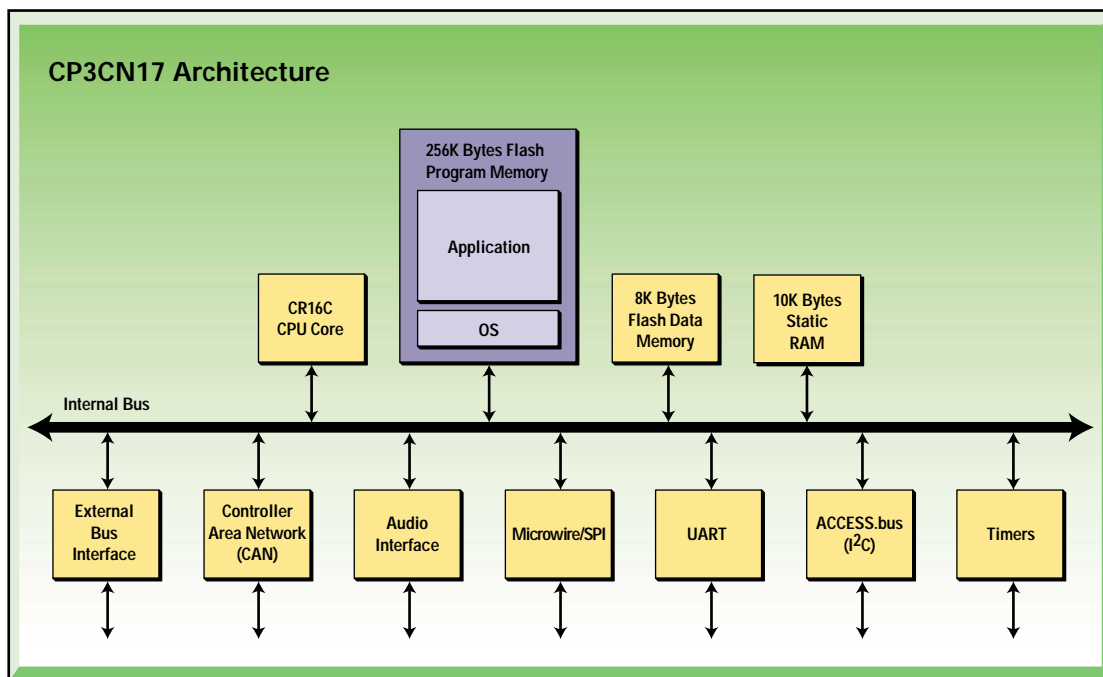
CAN-Enabled Connectivity Processor

The CP3CN17 connectivity processor combines a powerful RISC core with on-chip SRAM and Flash memory for high computing bandwidth, hardware communications peripherals for high I/O bandwidth, and an external bus for system expandability.

On-chip communications peripherals include: CAN controller, ACCESS.bus, Microwire/Plus, SPI, UART, and Advanced Audio Interface (AAI). Addi-

tional on-chip peripherals include DMA controller, PCM/CSVD conversion module, Timing and Watchdog Unit, Versatile Timer Unit, Multi-Function Timer, and Multi-Input Wakeup.

The low voltage and advanced power-saving modes achieve new design points in the trade-off between battery size and operating time for industrial and automotive applications.



CP3CN17 Features

High Integration for Industrial and Automotive Applications

CPU Features

- Fully static RISC processor core, capable of operating from 0 to 24 MHz with zero wait/hold states
- Minimum 41.2 ns instruction cycle time with a 24-MHz internal clock frequency, based on a 12-MHz external input
- 30 independently vectored peripheral interrupts

On-Chip Memory

- 256K bytes reprogrammable Flash program memory
- 8K bytes Flash data memory
- 10K bytes of static RAM data memory
- Addresses up to 8M bytes of external memory

Broad Range of Hardware Communications Peripherals

- Full CAN interface with 15 message buffers conforming to CAN specification 2.0B active
- I²C-compatible ACCESS.bus synchronous serial bus

- 8/16-bit SPI, Microwire/Plus serial interface
- Universal Asynchronous Receiver/Transmitter (UART)
- Advanced Audio Interface (AAI) to connect to external 8/13-bit PCM Codecs as well as to ISDN-Controllers through the IOM-2 interface (slave only)
- PCM/CVSD converter supporting one bidirectional audio connection

General-Purpose Hardware Peripherals

- Dual 16-bit Multi-Function Timer
- Versatile Timer Unit with four subsystems (VTU)
- Four-channel DMA controller
- Timing and Watchdog Unit

Industry-Proven Connectivity Solutions

Flexible I/O

- Up to 37 general-purpose I/O pins (shared with on-chip peripheral I/O)
- Programmable I/O pin characteristics: TRI-STATE output, push-pull output, weak pull-up input, high-impedance input
- Schmitt triggers on general-purpose I/O inputs
- Multi-Input Wakeup Unit (MIWU)

Extensive Power and Clock Management Support

- On-chip Phase Locked Loop
- Support for multiple clock options
- Dual clock and reset
- Power-down modes

Power Supply

- I/O port operation at 2.5V to 3.3V
- Core logic operation at 2.5V
- On-chip power-on reset

Temperature Range

- -40°C to +85°C (Industrial)

Packages

- CSP-48, LQFP-100

Complete Development Environment

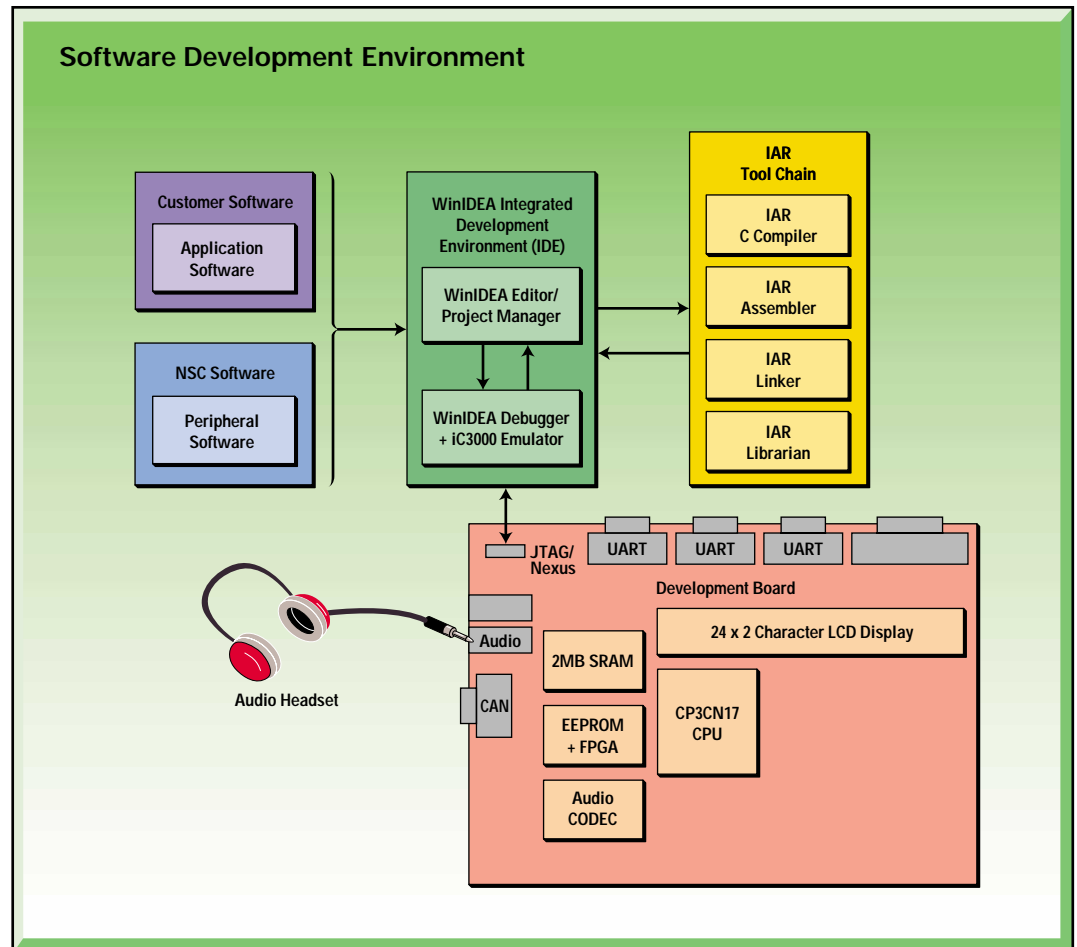
- Pre-integrated hardware and software support for rapid prototyping and production
- Integrated environment
- Project manager
- Multi-file C source editor
- High-level C source debugger
- Comprehensive and integrated technical support

Software Resources

Operating System and Development Tools

The CP3CN17 is backed up by the software resources designers need for rapid time-to-market, including an operating system, peripheral drivers, reference designs, and an integrated development environment.

National Semiconductor offers a complete and industry-proven application development environment for CP3CN17 applications, including the IAR Embedded Workbench, iSYSTEM winIDEA and iC3000 Active Emulator, Development Board, and Peripheral Software.



μC/OS-II Real-Time Operating System

Compact Multi-Tasking Kernel for Embedded Applications

The μC/OS-II real-time kernel is a portable, ROMable, scalable, preemptive real-time, multitasking kernel that provides the following services:

- Semaphores
- Event Flags
- Mutual Exclusion Semaphores (to reduce priority inversions)
- Message Mailboxes
- Message Queues
- Task Management (Create, Delete, Change Priority, Suspend/Resume etc.)
- Fixed-Sized Memory Block Management
- Time Management

The execution time for most of the services provided by the μC/OS-II kernel is both constant and deterministic. This means that execution times do not depend on the number of tasks running in the application. The μC/OS-II kernel is also very fast. For example, the scheduler in μC/OS-II consists of only four simple lines of C. The CR16C's PUSH and POP instructions help to improve OS efficiency because the bulk of a task's context (registers R0..R14) can be saved or restored from its stack in just 2 PUSH instructions or 2 POP instructions, together consuming as little as 40 clock cycles.

The μC/OS-II kernel is written in C, and source code is available. The large user base and long track record have proven its quality and robustness. The implementation of the μC/OS-II kernel on the CR16C devices continues the upward growth path from the previous generation of CR16B devices. This demonstrates National's commitment to introducing new technology, denser integration, and higher performance in the CompactRISC architecture while maintaining software and hardware standards that protect your investment in product development.

Product Selection Guide

Packaging Options Cover Wide Range of Applications

Part Number (NSID)	Speed (MHz)	Temp. Range	Program Flash (kBytes)	Data Flash (kBytes)	SRAM (kBytes)	I/Os	External Address Lines	Package Type
CP3CN17G38	24	-40° to +85°C	256	8	10	40	23	LQFP-100
CP3CN17K38	24	-40° to +85°C	256	8	10	23	0	CSP-48

National Semiconductor provides a comprehensive set of support services. Product information, including sales literature and technical assistance, is available through National's Customer Support Centers.

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(IDD telephone charge to be paid by caller)

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