Software Installation

4

Check the CP3000 area on the National Semiconductor web site (**www.national.com/appinfo/CP3000**) and the Release Notes supplied with the evaluation kit to be sure you are using the latest versions of the software tools.

To install the software, load the evaluation kit CD-ROM, click through the license agreement (if you agree to its terms), then click on the Software Installation button in the Main Navigation Screen. This brings up the view shown below.

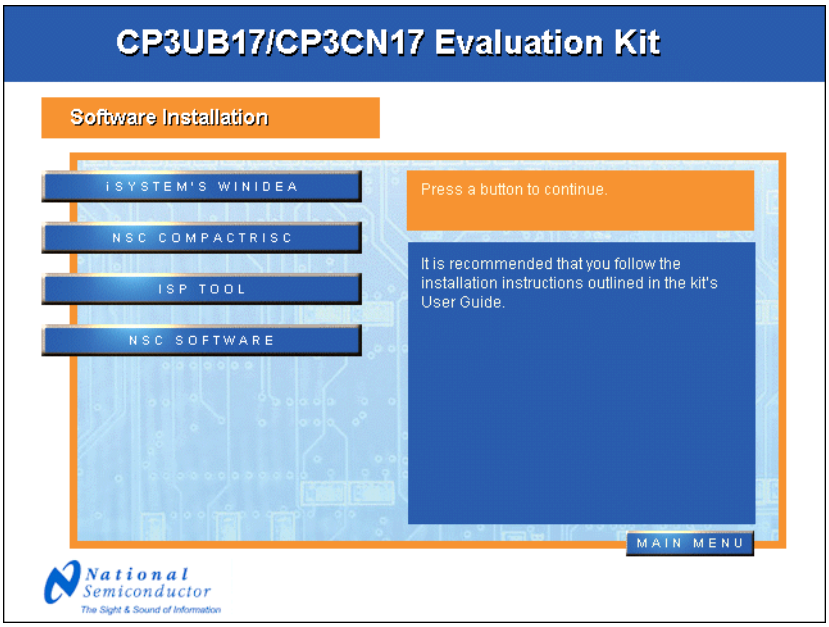

Figure 4-1. Software Installation Screen

Software Installation

Software installation has four main parts, which correspond to the four buttons on the screen shown in Figure 4-1:

- **winIDEA Project Manager and Debugger**—the integrated development environment (IDE) for compiling, downloading, and debugging application programs.
- **NSC CompactRISC**—the C compiler tool chain developed by National Semiconductor from the GNU tools. winIDEA can be configured to call this tool chain for compiling application programs. (Alternatively, winIDEA support is available for a C compiler tool chain from IAR Systems.) A license key is provided in the evaluation kit which is needed to install the NSC tools.
- **ISP Tool**—the CRISP tool for downloading application code to the evaluation board over a serial connection. See the CP3UB17/CP3CN17 ISP and CRISP User's Guide for more information.
- **NSC Software**—application examples and template files for creating new applications. The template files configure winIDEA to call the NSC tool chain. The top-level structure of the NSC software installation is shown in Figure 4-2.

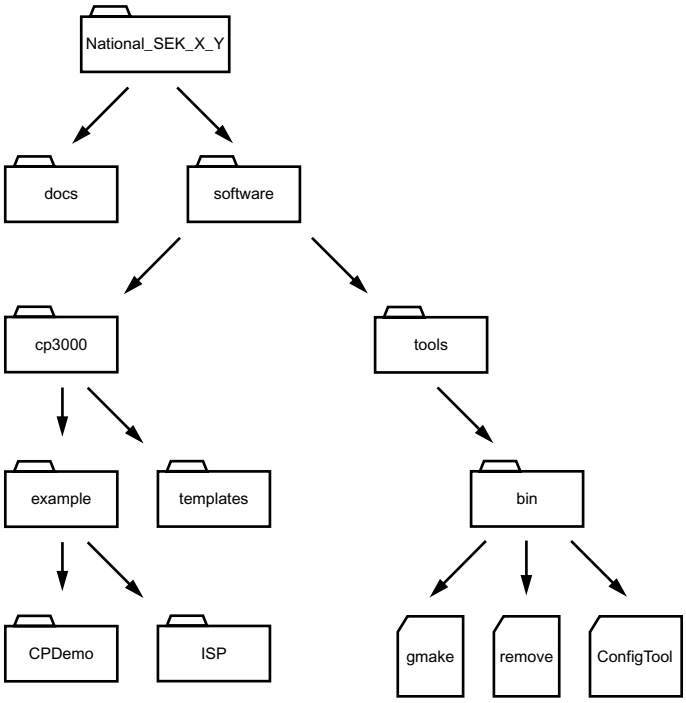

Figure 4-2. Organization of Files Loaded by the NSC Software Installation

The **bin** folder contains these executable files:

- **gmake**—the GNU make utility.
- **remove**—a file deletion utility called by makefiles.
- **ConfigTool**—a utility which defines target configuration settings used during compilation (CPU type, board type, etc.).

The **templates** folder contains winIDEA files which are replicated to create a new project. There are two sets of template files which configure winIDEA to call the NSC tool chain:

- **template_NS.jrf, template_NS.QRF**—template files to compile applications for conventional download using winIDEA.
- **template_NS_ISP.jrf, template_NS_ISP.QRF**—template files to compile applications for download through the In-System Programming (ISP) interface. See the **CP3UB17/CP3CN17 ISP and CRISP User's Guide** for more information about the ISP.

The **example** folder contains the files for the **CPDemo** example program used in this manual and the ISP software described in the **CP3UB17/CP3CN17 ISP and CRISP User's Guide**.

4.1 Program Menu Shortcuts

The software installation adds shortcuts to the Start -> Programs menu. The shortcuts you are likely to use most often are:

- **winIDEA 9.4 -> winIDEA NSC EVB**—enters the winIDEA IDE.
- **CRISP -> CRISP**—enters the CRISP tool.
- **National SEK 1.5 -> Configuration Tool**—initializes macros which control compilation for a specific hardware target configuration. This utility **must** be run before you can compile any application programs.
- **National SEK 1.5 -> CPDemo**—user interface utility for controlling the **CPDemo** application example. This utility runs on the host PC and communicates over a serial connection to the **CPDemo** executable code running on the evaluation board.

Software Installation

Program Menu Shortcuts

Hardware Installation

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Figure 5-1 shows the hardware connections between the host PC and the CP3UB17/CP3CN17 Evaluation Board.

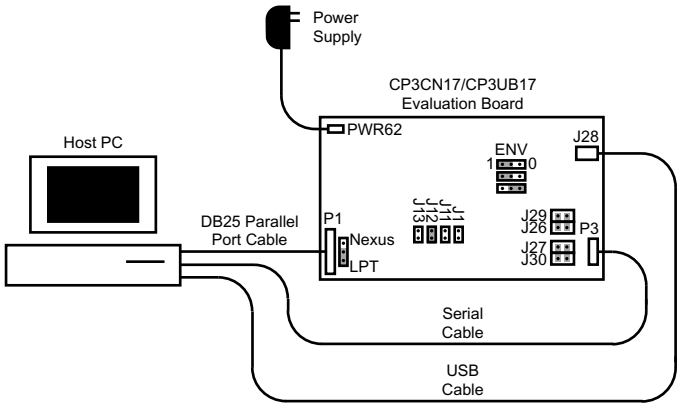

Figure 5-1. Hardware Connections

The following procedure sets up the hardware:

1. **Connect the Parallel Port on the Host PC to the Evaluation Board.** The cable is plugged into the connector for the LPT1 parallel port on the host PC and connector P1 on the evaluation board.
2. **Connect a Serial Port on the Host PC to the Evaluation Board.** The cable is plugged into a connector for the COM1 or COM2 serial port on the host PC and connector P3 on the evaluation board.

3. **Connect a USB Port on the Host PC to the Evaluation Board.** The cable is plugged into a connector for a USB port on the host PC and connector J28 on the evaluation board.
4. **Configure the Clock Source Jumpers.** The clock source is controlled by jumpers J1, J11, J12, and J13, as described in Table 12-7. Select the oscillator module by installing jumper J12. Leave jumper positions J1, J11, and J13 empty.
5. **Configure the ENV Jumpers.** Configure the board for ERE mode, in which the on-chip flash memory and external flash memory are enabled. Jumpers J15 (ENV0) and J16 (ENV1) are installed on the 1 side of the jumper block. Jumper J17 (ENV2) is installed on the 0 side.
6. **Enable the Parallel Port Interface.** The connection used for downloading applications to the evaluation board can be the parallel port interface on connector J1 or the Nexus/JTAG interface on connector JP1. Enable the parallel port interface by installing jumper J25 on the LPT side of the jumper block.
7. **Apply Power to the Evaluation Board.** Plug the power supply into an AC outlet, and plug the power cable into connector PWR62 on the evaluation board.