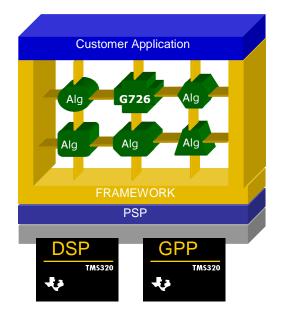


- Compliant with the eXpressDSP<sup>™</sup>
   Algorithm Interface Standard (XDAIS)
- Compliant with the eXpressDSP Multimedia (XDM) interface
- Mixed C and C64x+ assembly code implementation
- Bit-exact with all ITU G726 test sequences
- Supports both ELF and COFF formats



## description

The ITU G.726 converts A-law or U-law PCM input samples sampled at 8 KHz sampling rate into a 40, 32, 24, or 16 kbps ADPCM bit-stream

- Encoder Compresses the A-law or U-law PCM input samples into a 40, 32, 24, or 16 kbps ADPCM bit-stream
- Decoder expands 40, 32, 24, or 16 kbps bitstream into A-law or U-law PCM samples
- Bit Compliant with ITU-T G.726 specifications
- Optimized for TI C64x+ DSP
- C callable interface for encoder and decoder
- Re-entrant multi channel implementation
- Implementation compliant to eXpressDSP<sup>™</sup>
- Compliant with the eXpressDSP Multimedia (XDM) interface
- Supports RTP Special packing format as defined in RFC3551 and Linear packing format
- Fully interruptible Code
- This release supports both Big and Little Endian Mode of operation
- Efficient Scratch memory management with reduced stack requirements
- The implementation support run time data buffers relocation and constant relocation
- Fully validated on TMS320C6455 DSK, using CCS version 4.2 with the code generation tools version 7.2.0A10197



Supports both ELF and COFF formats

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# **Summary of performance**

Table 1. Configuration Table

CONFIGURATION	ID
Encoder – 40 kbps rate, Little Endian	G726_001
Decoder – 40 kbps rate, Little Endian	G726_002
Full Duplex – 40 kbps rate, Little Endian	G726_003
Encoder – 40 kbps rate, Big Endian	G726_004
Decoder – 40 kbps rate, Big Endian	G726_005
Full Duplex – 40 kbps rate, Big Endian	G726_006

Table 2. Cycles Information – TMS320C6455 DSK (COFF Library)

CONFIGURATION ID	PERFORMANCE STATISTICS (IN MEGACYCLES/SEC) <sup>1</sup>		
	AVERAGE <sup>2</sup>	PEAK <sup>2</sup>	
G726_001	1.72	1.75	
G726_002	2.04	2.04	
G726_003	3.760	3.79	
G726_004	1.72	1.76	
G726_005	2.04	2.04	
G726_006	3.76	3.80	

Measured with frame size= 80 samples (10ms)

Table 3. Cycles Information – TMS320C6455 DSK (ELF Library)

CONFIGURATION ID	PERFORMANCE STATISTICS (IN MEGACYCLES/SEC) <sup>1</sup>		
	AVERAGE <sup>2</sup>	PEAK <sup>2</sup>	
G726_001	1.70	1.74	
G726_002	2.03	2.04	
G726_003	3.730	3.78	
G726_004	1.70	1.74	



<sup>&</sup>lt;sup>2</sup> Measured with program and data memory, stack and I/O buffers in L2. L1P and L1D cache Invalidation done for every frame Measured with 32K cache at L1P, 32K cache at L1D. Both program and data placed at L2 configured as SRAM



G726_005	2.03	2.04
G726_006	3.73	3.78

Measured with frame size= 80 samples (10ms)

Table 4. Memory Statistics - Generated with Code Generation Tools Version 7.2.0A10197 (COFF Library)

	MEMORY STATISTICS <sup>3</sup>				
CONFIGURATION	PROGRAM DATA MEMORY			TOTAL	
	MEMORY	INTERNAL	EXTERNAL	STACK	TOTAL
G726_001	5.47	0	1.347	0.086	6.903
G726_002	6.88	0	1.347	0.094	8.321
G726_003	11.13	0	1.461	0.094	12.685
G726_004	5.47	0	1.347	0.086	6.903
G726_005	6.88	0	1.347	0.094	8.321
G726_006	11.13	0	1.461	0.094	12.685

<sup>&</sup>lt;sup>3</sup> All memory requirements are expressed in kilobytes (1 kilobyte = 1024 bytes)

Table 5. Memory Statistics - Generated with Code Generation Tools Version 7.2.0A10197 (ELF Library)

		MEMORY STATISTICS <sup>3</sup>			
CONFIGURATION	PROGRAM	DATA MEMORY			TOTAL
	MEMORY	INTERNAL	EXTERNAL	STACK	TOTAL
G726_001	5.47	1.347	0	0.086	6.903
G726_002	6.88	1.347	0	0.094	8.321
G726_003	11.13	1.461	0	0.094	12.685
G726_004	5.47	1.347	0	0.086	6.903
G726_005	6.88	1.347	0	0.094	8.321
G726_006	11.13	1.461	0	0.094	12.685

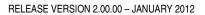
All memory requirements are expressed in kilobytes (1 kilobyte = 1024 bytes)

Table 6. Internal Data Memory Split-up

	DATA MEMORY – INTERNAL <sup>4</sup>		
CONFIGURATION	SHARED		INSTANCE <sup>5</sup>
	CONSTANTS	SCRATCH	INSTANCE
G726_001	1.078	0.156	0.113

<sup>&</sup>lt;sup>2</sup> Measured with program and data memory, stack and I/O buffers in L2. L1P and L1D cache Invalidation done for every frame Measured with 32K cache at L1P, 32K cache at L1D. Both program and data placed at L2 configured as SRAM

# G726 ON TMS320C64X+





G726_002	1.078	0.156	0.113
G726_003	1.078	0.156	0.227
G726_004	1.078	0.156	0.113
G726_005	1.078	0.156	0.113
G726_006	1.078	0.156	0.227

<sup>&</sup>lt;sup>4</sup> All memory requirements are expressed in kilobytes (1 kilobyte = 1024 bytes) <sup>5</sup> Does not include I/O buffers



#### notes

Total Data Memory for N Non-Pre-Emptive Instances =
 Constants + Runtime Tables + Scratch + N\*(Instance + I/O buffers + Stack)

Total Data Memory for N Pre-Emptive Instances =

Constants + Runtime Tables + N\*(Instance + I/O buffers + Stack + Scratch)

#### references

ITU Recommendation G.726

## glossary

Constants Elements that go into .const memory section

Scratch Memory space that can be reused across different instances of the algorithm

Shared Sum of Constants and Scratch

Instance Persistent-Memory that contains persistent information - allocated for each

instance of the algorithm

# acronyms

ITU International Telecommunication Union

ITU-T Telecommunication Standardization Sector of ITU



# **REVISION HISTORY**

**Scope:** Applicable updates to the G726 on C6455 have been incorporated.

DATE	VERSION	ADDITIONS/CHANGES/DELETIONS
31 <sup>st</sup> Mar 2006	1.0	Initial Version
08 <sup>th</sup> February 2007	1.1	Updated the label and release date
June 2008	1.11	Updated with xDM1.0 APIs
August 2009	1.11.01	Patch release to resolve noise output during high amplitude inputs
January 2012	2.00.00	Added ELF support

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