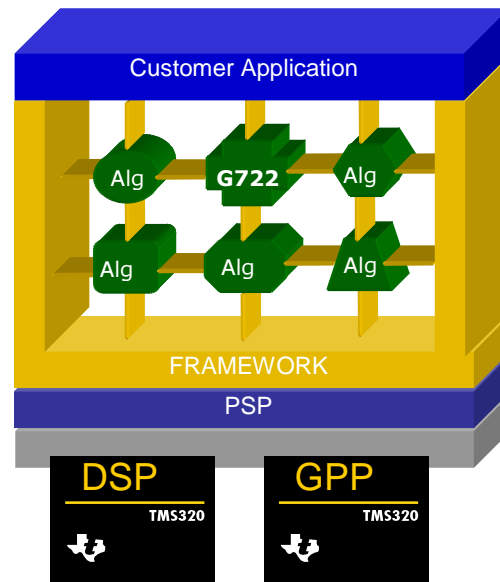




- This is an implementation of ITU G.722.1 recommendations on TI C64X+ processor
- Mixed C and C64X+ assembly code implementation
- eXpressDSP™ compliant
- Bit-exact with all ITU G.722.1 test sequences
- Validated on TMS320C6455 DSK with Code Composer Studio 4.2 and Code Generation Tools version 7.2.0A10197
- Supports both ELF and COFF formats



## description

The ITU G.722.1 is the codec for wideband and super wideband speech. It is a low complexity encoder and decoder that may be used for 7KHz or 14KHz bandwidth audio signals. Encoder takes linear PCM input signals (14, 15, or 16 bit 2's compliment) sampled at 16/32KHz sampling rate and encodes using Modulated Lapped Transform (MLT) technology to give 24kbps or 32kbps bit rates for wideband speech and 24kbps or 32kbps or 48kbps for super wideband speech. Decoder expands encoded bit stream into linear PCM samples.

- Bit Compliant with ITU-T G.722.1 specifications
- Optimized for TI C64X+ DSP
- C callable interface for encoder and decoder
- Re-entrant multi channel implementation
- Implementation Compatible with TI XDAIS rules
- Fully interruptible Code
- Relocatable tables
- This release supports Big Endian and Little Endian Mode of operation
- Efficient Scratch memory management with reduced stack requirements
- The implementation support run time data buffers relocation & table relocation
- The implementation supports both ELF and COFF formats
- Fully validated on TMS320C6455 DSK, using CCS version 4.2 with the code generation tools version 7.2.0A10197



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



Copyright © 2012, Texas Instruments Incorporated



Summary of performance

Table 1. Configuration Table

CONFIGURATION	ID
Encoder ,Big Endian	G722_001
Decoder, Big Endian	G722_002
Full Duplex, Big Endian	G722_003
Encoder ,Little Endian	G722_004
Decoder, Little Endian	G722_005
Full Duplex, Little Endian	G722_006

Table 2. Cycles Information (wideband) – TMS320C6455 DSK (COFF Library)

CONFIGURATION ID	PERFORMANCE STATISTICS (IN MEGACYCLES/SEC) <sup>1</sup>	
	AVERAGE	PEAK
G722_001	1.15	1.23
G722_002	1.45	1.56
G722_003	2.60	2.79
G722_004	1.14	1.22
G722_005	1.44	1.54
G722_006	2.58	2.76

<sup>1</sup> Measured with frame size= 320 samples (20ms)

Measured with 32K L1P configured as cache, 32K L1D configured as cache , with all program and data in L2 Memory configured as SRAM. Both L1P and L1D are invalidated before each encoder and decoder execution

Table 3. Cycles Information (super wideband) – TMS320C6455 DSK (COFF Library)

CONFIGURATION ID	PERFORMANCE STATISTICS (IN MEGACYCLES/SEC) <sup>1</sup>	
	AVERAGE	PEAK
G722_001	2.16	2.37
G722_002	2.75	2.87
G722_003	4.91	5.24
G722_004	2.15	2.36



G722_005	2.71	2.83
G722_006	4.86	5.19

Measured with frame size= 640 samples (20ms)

Measured with 32K L1P configured as cache, 32K L1D configured as cache , with all program and data in L2 Memory configured as SRAM. Both L1P and L1D are invalidated before each encoder and decoder execution

**Table 4. Cycles Information (wideband) – TMS320C6455 DSK (ELF Library)**

CONFIGURATION ID	PERFORMANCE STATISTICS (IN MEGACYCLES/SEC) <sup>1</sup>	
	AVERAGE	PEAK
G722_001	1.15	1.23
G722_002	1.42	1.53
G722_003	2.57	2.76
G722_004	1.14	1.22
G722_005	1.41	1.52
G722_006	2.55	2.74

<sup>1</sup> Measured with frame size= 320 samples (20ms)

Measured with 32K L1P configured as cache, 32K L1D configured as cache , with all program and data in L2 Memory configured as SRAM. Both L1P and L1D are invalidated before each encoder and decoder execution

**Table 5. Cycles Information (super wideband) – TMS320C6455 DSK (ELF Library)**

CONFIGURATION ID	PERFORMANCE STATISTICS (IN MEGACYCLES/SEC) <sup>1</sup>	
	AVERAGE	PEAK
G722_001	2.16	2.37
G722_002	2.69	2.81
G722_003	4.85	5.18
G722_004	2.15	2.36
G722_005	2.66	2.78
G722_006	4.81	5.14

<sup>1</sup> Measured with frame size= 640 samples (20ms)

Measured with 32K L1P configured as cache, 32K L1D configured as cache , with all program and data in L2 Memory configured as SRAM. Both L1P and L1D are invalidated before each encoder and decoder execution

**Table 6. Memory Statistics - Generated with Code Generation Tools Version 7.2.0A10197 (COFF Library)**

CONFIGURATION	MEMORY STATISTICS <sup>2</sup>		
	PROGRAM	DATA MEMORY	TOTAL



	MEMORY	INTERNAL	EXTERNAL	STACK	
G722_001	10.5	36.24	0	0.25	46.99
G722_002	9.94	36.88	0	0.34	47.16
G722_003	18.6	38.17	0	0.34	57.11
G722_004	10.38	36.24	0	0.25	46.87
G722_005	9.94	36.88	0	0.34	47.16
G722_006	18.48	38.17	0	0.34	56.99

<sup>2</sup> All memory requirements are expressed in kilobytes (1 kilobyte = 1024 8-bit bytes).

**Table 7. Memory Statistics - Generated with Code Generation Tools Version 7.2.0A10197 (ELF Library)**

CONFIGURATION	MEMORY STATISTICS <sup>2</sup>				
	PROGRAM MEMORY	DATA MEMORY			TOTAL
		INTERNAL	EXTERNAL	STACK	
G722_001	10.5	36.24	0	0.25	46.99
G722_002	9.94	36.88	0	0.34	47.16
G722_003	18.6	38.17	0	0.34	57.11
G722_004	10.34	36.24	0	0.25	46.83
G722_005	9.94	36.88	0	0.34	47.16
G722_006	18.44	38.17	0	0.34	56.95

<sup>2</sup> All memory requirements are expressed in kilobytes (1 kilobyte = 1024 8-bit bytes).

**Table 8. Internal Data Memory Split-up**

CONFIGURATION	DATA MEMORY – INTERNAL <sup>2</sup>		
	SHARED		INSTANCE <sup>3</sup>
	CONSTANTS	SCRATCH	
G722_001	28.7	6.25	1.29
G722_002	28.7	6.25	1.93
G722_003	28.7	6.25	3.22
G722_004	28.7	6.25	1.29
G722_005	28.7	6.25	1.93
G722_006	28.7	6.25	3.22

<sup>3</sup> All memory requirements are expressed in kilobytes (1 kilobyte = 1024 8-bit bytes)

<sup>4</sup> Does not include I/O buffers



## notes

- Total Data Memory for N *Non-Pre-Emptive* Instances =  
Constants + Runtime Tables + Scratch + N\*(Instance + I/O buffers + Stack)
- Total Data Memory for N *Pre-Emptive* Instances =  
Constants + Runtime Tables + N\*(Instance + I/O buffers + Stack + Scratch)

## references

ITU Recommendation G.722

## glossary

Constants	Elements that go into .const memory section
Scratch	Memory space that can be reused across different instances of the algorithm
Shared	Sum of Constants and Scratch
Instance	Persistent-Memory that contains persistent information - allocated for each instance of the algorithm

## acronyms

ITU	International Telecommunication Union
ITU-T	Telecommunication Standardization Sector of ITU



**REVISION HISTORY**

**Scope:** Applicable updates to the G722 on C6455 have been incorporated.

DATE	VERSION	ADDITIONS/CHANGES/DELETIONS
08 FEB 2005	1.0	Initial Version
07 MAR 2005	1.1	Updated after re-release
10 NOV 2006	1.00	Adding xDM APIs.
MAR 2009	1.11.00	Big endian support
JUNE 2009	1.12.00	ITU-T Appendix IV (plc) support
January 2012	2.00.00	Added ELF support

## **IMPORTANT NOTICE**

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

**Copyright © 2012 Texas Instruments Incorporated. All rights reserved.**

Information in this document is subject to change without notice. Texas Instruments may have pending patent applications, trademarks, copyrights, or other intellectual property rights covering matter in this document. The furnishing of this document is given for usage with Texas Instruments products only and does not give you any license to the intellectual property that might be contained within this document. Texas Instruments makes no implied or expressed warranties in this document and is not responsible for the products based from this document. This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Texas Instruments assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.