H.264 Baseline Profile Decoder (2.00) on C64x+

FEATURES

- **eXpressDSP™ Digital Media (XDM 1.0 IVIDDEC2) interface compliant**
- **Validated on the DM644x EVM**
- **Up to level 3.0 features of the baseline profile (BP) supported**
- **Progressive frame type picture decoding supported**
- **Multiple slices and multiple reference frames supported**
- **CAVLC decoding supported**
- **Intra-prediction and inter-prediction modes supported**
- **Up to 16 MV per MB supported**
- **Frame size being non-multiples of 16 through frame cropping supported**
- **Frame width of the range 32 to 720 pixels supported**
- **Byte-stream syntax and NAL unit format for the input bit stream supported**
- **Long term reference frames supported**
- **Gaps in the frame_num**
- **Decoding of streams with IPCM coded macroblocks supported**
- **Skipping of non-reference pictures supported**
- **Configurable delay for display of frames supported**
- **Error resiliency supported**
- **Error concealment supported**
- **Outputs are available in YUV 420 planar and 422 interleaved little endian formats**
- **Tested for compliance with JM version 12.2 reference decoder**
- **ASO and FMO error concealment feature supported**
- **Redundant slices supported**
- **Parsing of Supplemental Enhancement Information(SEI) and Video Usability Information (VUI) supported**
- **Adaptive reference picture marking supported**
- **Reference picture list reordering supported**
- **All resolutions up to D1 (PAL and NTSC) including CIF and QCIF supported**
- **This codec can be used on any of TI's C64x+ based platforms such as DM644x, DM648, DM643x, OMAP35xx, and their derivatives.**

DESCRIPTION

H.264 (from ITU-T, also called as H.264/AVC) is a popular video coding algorithm enabling high quality multimedia services on a limited bandwidth network. H.264 standard defines several profiles and levels which specify restrictions on the bit stream and hence limits the capabilities needed to decode the bit streams. Each profile specifies a subset of algorithmic features and limits that all decoders conforming to that profile may support. Each level specifies a set of limits on the values that may be taken by the syntax elements in the profile.

PRODUCT PREVIEW

Performance Summary

This section describes performance of the H.264 Baseline Profile Decoder on DM644x EVM.

Table 1. Configuration Table

CONFIGURATION	ID
Level 1.0 Baseline Profile	H264_DEC_001
Level 2.0 Baseline Profile	H264_DEC_002
Level 3.0 Baseline Profile	H264_DEC_003

Table 2. Cycles Information – Profiled on DM644x EVM With Code Generation Tools Version 6.0.8

CONFIGURATION ID	PERFORMANCE STATISTICS(1) (MEGA CYCLES PER SECOND)(2)		
	TEST DESCRIPTION	AVERAGE(3)	PEAK(4)
H264_DEC_001	foreman_i_p1.264, YUV422ILE, 4MV, QCIF(176x144), @ 300kbps	30	33
	FM1_BT_B.264,YUV422ILE, FMO with all types of slice-groups, QCIF(176x144), 270@ kbps	60	88
	FM1_FT_D.264,YUV422ILE,40% non-FMO, non-ASO frames and 60% ASO/FMO frames, QCIF(176x144), @ 187 kbps	44	63
	FM2_SVA_A.264,YUV422ILE, ASO/FMO frames, QCIF(176x144), @ 151kbps	59	64
	FM3_FT_A.264,YUV422ILE,ASO/FMO present, QCIF(176x144), @241 kbps	50	76
H264_DEC_002	Cities_CIF_500Kbps.264, YUV422ILE, 4MV, CIF(352x288), @ 500 kbps	88	109
	traffic_multiple_slice_aso.264,YUV422ILE, only ASO present on all frames, CIF(352x288), @ 560 kbps	95	121
H264_DEC_003	foreman_vga_1mbps_100f.264, YUV422ILE, 4MV, VGA(640x480), @ 1 mbps	203	282
	fire_30frames_2_Mbps.264, YUV422ILE, 16MV, D1(720x480), @ 2 mbps	292	311
	sheilds_720x480_1MV_1_5Mbps.264 , YUV422ILE, 1MV, D1 (720x480) @ 1.5Mbps	220	336

(1) Average and peak MCPS measurements can vary by +/-5%.
(2) Measured with program memory, stack, I/O buffers in external memory, 32K-bytes L1P Cache, 64K-bytes L1D Data memory, 16K-bytes L1D Cache, 64K-bytes L2 Cache, DDR speed at 162 MHz, and CPU speed at 486 MHz
(3) Based on average number of cycles per frame @ 30 frames per second (fps)
(4) Based on worst case cycles per frame @ 30 fps

Table 3. Memory Statistics - Generated With Code Generation Tools Version 6.0.8

CONFIGURATION ID	MEMORY STATISTICS(1)				TOTAL
	PROGRAM MEMORY	DATA MEMORY			
		INTERNAL	EXTERNAL	STACK	
H264_DEC_001	472	62	1290	12	1836
H264_DEC_002	472	62	4048	12	4596
H264_DEC_003	472	62	6280	12	6826

(1) All memory requirements are expressed in kilobytes (1K-byte = 1024 bytes) and there could be a variation of approximately 1-5% in values

Table 4. Internal Data Memory Split-Up

CONFIGURATION ID	DATA MEMORY - INTERNAL (1)		
	SHARED		INSTANCE (2)
	CONSTANTS	SCRATCH	
H264_DEC_001	0	62	0
H264_DEC_002	0	62	0
H264_DEC_003	0	62	0

(1) Internal memory refers to L1D RAM. All memory requirements are expressed in kilobytes and there could be a variation of approximately 1-5% in values.
(2) I/O buffers not included. Some of the instance memory buffers could be scratch.

Table 5. External Data Memory Split-Up

CONFIGURATION ID	DATA MEMORY-EXTERNAL (1)		
	CONSTANT	FAR	PERSISTENT
H264_DEC_001	5	10	1275
H264_DEC_002	5	10	4033
H264_DEC_003	5	10	6265

(1) All memory requirements are expressed in kilobytes (1K-byte = 1024 bytes) and there could be a variation of approximately 1-5% in values

Notes

- Evaluation version performance values may be higher than the values specified in the performance table.
- Display buffer for YUV422 interleaved format is 810K-bytes for 625 SD format (720 x 576)
- Input buffer to algorithm is assumed to have at least one encoded frame data. Otherwise, the application must provide CPB buffer size amount of valid data to the algorithm. For a specific level, the CPB size could be referred from the standard.
- Memory Configuration
  - L1P: 32K-bytes program cache (32 bytes cache line width, direct mapped cache)
  - L1D: 64K-bytes data memory and 16K-bytes data cache (64 bytes cache line width, 2-way set associative cache)
  - L2: 64K-bytes cache (128 bytes cache line width, 4-way set associative cache)
- The performances obtained in Table 2 are sensitive to algorithm code placement. See the sample linker file provided in the test application setup for algorithm code placement. This is used for profiling in Table 2.
- The algorithm uses 4 QDMA channels. Channels 0, 2, and 3 each require up to a maximum of 8 linked transfers. Channel 1 requires 24 PARAM sets to perform 24 linked transfers. The algorithm uses DMAN3 interface for logical allocation of these channels.
- Total data memory for N non pre-emptive instances = Constants + Runtime Tables + Scratch + N*(Instance + I/O buffers + Stack)
- Total data memory for N pre-emptive instances = Constants + Runtime Tables + N*(Instance + I/O buffers + Stack + Scratch)

References

- ISO/IEC 14496-10:2005 (E) Rec. - Information technology – Coding of audio-visual objects – H.264 (E) ITU-T Recommendation
- *H.264 Baseline Profile Decoder on C64x+ User's Guide* (literature number: SPRUEA1C)

Glossary

Term	Description
Constants	Elements that go into .const memory section
Scratch	Memory space that can be reused across different instances of the algorithm
Shared	Sum of Constants and Scratch
Instance	Persistent-memory that contains persistent information - allocated for each instance of the algorithm

Acronyms

Acronym/Abbreviation	Description
625SD	Level 3.0 maximum resolution format size 720 x 576
CIF	Common Intermediate Format
CPB	Coded Picture Buffer
D1	SDTV image resolution (720x480)
DMA	Direct Memory Access
DMAN3	DMA Manager
EVM	Evaluation module
QCIF	Quarter Common Intermediate Format
QDMA	Quick Direct Memory Access
SDTV	Standard Definition Television
SEI	Supplemental Enhancement Information
VGA	Video Graphics Array (640 x 480 resolution)
VUI	Video Usability Information
XDM	eXpressDSP Digital Media

Revision History

This data sheet revision history highlights the changes made to the SPRS315B codec specific data sheet to make it SPRS315C.

Table 6. Revision History of H264 Decoder on C64x+

SECTION	ADDITIONS/MODIFICATIONS/DELETIONS
Global	Modified Code Generation Tools version to 6.0.8
Section 1	Features: • Updated XDM version • Added the following: – Error resiliency supported – All resolutions up to D1 (PAL and NTSC) including CIF and QCIF supported • Added supported platforms
Table 2	Cycles Information: • Added the last row to Test Description column • Updated Average and Peak values
Table 3	Memory Statistics: • Updated Program Memory, Internal, External, Stack, and Total values
Table 4	Internal Data Memory Split-up: • Updated Scratch values
Table 5	Added table for External Data Memory Split-up

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