MPEG4 Advanced Simple Profile Decoder (v02.00.00) on DM365

FEATURES

- **eXpressDSP Digital Media (XDM1.0 IVIDDEC2) interface compliant**
- **Validated on DM365 EVM with MVL 5.0**
- **Up to Level 5 features of the Advanced Simple Profile (ASP) supported**
- **GMC Toolset not supported**
- **H.263 baseline profile (profile0), levels 10, 20, 30 and 45 supported**
- **Progressive and Interlace type picture decoding supported**
- **Multiple packet decoding supported**
- **Short video header supported**
- **AC/DC prediction supported**
- **4MV and UMV modes supported**
- **Motion compensation pixel accuracy up to Quarter-pel.**
- **Both MPEG4 and H.263 style quantization is supported**
- **Error Resilience(ER) tools (DP, RVLC, HEC and re-sync marker) up to D1 resolution supported**
- **Resolutions up to 1080P(1920 x 1088) supported**
- **A minimum resolution of 48 x 48 supported**
- **YUV420 output format with Chroma interleaved for the frames supported**
- **Performs predictor based temporal error concealment on erroneous frames and reports the type of error occurred**
- **Uses configurable frame display delay for out of order display**

DESCRIPTION

MPEG4 (from ISO/IEC) is a popular video coding algorithm enabling high quality multimedia services on a limited bandwidth network. MPEG4 standard defines several profiles and levels, which specify restrictions on the bit stream, and hence limits the capabilities needed to decode the bit-streams. This project is developed using Code Composer Studio version 3.3.81.6 and using the code generation tools version 4.1.4.

PRODUCT PREVIEW

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Copyright © 2009, Texas Instruments Incorporated

Performance Summary

This section describes the performance of the MPEG4 Advanced Simple Profile Decoder on DM365 EVM.

Performance Measurement Procedure

- Measured with program memory and I/O buffers in external memory, I/D cache enabled, ARM @297 MHz, DDR @ 243 MHz, Monta Vista Linux 5.0
- Linux is used to measure the performance numbers in this Datasheet.
- The process time is measured across algActivate/process/algDeactivate function call using gettimeofday() utility of linux
- NFS File system is used as an environment in performance measurement.

Table 1. Configuration Table

CONFIGURATION	ID
MPEG4 Advanced Simple Profile levels up to 5	MPEG4DEC_02

Table 2. Cycles Information for Streams Encoded Using MJCP

INPUT NAME	RESOLUTION	PERFORMANCE STATISTICS (MEGA CYCLES PER SECOND)					
		AVERAGE			PEAK		
		ARM926 PER FRAME	DECODE PER FRAME	FPS	ARM926 PER FRAME	DECODE PER FRAME	FPS
akiyo_cif_mjcp_512kbps.m4v	cif@30fps, 484 kbps	0.188	1.005	248.324	0.258	1.127	75.143
spykids_d1_mjcp_4mbps.m4v	D1@30fps, 3.8 mbps	0.222	3.636	76.899	0.292	3.713	75.143
CREW_720p_mjcp_8mbps_25fps.m4v	720p @25fps, 7.6 mbps	0.288	9.562	30.133	0.356	9.726	29.625

Table 3. Cycles Information for Streams Encoded Using HDVICP

INPUT NAME	RESOLUTION	PERFORMANCE STATISTICS (MEGA CYCLES PER SECOND)					
		AVERAGE			PEAK		
		ARM926 PER FRAME	DECODE PER FRAME	FPS	ARM926 PER FRAME	DECODE PER FRAME	FPS
akiyo_cif_hdvicp_512kbps.m4v	cif@30fps, 512 kbps	0.189	1.004	249.314	0.265	1.11	218.055
spykids_d1_hdvicp_4mbps.m4v	D1@30fps, 3.9mbps	0.222	3.455	80.665	0.296	3.557	77.555
CREW_720p_hdvicp_8mbps_25fps.m4v	720p @25fps, 7.7 mbps	0.29	9.121	31.536	0.401	9.304	30.921

Table 4. Cycles Information for Generic Test Cases

INPUT NAME	RESOLUTION	PERFORMANCE STATISTICS (MEGA CYCLES PER SECOND)					
		AVERAGE			PEAK		
		ARM926 PER FRAME	DECODE PER FRAME	FPS	ARM926 PER FRAME	DECODE PER FRAME	FPS
foreman_cif_30fps_sp_512kbps.m4v	cif@30fps, 600 kbps	0.189	1.152	220.848	0.271	1.244	206.441
mobile_calendar.m4v	PAL@25fps, 8.5 mbps	0.246	5.198	54.529	0.307	5.547	51.203
crew_720p_8Mb_SP_90fm_30fps.m4v	720p @30fps, 7.7 mbps	0.293	9.471	30.399	0.371	9.828	29.356
crew_720p_8Mb_ASP_90fm_30fps.m4v	720p @30fps, 7.5 mbps	0.311	28.665	28.665	0.399	11.339	25.489
tractor_1080p_25fps_sp_13mbps.m4v	1080p@30fps,13mbps	0.421	21.980	13.254	0.503	23.339	12.499

PRODUCT PREVIEW

Copyright © 2009, Texas Instruments Incorporated

NOTE:

1. These figures depict the load on ARM926 and HDVICP separately. For calculating FPS, both the loads have been added, as these operations happen sequentially.
2. These figures are with cache enabled on ARM926 side.
3. They are measured in standalone mode without actual framework.
4. All numbers are collected (both average and peak) at frame-level processing.
5. The version of the code used to collect these numbers have the following features included:
   a. Interrupt mode of operation – one interrupt signal processing overhead per frame.
   b. Approximate interrupt latency – 2.7uS.
   c. Resetting of vIMCOP and loading of code into HDVICP program memory – once per stream

Table 5. Memory Statistics

CONFIGURATION ID	MEMORY STATISTICS (IN BYTES)					
	PROGRAM MEMORY	DATA MEMORY				TOTAL
		CONSTANT	HEAP		STACK	
			PERSISTENT	SCRATCH		
MPEG4DEC_02	190640	104376	1892512	0	12288	2199816

NOTE:

1. All these memory requirements are for ARM926 decoder library only. They do not include any memory requirements from test application side and input/output buffers for decoding. Stack, heap and code requirements for test-application are additional.
2. Constant memory size requirements include code memory of HDVICP since it forms a constant table on ARM926 before transfer.

Table 6. Internal Data Memory Split-Up

CONFIGURATION ID	DATA MEMORY - HDVICP (IN BYTES)			
	PROGRAM MEMORY (BYTES)	DATA MEMORY (BYTES)	HDVICP BUFFERS	VICP (BYTES)
MPEG4DEC_02	48K	32K	ALL	0

Table 7. DM365 MPEG4 Decoder Usage of Memory via CMEM.

I/O BUFFERS	SIZE IN BYTES
Input Buffer	1024000
Output Buffer	3206016
MEMTABS	**SIZE IN BYTES**
Memtab 0	1280
Memtab 1	1280
Memtab 2	512
Memtab 3	640
Memtab 4	2688
Memtab 5	512
Memtab 6	4224
Memtab 7	103680
Memtab 8	24064
Memtab 9	128
Memtab 10	747648
Memtab 11	319264
Memtab 12	384
Memtab 13	10240

PRODUCT PREVIEW

Copyright © 2009, Texas Instruments Incorporated

Table 7. DM365 MPEG4 Decoder Usage of Memory via CMEM. (continued)

I/O BUFFERS	SIZE IN BYTES
Memtab 14	65792
Memtab 15	30720
Memtab 16	576000
Memtab 17	3456

NOTE:

1. All these memory requirements are for maxWidth and maxHeight of 1920x1088
2. Output Buffer Size mentioned above is for one set of Luma and Chroma output buffer
3. The size of the input buffer should be equal to or greater than one frame data

The following cmem allocations are dependent upon the maxWidth and maxheight and it gives the formula for calculating the size based on the input resolution. The table has numbers for 1080p resolution.

1. Output Buffer = Luma_frameSize_padded + Chroma_frameSize_padded.
2. Memtab 8 = (24 * (mbWidth + 2 + 14) * 2) + (64 * 2 * (mbWidth + 2 + 14)) + 128
3. Memtab 10 = 2 * mbWidth * (mbHeight + 2) * 44 + (mbWidth * (mbHeight + 2))
4. Memtab 16 = (((mbHeight + 2) * (mbWidth + 3) * 16 * 16) * 9/2)
   Where,
   Luma_frameSize_padded = ((maxWidth + 32 + alignment)*(maxHeight+ 32)).
   Chroma_frameSize_padded = Luma_frameSize_padded / 2.
   mbWidth = (maxWidth + 15)/16;
   mbHeight = (maxHeight + 15)/16;

PRODUCT PREVIEW

Copyright © 2009, Texas Instruments Incorporated

Notes

- DMA configuration

Table 8. DMA Configuration

TC Q'S	TC0	TC1	TC2	TC3	TOTAL
Usage	Used by Codec	Used by Codec	Used by Codec	Reserved for System	-
Priority	1	1	1	0	-
EDMA Channels	22	2	6	NA	26
PaRAM Entries	30	5	8	NA	90
QDMA Channels	0	0	0	NA	0

- HDVICP and VICP
  - The entire HDVICP is a video resource and is used by the codec and VICP is not used by the codec
- The HDVICP/EDMA resources are acquired using a generic resource manager known as Framework Component. Please refer user guide for details.
- Code Placement
  - All the algorithm code is placed in external memory. The performance quoted is not sensitive to algorithm code placement.

References

- ISO/IEC 14496-2:2003(E), 'Information Technology – Coding Of Audio-Visual Objects – Part 2: Visual'
- User Guide for MPEG4 Advanced Advanced Simple Profile Decoder (literature number: SPRUGR3)

Glossary

Term	Description
Constants	Elements that go into .const memory section
Scratch	Memory space that can be reused across different instances of the algorithm
Shared	Sum of Constants and Scratch
Instance	Persistent-memory that contains persistent information - allocated for each instance of the algorithm

Acronyms

Acronym	Description
CIF	Common Intermediate Format
D1	720x480 or 720x576 resolutions in progressive scan
720p	1280x720
1080p	1920x1088
DMA	Direct Memory Access
DP	Data-Partition
EVM	Evaluation Module
GMC	Global Motion Compensation
HDVICP	High Definition Video and Imaging Co-Processor sub-system
HEC	Header Extension Code
QCIF	Quarter Common Intermediate Format
QVGA	Quarter Video Graphics Array
RVLC	Reversible Variable Length Coding
SQCIF	Sub Quarter Common Intermediate Format
TCM	Tightly Coupled Memory
UMV	Unrestricted Motion Vectors
VICP	Video and Imaging Co-Processor sub-system
VGA	Video Graphics Array

PRODUCT PREVIEW

Copyright © 2009, Texas Instruments Incorporated

Acronym	Description
XDM	eXpressDSP Digital Media

PRODUCT PREVIEW

Copyright © 2009, Texas Instruments Incorporated

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DLP® Products	www.dlp.com	Broadband	www.ti.com/broadband
DSP	dsp.ti.com	Digital Control	www.ti.com/digitalcontrol
Clocks and Timers	www.ti.com/clocks	Medical	www.ti.com/medical
Interface	interface.ti.com	Military	www.ti.com/military
Logic	logic.ti.com	Optical Networking	www.ti.com/opticalnetwork
Power Mgmt	power.ti.com	Security	www.ti.com/security
Microcontrollers	microcontroller.ti.com	Telephony	www.ti.com/telephony
RFID	www.ti-rfid.com	Video & Imaging	www.ti.com/video
RF/IF and ZigBee® Solutions	www.ti.com/lprf	Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2009, Texas Instruments Incorporated