H.264 Base/Main/High Profile Decoder (v02.00.00) on DM365/DM368

FEATURES

- eXpressDSP™ Digital Media (XDM 1.2 IVIDDEC2) interface compliant
- Validated on DM365 EVM with MVL 5.0
- H.264 Baseline, Main & High Profiles up to level 4.2 compliant (limited to maximum of 1920x1088 frame resolution)
- Progressive, Field, PAFF and MBAFF frame type picture decoding supported
- CAVLC and CABAC decoding supported
- Main Profile features like B-Slice decoding and CABAC supported
- Weighted prediction for motion compensation in both P and B-slices supported
- Transform 8x8 mode, interspersed with transform 4x4 MBs supported
- Parsing and decoding with scaling lists present both in SPS and PPS NAL units supported
- Second chroma qp index offset value present in PPS supported
- All intra-prediction and inter-prediction modes supported
- Up to 16 MV per MB supported
- Both adaptive and sliding window DPB management supported
- Output order conformance using frame bumping process supported
- Uses configurable frame display delay for out of order display
- Multiple slices and multiple reference frames supported
- Supports for low latency call back APIs for low delay applications
- Byte stream NAL unit format for input bit-stream
- Frame/Field based decoding with frame size being multiples of 2 supported
- Field based decoding with frame height being multiple of 4 supported
- Outputs are available in YUV420 interleaved big endian format
- SEI (Supplemental Enhancement Information) and VUI (Video Usability Information) supported
- Performs predictor based spatial and temporal error concealment on erroneous frames and reports the type of error occurred
- Supports closed loop decoding of 1920x1088 streams generated by DM36x H.264 encoder, at 30fps on DM368 432 MHz
- This version of the decoder does not support the following features:
  - Error resilience features such as ASO/FMO and redundant slices
  - Dynamic change in resolution
  - Monochrome format in High Profile

DESCRIPTION

H.264 (from ITU-T, also called as H.264/AVC) is a popular video coding algorithm enabling high quality multimedia services on a limited bandwidth network. H.264 standard defines several profiles and levels which specify restrictions on the bit stream and hence limits the capabilities needed to decode the bit streams. This project is developed using Code Composer Studio version 3.3.81.6 and using the code generation tools version 4.1.3.

PRODUCT PREVIEW

Performance Summary

This section describes the performance of standalone H.264 high profile decoder validated on the DM365 EVM resulting in performance equivalent to 30fps.

Table 1. Configuration Table

CONFIGURATION	ID
H.264 High Profile levels up to 4.2 – Universal decoder Closedloopflag = 0.	H264_DEC_01
H.264 High Profile levels up to 4.2 – Closed loop decoder for decoding Platinum mode streams (PRC OFF, one MV/MB, one reference picture) Closedloopflag = 1	H264_DEC_02

Performance Measurement Procedure

- Measured with program memory and I/O buffers in external memory, I/D cache enabled, Monta Vista® Linux® 5.0, ARM @432 MHz, DDR @ 340 MHz for both the configurations.
- Linux is used to measure the performance numbers in this Datasheet.
- The process time is measured across algActivate/process/algDeactivate function call using gettimeofday() utility of linux.
- NFS File system is used as an environment in performance measurement.
- Performance numbers are measured on linux OS .The performance numbers will be same for CCS version Codec library

Table 2. Cycles Information for Decoder Cofiguration H264_DEC_01

INPUT NAME	PARAMETER	AVERAGE (1)			PEAK (1)		
		ARM926 PER MHz	FRAME DECODE MHZ	FPS	ARM926 PER MHz	FRAME DECODE MHZ	FPS
colorful_toys_cif_5frms_420P_256kbps.264	CIF(352x288) High profile, cabac, IPP , single slice 256kbps, sequence scaling, transform 8X8, single reference frame, 1MV/MB, progressive	0.41	1.32	338.06	1.00	1.95	222.62
D1_football_720x480_384_30fBP_384kbps.264	D1(720x480) Base profile, cavlc, IPP, multislice, 384kbps, single reference frame, upto 4MV/MB, progressive	0.34	3.38	137.35	0.96	3.98	123
720p50_shields_ter_1280x720_420p_hp_lev4_17mbps_4mbps.264	720p (1280x720) High profile, cabac, IPB, multislice, 4mbps, transform 8X8, 5 reference frames, upto 16MV/MB, progressive	0.45	9.14	48	1.81	10.40	43.47
tractor_1920x1080_420p_MP_6mbps.264	1080p (1920x1080) Main profile, cabac, IPP, singleslice, 6mbps, single reference frame, upto 16MV/MB, progressive	0.47	20.06	23.20	1.12	20.60	17.36
foreman_cif_cabac_mult_slice_i_2b_p_interlaced_512kbps.264	CIF(352x288) Main profile, cabac, IPB, multislice, 512kbps, 2 reference frame, upto 16 MV/MB, interlace	0.40	1.89	237.8	0.71	2.14	220.12
hp_d1_cabac_i_2b_p_interlaced_2mbps.264	D1(720x480) Main profile, cabac, IPB, singleslice, 2mbps 2 reference frame, upto 16MV/MB, interlace	0.58	4.36	99.88	0.9	4.70	96.99
parkrun_p1280x720_30fps_420pl_30fr_HP_interlaced_7mbps.264	1280x720 High profile, CAVLC, IPP, multislice, 7mbps, single reference frame, 1MV/MB, interlace	0.96	10.07	45.88	1.47	12.63	32.62
stockholm_i1920x1088_30fps_420pl_252fr_HP_Interlaced_6mbps	1920x1080 High profile, CABAC, IPP, singleslice, 6mbps, sequence scaling, , transform 8X8, 2 reference frames, 1MV/MB, interlace	1.41	19.18	24.77	2.58	20.38	21.81

(1) Average and peak values may vary by ±5%.

Table 2. Cycles Information for Decoder Cofiguration H264_DEC_01 (continued)

INPUT NAME	PARAMETER	AVERAGE (1)			PEAK (1)		
		ARM926 PER MHz	FRAME DECODE MHZ	FPS	ARM926 PER MHz	FRAME DECODE MHZ	FPS
flower_352x288_HP_MBAFF_20_250 frames..264	CIF(352x288) High profile, CABAC, IPB, singleslice, 1mbps, transform 8X8, 5 reference frames, upto 16MV/MB, mbaff	0.37	1.84	293.5	1.83	3.11	142.34
door_p720x480_30 fps_420pl_40fr_HP _mbaff_1.5mbps.2 64	D1(720x480) High profile, CAVLC, IPP, multislice, 1.5mbps, single reference frame, 1MV/MB, mbaff	0.51	4.42	104.35	0.83	6.21	72.70
parkrun_p1280x72 0_30fps_420pl_30f r_HP_mbaff_7mbp s.264	(1280x720) High profile, CAVLC, IPP, multislice, 7mbps, single reference frame, 1MV/MB, mbaff	0.74	11.47	40.17	2.14	13.29	34.31
sjuggle_p1920x108 0_30fps_420pl_10f r_HP_mbaff_7mbp s.264	(1920x1080) High profile, CAVLC, IPP, multislice, 7mbps, single reference frame, 1MV/MB, mbaff	0.97	21.91	19.78	1.39	22.83	18.98

Table 3. Cycles Information for Decoder Cofiguration H264_DEC_02

INPUT NAME	RESOLUTION	AVERAGE (1)			PEAK (1)		
		ARM926 MHz	FRAME DECODE MHZ	FPS	ARM926 MHz	FRAME DECODE MHZ	FPS
akiyo_p352x288_30fps_420pl_300fr_120kbps.264 (progressive)	CIF(352x288)	0.36	1.08	410.38	0.84	1.51	287.85
shields_p720x480_25fps_420pl_252fr_2.4mbps.264 (progressive)	D1(720x480)	0.41	2.85	156.41	1.37	3.42	152.77
parkrun_p1280x720_30fps_420pl_300fr_4mbps.264 (progressive)	720p (1280x720)	0.83	6.21	74.65	1.06	6.43	39.07
sriverbed_p1920x1080_30fps_420pl_8mbps.264(progressive)	1080p (1920x1080)	0.87	12.96	33.69	0.98	21.78	19.71
waterfall_p352x288_30fps_420pl_260fr_HP_interlaced_256kbps.264 (interlace)	CIF(352x288)	0.64	1.58	278.27	1.18	2.17	252.02
jcube_i720x480_30fps_420pl_260fr_HP_Interlaced_2mbps.264 (interlace)	D1(720x480)	0.75	3.01	144.82	0.94	3.19	133.62
parkrun_p1280x720_30fps_420pl_30fr_HP_interlaced_7mbps.264 (interlace)	1280x720	0.94	7.64	64.90	1.21	9.77	61.78
EuropeanMarket_i1920x1080_30fps_420pl_450frames_HP_Interlaced_6mbps.264 (interlace)	1920x1080	1.46	13.78	31.36	2.60	14.90	28.55

(1) Average and peak values may vary by ±5%.

Notes:

- The performance numbers measured on DM368 platform with ARM @432 MHz, DDR @ 340, for other DM36x variants like ARM @297 MHz, DDR @ 270, these numbers will vary linearly based on DDR frequency ratio.
- The performance numbers are measured at certain bit-rates. For larger bit-rates like more than 12mbps for 720p and more than 20mbps for 1080p, some degradation in performance numbers can be observed.
- Decode frame depicts the cumulative load on ARM926 and HDVICP.
- The values in Table 2 and Table 3 are as measured on the ARM926 side. These are the actual cycles as seen from the host on the DM365 EVM board and will be close to cycles seen on the final system (for average case).
- ARM926 represents mega cycles per frame spend on ARM926.
- Decode frame time is the time seen from ARM926 only. Since most of the processing happens at HDVICP, the active load on ARM926 is the value mentioned in ARM926 column. Decoder frame time has no connection with HDVICP running at 340 MHz
- All the values are collected (both average and peak) at frame-level processing.
- They are measured in presence of linux without any system traffic
- The version of the code used to collect these numbers have the following features included:
  - Interrupt mode of operation – one interrupt signal processing overhead per frame.
  - Resetting of HDVICP and loading of code into HDVICP code and data memory – once per stream.

Table 4. Memory Statistics (Host ARM926 External Memory)

CONFIGURATION ID	MEMORY STATISTICS (IN BYTES)[1]						
	PROGRAM MEMORY	DATA MEMORY					TOTAL
		CONSTANT[2]	HEAP		STACK	DPB FOR LEVEL 4.2[3]	
			PERSISTENT[4]	SCRATCH			
H264_DEC_01	127336	374898	19054032	133120	16348	19000000	38705734
H264_DEC_02	127336	374898	9175680	133120	16348	19000000	28827382

(1) All these memory requirements are for ARM926 decoder library only. They do not include any memory requirements from test application side and input stream buffer. Stack, heap and code requirements for test-application are additional.
(2) Constant memory size requirements include HDVICP program memory since it forms a constant table on ARM926 before transfer. The constant size is the sum of .cinit, .bss, and .const sections used by H.264 decoder library.
(3) DPB for level 4.2 indicates tentative buffer requirements on the test application side to manage the DPB requirements of level 4.2 (however limited to the maximum resolution of 1920x1088) compliant H.264 decoder library implementing XDM1.2 API. DPB memory requirements given here include padding requirements along all dimensions (luma and packed chroma) assuming 4:2:0 format. It also includes memory required for holding the current frame. To enable optimal DMA transfers in the application, the picture width has been aligned to next 32-byte boundary. For example, padded and aligned 1080p picture would have a width of 1920 + 48 (Padding) + 16(alignment) = 1984. Because of these padding and alignment constraints, the DPB requirement for a normal picture would be different from that of its rotated version. The DPB requirement for some of the supported resolutions on the higher-end is given in Table 5.
(4) Persistent memory includes space required for 256 PPS and 32 SPS.

Table 5. DPB Requirement (for level 4.2)

RESOLUTION	DPB REQUIREMENT
1920x1088	19000000

Table 6. Internal Data Memory Split-Up

CONFIGURATION ID	DATA MEMORY - VICP and HDVICP (in bytes)			
	HDVICP PROGRAM MEMORY (bytes)	HDVICP DATA MEMORY (bytes)	HDVICP BUFFERS (bytes)	VICP (bytes)
H264_DEC_01 H264_DEC_02	48K	32K	ALL	40992

Note:
Formula for calculating VICP memory usage: Size = ((maxWidthMbs + 2) * 304) + ((maxWidthMbs + 2) * 32)

Table 7. H264 Decoder DM365 Codec Usage of Memory Via CMEM

BUFFER	YUV420P
Input Buffer[1]	0x200000 (Max)
Single Output Buffer (Luma + Chroma)	3523584
MEMTAB NUMBER	**SIZE IN BYTES[2]**
Memtab 0	1408
Memtab 1	17792
Memtab 2	17792
Memtab 3	1408
Memtab 4	8192
Memtab 5	18321120[3]
Memtab 6	282624
Memtab 7	195880
Memtab 8	175328
Memtab 9	58144
Memtab 10	384
Memtab 11	10240
Memtab 12	65792

(1) The size of the input buffer should be equal to or greater than one frame data..
(2) The table has numbers for 1080p resolution.
(3) The memtab 5 size is 8442768 bytes for configuration ID H264_DEC_02

Table 7. H264 Decoder DM365 Codec Usage of Memory Via CMEM (continued)

BUFFER	YUV420P
Memtab 13	30720

The following CMEM allocations are dependent on the maxWidth and maxheight and it provides the formula for calculating the size based on the input resolution:

- Output Buffer = Luma_frameSize_padded + Chroma_frameSize_padded

  where Luma_frameSize_padded = ((maxWidth + 48 + alignment)*(maxHeight+ 96)). and Chroma_frameSize_padded = Luma_frameSize_padded / 2.
- Memtab 4 = 2 * ((((maxWidth + 4 * 16) * 2) + 8 + 127) & 0xFFFFFF80)

  This is for storing the top rows for intra prediction. One for even row and one for odd row.
- Memtab 5 = Frame level collocated MB Info + Extra Frame Padding buffers

  where MB_Info_frame = ((((maxWidth >> 4) + 1) * (maxHeight >> 4)) + 1) * (dpb_limit at level 4.2 + 1). This is for storing ecd mb info data.and Frame_Pad_Buf = Luma_Frame_Pad_Buf + Chroma_Frame_Pad_Bufwhere Luma_Frame_Pad_Buf = ((maxWidth + 48 + alignment)*(48 + 1MB BB + 6) and Chroma_Frame_Pad_Buf = Luma_Frame_Pad_Buf / 2 Output Buffer maintains Field type padding only. Frame padding requires additional memory.

Notes

- HDVICP and VICP
  - The entire HDVICP is a video resource and is used by the codec
  - The codec uses VICP memory as scratch buffers and hence there is restriction on the usage of VICP concurrently.
- DMA configuration

Table 8. DMA Configuration for Universal Decoder

TC Q's	TC 0	TC 1	TC 2	TC 3	TOTAL
Usage	Used by codec	Used by codec	Used by codec	Reserved for system	-
Priority	1	1	1	0	-
EDMA Channels	16	9	1	NA	26
PaRAM Entries	58	14	1	NA	73
QDMA Channels	0	0	0	NA	0

Table 9. DMA Configuration for Closed Loop Decoder

TC Q's	TC 0	TC 1	TC 2	TC 3	TOTAL
Usage	Used by codec	Used by codec	Used by codec	Reserved for system	-
Priority	1	1	1	0	-
EDMA Channels	9	9	22	NA	40
PaRAM Entries	24	9	30	NA	63
QDMA Channels	0	0	0	NA	0

- The HDVICP/VICP/EDMA resources are acquired using a generic resource manager known as Framework Component. See *H.264 High Profile Decoder on DM365 User's Guide (SPRUEV0C)* for details.
- Code Placement
  - All the algorithm code are placed in external memory. The performance quoted is not sensitive to algorithm code placement.

References

- ISO/IEC 14496-10:2005 (E) Rec. - Information technology – Coding of audio-visual objects – H.264 (E) ITU-T Recommendation.
- *H.264 High Profile Decoder on DM365 User's Guide* (SPRUEV0C)

Glossary

TERM	DESCRIPTION
Constants	Elements that go into .const memory section
Scratch	Memory space that can be reused across different instances of the algorithm
Shared	Sum of Constants and Scratch
Instance	Persistent-memory that contains persistent information - allocated for each instance of the algorithm

Acronyms

ACRONYM	DESCRIPTION
ASO	Arbitrary Slice Order
CIF	Common Intermediate Format
1080p	1920x1080 or 1920x1088 resolution
DMA	Direct Memory Access
DPB	Decoded Picture Buffer

ACRONYM	DESCRIPTION
DTCM	Data Tightly Coupled Memory
EVM	Evaluation Module
FIQ	Fast Interrupt Request
FMO	Flexible Macro-block Ordering
HDVICP	High Definition Video and Imaging Co-Processor sub-system
IRQ	Interrupt Request
PPS	Picture Parameter Set
QCIF	Quarter Common Intermediate Format
QVGA	Quarter Video Graphics Array
RS	Redundant Slice
SEI	Supplemental Enhancement Information
SPS	Sequence Parameter Set
SQCIF	Sub Quarter Common Intermediate Format
UMV	Unrestricted Motion Vectors
VICP	Video and Imaging Co-Processor sub-system
VUI	Video Usability Information
WFI	Wait For Interrupt
XDAIS	eXpressDSP Algorithm Interface Standard
XDM	eXpressDSP Digital Media

Revision History

This datasheet revision history highlights the changes made to SPRS544B codec specific datasheet to make it SPRS544C

Table 10. Revision History for H.264 High Profile Decoder on DM365

SECTION	CHANGES
Table 2	Cycles Information for Decoder Cofiguration H264_DEC_01: • Updated Average and Peak values
Table 8	DMA Configuration for Universal Decoder • Updated TC Q's values

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