

Acoustic Echo Canceller (AEC)

Acoustic Echo Cancellation (AEC) is meant to cancel the echo generated during speakerphone operation due to the reverberations of the far end signal in the near end environment where an audio/video IP Phone is operating. Acoustic echo cancellers become important owing to the network delays that are an inherent part of packet based IP networks.

Features

- Support for 8kHz as well as 16kHz sampling frequency
- Does not make assumptions on the amount of echo or the ERL
- Does not make any assumptions on frame size
- No system delay introduced
- Does not conform to all specifications of ITU-T G.167 Recommendation
- Highly optimized for ARM9E core.
- Works in little-endian mode only.
- 'C' callable interface for AEC functions.
- Scratch based implementation, which avoids over-loading of stack during run-time.

AEC Validation

Ittiam's AEC module's optimized implementation on ARM9E core has been validated and tested extensively for various test cases, including a subset of the G.167 tests.

Resource requirement on simulator

Function	MCPS		Pgm	Table	Static	Scratch
	Avg	Peak	ROM (kb)		RAM (kb)	
AEC (8KHz, 10ms)	46.39	62.57	20.84	0	13.80	0
AEC (CNG Enabled)	49.69	66.18	43.15	0.93	15.92	1.37

Note: Static Memory requirements are for one instance of AEC and proportionally increases with the number the instances created.

Worst-case stack size requirement is KB. KB memory equals 1024 Bytes.

Note: Performance will be affected if the desired alignment for ROM and RAM is not provided.

Peak MCPS was measured using the various test vectors and is profiled on ARM simulator assuming zero-wait states.

Resource Requirement Details

CPU Loading

AEC configuration	Platforms			
	Simulator		Hardware	
	Avg	Peak	Avg	Peak
8 KHz, 10ms frame length, 128ms tail length	46.39	62.57	76.91	110.39
CNG enabled	49.69	66.18	85.21	118.47

Memory Usage

Summary

Configurations	Program	Table	Static	Stack	Scratch	Input	Output
8 KHz, 10ms frame length, 128ms tail length	20.84	0	13.80	0.4	0	2x(0.16)	2x(0.16)
CNG Enable	43.15	0.93	15.92	0.5	1.37	2x(0.16)	2x(0.16)

Memory usage detail for 8000 Hz sampling frequency

Record	Size	Attribute	Space	Alignment
0	608	IALG_PERSIST	IALG_DARAM0	8
1	612	IALG_PERSIST	IALG_SARAM	64
2	13726	IALG_PERSIST	IALG_DARAM0	2048
3	76	IALG_PERSIST	IALG_DARAM0	8
4	1964	IALG_PERSIST	IALG_SARAM	8
5	992	IALG_SCRATCH	IALG_SARAM	8
6	26	IALG_WRITEONCE	IALG_DARAM0	8
7	66	IALG_WRITEONCE	IALG_DARAM0	8
8	66	IALG_WRITEONCE	IALG_DARAM0	8
9	480	IALG_WRITEONCE	IALG_DARAM0	8
10	24	IALG_WRITEONCE	IALG_DARAM0	8
11	24	IALG_WRITEONCE	IALG_DARAM0	8
12	66	IALG_WRITEONCE	IALG_DARAM0	8
13	98	IALG_WRITEONCE	IALG_DARAM0	8
14	28	IALG_PERSIST	IALG_DARAM0	8
15	16	IALG_PERSIST	IALG_SARAM	8
16	472	IALG_SCRATCH	IALG_SARAM	8
17	98	IALG_WRITEONCE	IALG_DARAM0	8

Memory usage detail for 16000 Hz sampling frequency

Record	Size	Attribute	Space	Alignment
0	608	IALG_PERSIST	IALG_DARAM0	8
1	612	IALG_PERSIST	IALG_SARAM	64
2	26014	IALG_PERSIST	IALG_DARAM0	4096
3	76	IALG_PERSIST	IALG_DARAM0	8
4	1964	IALG_PERSIST	IALG_SARAM	8
5	1472	IALG_SCRATCH	IALG_SARAM	8
6	26	IALG_WRITEONCE	IALG_DARAM0	8
7	66	IALG_WRITEONCE	IALG_DARAM0	8
8	66	IALG_WRITEONCE	IALG_DARAM0	8
9	480	IALG_WRITEONCE	IALG_DARAM0	8
10	24	IALG_WRITEONCE	IALG_DARAM0	8
11	24	IALG_WRITEONCE	IALG_DARAM0	8
12	66	IALG_WRITEONCE	IALG_DARAM0	8
13	98	IALG_WRITEONCE	IALG_DARAM0	8
14	960	IALG_PERSIST	IALG_SARAM	8
15	960	IALG_WRITEONCE	IALG_DARAM0	8
16	24	IALG_WRITEONCE	IALG_DARAM0	8
17	24	IALG_WRITEONCE	IALG_DARAM0	8
18	28	IALG_PERSIST	IALG_DARAM0	8
19	16	IALG_PERSIST	IALG_SARAM	8
20	792	IALG_SCRATCH	IALG_SARAM	8
21	98	IALG_WRITEONCE	IALG_DARAM0	8
19	16	IALG_PERSIST	IALG_SARAM	8
20	792	IALG_SCRATCH	IALG_SARAM	8
21	98	IALG_WRITEONCE	IALG_DARAM0	8

Notes:

- Memory numbers are in KB (Kilobytes)
- Stack size is given for Process and Control calls. Including initialization it will be 0.7 KB with CNG support.
- I/O Buffer size is for input/output buffers for frame length of 10ms
- Performance numbers on Simulator generated with ARM ADS Tools version 1.2 *with 0-wait state memory access and without Cache*
- Hardware performance generated on ARM9E processor with 16Kb of I Cache and 8 Kb of D Cache.
- Hardware performance generated under Linux 2.6, using the ARM-GCC 3.4.3 Compiler
- MCPS numbers on the hardware will vary with the I-Cache and D-Cache size and with the memory configuration/place

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