H.264 Baseline Profile Decoder (v2.01) on OMAP3530

FEATURES

- **eXpressDSP™ Digital Media (XDM 1.0 IVIDDEC2) compliant**
- **Validated on the OMAP3530 EVM**
- **Up to Level 3.0 features of the Baseline Profile (BP) supported**
- **Progressive frame type picture decoding supported**
- **Multiple slices and multiple reference frames supported**
- **CAVLC decoding using the iVLCD hardware accelerator provided on OMAP3530 supported**
- **All intra-prediction and inter-prediction modes supported**
- **Up to 16 MV per MB supported**
- **Frame based decoding with frame size being multiples of 16 and non multiples of 16 supported**
- **Outputs are available in YUV420 planar and YUV422 interleaved**
- **Frame width of the range of 32 to 864 pixels is supported**
- **All resolutions up to and below WVGA including PAL and NTSC D1, CIF, QCIF and so on are Supported**
- **Tested for compliance with JM version 14.0 reference decoder**
- **ASO and FMO error concealment features supported**
- **Redundant slices supported**
- **Supplemental Enhancement Information (SEI) and Video Usability Information (VUI) supported**
- **NAL unit stream supported**
- **Reference picture list reordering supported**
- **Frame cropping and display width supported**
- **Configurable display delay supported**
- **Adaptive reference picture marking supported**
- **Returns the decoding status of each macro block of the frame in the buffer, which the application provides to the library**

DESCRIPTION

H.264 (from ITU-T, also called as H.264/AVC) is a popular video coding algorithm enabling high quality multimedia services on a limited bandwidth network. This codec has been built and tested on the OMAP3530 EVM with Code Composer Studio version 3.3.46.1 and code generation tools version 6.0.8.

PRODUCT PREVIEW

Performance Summary

This section describes the performance of the H.264 Baseline Profile Decoder on OMAP3530 EVM.

Table 1. Configuration Table

CONFIGURATION	ID
Level 1.0 Baseline Profile	H264_DEC_001
Level 2.0 Baseline Profile	H264_DEC_002
Level 3.0 Baseline Profile	H264_DEC_003

Table 2. Cycles Information for 420 format – Profiled on OMAP3530 Hardware with Code Generation Tools Version 6.0.8

CONFIGURATION ID	PERFORMANCE STATISTICS (MEGA CYCLES PER SECOND)(1) (2)		
	TEST DESCRIPTION	AVERAGE(3)	PEAK(4)
H264_DEC_001	mps_mw_a.264n, YUV420, 4MV, QCIF(176x144), @ 256kbps	29	33
H264_DEC_002	traffic_multiple_slice_aso.264n, YUV420, 4MV, CIF(352x288),@560kbps	82	108
H264_DEC_003	football_5mbps_30frames.264n, YUV420, 4MV, VGA(640x480),@ 5 mbps	262	303
	fire_30frames_2_Mbps.264n, YUV420, 16MV, D1(720x480), @ 2 mbps	251	263
	fire_30frames_5_Mbps.264n, YUV420, 16MV, D1(720x480), @ 5 mbps	295	308
	call_log.h264n, YUV420, 4MV, WVGA (864x480) @ 1.4Mbps	192	272
	00005_854x480_H264_10Mbps.264, YUV420, 4MV, WVGA (854x480) @ 10Mbps	363	563
	sheilds_720x480_1MV_1_5Mbps.264 , YUV420, 1MV, D1 (720x480) @ 1.5Mbps	211	280

(1) Measured with program memory, stack and I/O buffers in external memory, 32 K-bytes L1P cache, 64 K-bytes L1D data memory, 16 K-bytes L1D cache, 64 K-bytes L2D cache, 32 K-bytes SL2 memory for accelerators/sequencer usage and CPU speed at 350 MHz.
(2) Average and peak MCPS measurements can vary by +/-5%.
(3) Based on average number of cycles per frame @ 30 fps.
(4) Based on worst case cycles per frame @ 30 fps.

Table 3. Cycles Information for 422 format – Profiled on OMAP3530 Hardware with Code Generation Tools Version 6.0.8

CONFIGURATION ID	PERFORMANCE STATISTICS (MEGA CYCLES PER SECOND)(1) (2)		
	TEST DESCRIPTION	AVERAGE(3)	PEAK(4)
H264_DEC_001	mps_mw_a.264n, YUV422, 4MV, QCIF(176x144), @ 256kbps	30	33
H264_DEC_002	traffic_multiple_slice_aso.264n, YUV422, 4MV, CIF(352x288),@560kbps	82	108
H264_DEC_003	football_5mbps_30frames.264n, YUV422, 4MV, VGA(640x480),@ 5 mbps	261	303
	fire_30frames_2_Mbps.264n, YUV422, 16MV, D1(720x480), @ 2 mbps	251	263
	fire_30frames_5_Mbps.264n, YUV422, 16MV, D1(720x480), @ 5 mbps	295	307
	call_log.h264n, YUV422, 4MV, WVGA (864x480) @ 1.4Mbps	191	270
	00005_854x480_H264_10Mbps.264, YUV422, 4MV, WVGA (854x480) @ 10Mbps	365	562
	sheilds_720x480_1MV_1_5Mbps.264 , YUV422, 1MV, D1 (720x480) @ 1.5Mbps	211	280

(1) Measured with program memory, stack and I/O buffers in external memory, 32 K-bytes L1P cache, 64 K-bytes L1D data memory, 16 K-bytes L1D cache, 64 K-bytes L2D cache, 32 K-bytes SL2 memory for accelerators/sequencer usage and CPU speed at 350 MHz.
(2) Average and peak MCPS measurements can vary by +/-5%.
(3) Based on average number of cycles per frame @ 30 fps.
(4) Based on worst case cycles per frame @ 30 fps.

Table 4. Memory Statistics - Generated with Code Generation Tools Version 6.0.8

CONFIGURATION ID	MEMORY STATISTICS(1)					
	PROGRAM MEMORY	DATA MEMORY				TOTAL
		INTERNAL	EXTERNAL	STACK	SL2	
H264_DEC_001	554	62	1297	14	32	1959
H264_DEC_002	554	62	4056	14	32	4718
H264_DEC_003	554	62	6429	14	32	7091

(1) All memory requirements are expressed in kilobytes (1 kilobyte = 1024 bytes) and there could be a variation of around 1-5% in numbers.

Note: 9.8 K-bytes of SL2 data memory is used for iLF accelerator.

Table 5. Internal Data Memory Split-Up

CONFIGURATION ID	DATA MEMORY - INTERNAL(1)		
	SHARED		INSTANCE(2)
	CONSTANTS	SCRATCH	
H264_DEC_001	6	56	0
H264_DEC_002	6	56	0
H264_DEC_003	6	56	0

(1) Internal memory refers to L1D RAM. All memory requirements are expressed in kilobytes (1 kilobyte = 1024 bytes) and there could be a variation of around 1-5% in numbers.
(2) I/O buffers not included. Some of the instance memory buffers could be scratch.

Table 6. External Data Memory Split-Up

CONFIGURATION ID	DATA MEMORY - EXTERNAL		
	CONSTANTS	FAR	PERSISTENT
H264_DEC_001	20	1	1276
H264_DEC_002	20	1	4035
H264_DEC_003	20	1	6408

Table 7. iVLCD Co-processor(s) Memory Statistics

CONFIGURATION ID	IBUF0(1)	IBUF1(1)	QMEM(1)	HMEM(1)
H264_DEC_001	1	3	1	7
H264_DEC_002	1	3	1	7
H264_DEC_003	1	3	1	7

(1) All memory requirements are expressed in kilobytes (1 kilobyte = 1024 bytes).

Notes

- Evaluation version performance values may be higher than the values specified in the performance table.
- Display buffer for YUV422 interleaved format is 810 KB for WVGA format (864 X 480)
- Input buffer to algorithm is assumed to have at least one encoded frame data. Otherwise, the application must provide CPB buffer size amount of valid data to the algorithm. For a specific level the CPB size could be referred from the standard.
- Memory Configuration
  - L2: 64KB Cache
- The performances obtained in Table 2 are sensitive to algorithm code placement. Refer the sample linker file provided in the test application setup for algorithm code placement. This is used for profiling in Table 2.
- The algorithm uses 6 QDMA channels and parameter space equal to 48 parameter entries. The algorithm uses DMAN3 interface for logical allocation of these channels
- Total data memory for N non pre-emptive instances = Constants + Runtime Tables + Scratch + N*(Instance + I/O buffers + Stack)
- Total data memory for N pre-emptive Instances = Constants + Runtime Tables + N*(Instance + I/O buffers + Stack + Scratch)

References

- ISO/IEC 14496-10:2005 (E) Rec. - Information technology – Coding of audio-visual objects – H.264 (E) ITU-T Recommendation.
- *H.264 Baseline Profile Decoder on OMAP3530 User's Guide* (literature number: SPRUEU5A)

Glossary

TERM	DESCRIPTION
Constants	Elements that go into .const memory section
Scratch	Memory space that can be reused across different instances of the algorithm
Shared	Sum of Constants and Scratch
Instance	Persistent-memory that contains persistent information - allocated for each instance of the algorithm

Acronyms

ACRONYM	DESCRIPTION
625SD	Level 3.0 Maximum resolution format size 720x576
CIF	Common Intermediate Format
CPB	Coded Picture Buffer
DMA	Direct Memory Access
DMAN3	DMA Manager
EVM	Evaluation Module
QCIF	Quarter Common Intermediate Format
QDMA	Quick Direct Memory Access
SDTV	Standard Definition Television
VGA	Video Graphics Array (640x480 resolution)
WVGA	864x480 size resolution
XDM	eXpressDSP Digital Media

Revision History

This data sheet revision history highlights the changes made to the SPRS542 codec specific data sheet to make it SPRS542A

NOTE

There are no changes in data sheet for this release.

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