

## H.264 1080p@30 BP Encoder (v01.10.02) on DM6467

### FEATURES

- eXpressDSP™ Digital Media (XDM 1.0 IVIDENC1) compliant
- Validated on DM6467 EVM
- YUV420SP interleaved color sub-sampling (Y as a single plane and U and V components interleaved to form the second plane) formats supported
- H.264 Baseline Profile for only progressive I and P frames supported
- Multiple slices per frame conforming to H.241 requirement of fixed bytes per slice supported
- Only one motion vector per macro block supported
- Rate control at row and frame level supported
- DMA based framework supported

- C64x+ and both HDVICP0, HDVICP1 subsystems are used
- The 720p quality of this encoder is not at par with the 720p encode only solution from TI, tradeoffs have been made to get performance for 1080p at the cost of quality

### DESCRIPTION

H.264 is the latest video compression standard from the ITU-T Video Coding Experts Group and the ISO/IEC Moving Picture Experts Group. This H.264 Encoder is validated on the DM6467 EVM with Code Composer Studio version 3.3.49 and code generation tools version 6.0.8.

**PRODUCT PREVIEW**



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

eXpressDSP is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

Copyright © 2010, Texas Instruments Incorporated

## Performance Summary

This section describes the performance of the H.264 1080p@30 BP Encoder on DM6467 EVM.

**Table 1. Configuration Table**

CONFIGURATION	ID
H264 Baseline Profile Encoder with single frame as one slice	DM6467_BP_E_001
H264 Baseline Profile Encoder with H.241 support	DM6467_BP_E_002

**Table 2. Cycles Information – Profiled on DM6467 EVM with Code Generation Tools Version 6.0.8**

CONFIGURATION ID	PERFORMANCE STATISTICS (MEGA CYCLES PER SECOND) <sup>(1)</sup>				
	TEST DESCRIPTION <sup>(2)</sup>	NON-BLOCKING DSP CYCLES@675MHZ		BLOCKING DSP CYCLES@675MHZ	
		AVERAGE <sup>(3)</sup>	PEAK <sup>(4)</sup>	AVERAGE <sup>(3)</sup>	PEAK <sup>(4)</sup>
DM6467_BP_E_001	bluesky_p1920x1088_30fps_420pl.yuv Bitrate : 4Mbps	550	551	587	589
	pedestrian_p1920x1088_24fps_420pl.yuv Bitrate : 4Mbps	554	556	591	593
DM6467_BP_E_002	Input used: bluesky_p1920x1088_30fps_420pl.yuv Bitrate : 4Mbps Packet Size: 1500 bytes	591	593	618	619
	Input used: pedestrian_p1920x1088_24fps_420pl.yuv Bitrate : 4Mbps Packet Size: 1500 bytes	595	598	622	625

- (1) Measured with program memory, stack, and I/O buffers in external memory with cache configuration: 32 KB L1P Program Cache, 32 KB L1D Data Cache, 64 KB L2 Cache and 64KB mapped L2 SRAM. There could be a variation of approximately 1- 2% in the values.
- (2) The Intra Period for the test vectors is 30 frames. That is, with one I-frame and 29 P-frames.
- (3) Based on average number of cycles per frame @ 30fps. That is, with one I-frame and 29 P-frames.
- (4) Based on worst case cycles per frame @ 30fps.

**Table 3. Memory Statistics**

CONFIGURATION ID	MEMORY STATISTICS <sup>(1)</sup>				
	PROGRAM MEMORY	DATA MEMORY			TOTAL
		INTERNAL <sup>(2)</sup>	EXTERNAL <sup>(3)</sup>	STACK	
DM6467_BP_E_001	152	63	8594	12	8821
DM6467_BP_E_002	152	63	8594	12	8821

- (1) All memory requirements are expressed in kilobytes (1K-byte = 1024 bytes). There could be a variation of approximately 1-2% in the values.
- (2) Internal memory is placed in L2 SRAM.
- (3) Includes frame buffers for 1080i/p resolution.

**Table 4. Internal Data Memory Split-Up**

CONFIGURATION ID	DATA MEMORY - INTERNAL <sup>(1)</sup>		
	SHARED		INSTANCE
	CONSTANTS	SCRATCH	
DM6467_BP_E_001	0	63	0
DM6467_BP_E_002	0	63	0

- (1) All memory requirements are expressed in kilobytes. There could be a variation of approximately 1-2% in the values.

**Table 5. External Data Memory Split-Up**

CONFIGURATION ID	DATA MEMORY - EXTERNAL <sup>(1)</sup>		
	SHARED		INSTANCE
	CONSTANTS	SCRATCH	
DM6467_BP_E_001	164	23	8407

- (1) All memory requirements are expressed in kilobytes. There could be a variation of approximately 1-2% in the values.

**Table 5. External Data Memory Split-Up (continued)**

CONFIGURATION ID	DATA MEMORY - EXTERNAL <sup>(1)</sup>		
	SHARED		INSTANCE
	CONSTANTS	SCRATCH	
DM6467_BP_E_002	164	23	8407

**PRODUCT PREVIEW**

## Notes

The performance values in [Table 2](#) is a result of the following configurations:

- HDVICP
  - The entire HDVICP is a video resource and uses 16K ITCM and 8K DTCM.
  - The 1080i encoder uses both the HDVICP resources of DM6467. Hence, simultaneous encode/decode is not possible with this encoder.
- Cache configuration

**Table 6. Cache Configuration**

	AVAILABLE	USED
L1 p (Program Memory)	32k	32k – cache
L1d (Data Memory)	32k	32k – cache
L2	128k	64k – cache

- Resources used and clock speed

**Table 7. Resources Used and Clock Speed**

RESOURCES USED	CLOCK SPEED (IN MEGA HERTZ)
C64x+	675
ARM 968	337
HDVICP Co-processors	337
DDR (32-bit, 8 Bank)	310

- DMA configuration

**Table 8. DMA Configuration**

TC Q's	TC 0	TC 1	TC 2	TC 3	TOTAL USED	TOTAL AVAILABL E
<b>Usage</b>	Writes to HDVICP	Writes to DDR	Writes to L2 SRAM	Writes to HDVICP	-	-
<b>Priority</b>	2	2	2	2	-	-
<b>EDMA Channels</b>	19	7	19	4	49	64
<b>QDMA Channels</b>	0	0	0	0	0	8
<b>Number of PaRAM Sets</b>	-	-	-	-	103	512

- Code Placement
  - All the algorithm code are placed in external memory. The performance values in [Table 2](#) are sensitive to algorithm code placement. See the sample linker file provided in the test application setup for algorithm code placement.

## References

- ISO/IEC 14496-10:2005 Information technology -- Coding of audio-visual objects -- Part 10: Advanced Video Coding
- *H.264 1080p@30 BP Encoder User's Guide* (literature number: SPRUGN8E)

## Glossary

TERM	DESCRIPTION
Constants	Elements that go into .const memory section
Scratch	Memory space that can be reused across different instances of the algorithm
Shared	Sum of Constants and Scratch
Instance	Persistent-memory that contains persistent information - allocated for each instance of the algorithm

## Acronyms

ACRONYM	DESCRIPTION
BP	Baseline Profile
CIF	Common Intermediate Format
DMA	Direct Memory Access
DMAN3	DMA Manager
EVM	Evaluation Module
GOP	Group of Pictures
HDVICP	High Definition Video and Imaging Co-Processor
HP	High Profile
LPF	Loop Filter
MV	Motion Vector
QCIF	Quarter Common Intermediate Format
QDMA	Quick Direct Memory Access
QPI	Quarter Pel Interpolation
QVGA	Quarter Video Graphics Array
SQCIF	Sub Quarter Common Intermediate Format
SEI	Supplemental Enhancement Information
UMV	Unrestricted Motion Vector
VGA	Video Graphics Array
XDM	eXpressDSP Digital Media

## Revision History

Revision history highlights the changes made to the SPRS600D codec specific data sheet to make it SPRS600E.

**Table 9. Revision History for H.264 1080p@30 BP Encoder on DM6467**

Section	Changes
<a href="#">Table 2</a>	<ul style="list-style-type: none"> <li>Modified Average and Peak values.</li> </ul>

## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

<b>Products</b>		<b>Applications</b>	
Amplifiers	<a href="http://amplifier.ti.com">amplifier.ti.com</a>	Audio	<a href="http://www.ti.com/audio">www.ti.com/audio</a>
Data Converters	<a href="http://dataconverter.ti.com">dataconverter.ti.com</a>	Automotive	<a href="http://www.ti.com/automotive">www.ti.com/automotive</a>
DLP® Products	<a href="http://www.dlp.com">www.dlp.com</a>	Communications and Telecom	<a href="http://www.ti.com/communications">www.ti.com/communications</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>	Computers and Peripherals	<a href="http://www.ti.com/computers">www.ti.com/computers</a>
Clocks and Timers	<a href="http://www.ti.com/clocks">www.ti.com/clocks</a>	Consumer Electronics	<a href="http://www.ti.com/consumer-apps">www.ti.com/consumer-apps</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>	Energy	<a href="http://www.ti.com/energy">www.ti.com/energy</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>	Industrial	<a href="http://www.ti.com/industrial">www.ti.com/industrial</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>	Medical	<a href="http://www.ti.com/medical">www.ti.com/medical</a>
Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>	Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
RFID	<a href="http://www.ti-rfid.com">www.ti-rfid.com</a>	Space, Avionics & Defense	<a href="http://www.ti.com/space-avionics-defense">www.ti.com/space-avionics-defense</a>
RF/IF and ZigBee® Solutions	<a href="http://www.ti.com/lprf">www.ti.com/lprf</a>	Video and Imaging	<a href="http://www.ti.com/video">www.ti.com/video</a>
		Wireless	<a href="http://www.ti.com/wireless-apps">www.ti.com/wireless-apps</a>

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2010, Texas Instruments Incorporated