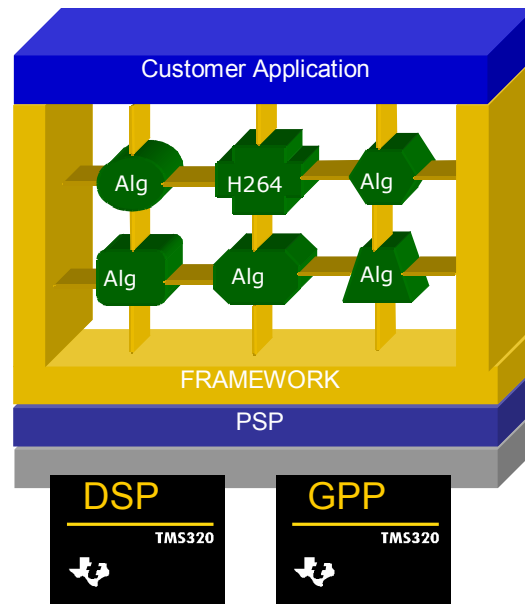




- eXpressDSP Digital Media (XDM 1.2 IVIDDEC2) compliant
- Up to 1080p60 of the Baseline Profile (BP) supported
- Validated on DM6467 EVM
- Progressive type picture decoding supported
- Multiple slices and multiple reference frames supported
- CAVLC decoding supported
- All intra-prediction and inter-prediction modes supported
- Up to 16 MV per MB supported
- Frame based decoding supported
- Picture width greater than 176 pixels supported
- Tested for compliance with JM version 10.1 reference decoder
- Long term reference frame and Adaptive reference picture marking supported
- Reference Picture List Reordering supported
- PCM Macroblock decoding supported
- Gaps in frame\_num supported
- Error Resiliency and Concealment supported
- SEI and VUI parsing supported
- Intra-frame Pulse Code Modulation (I\_PCM) decoding



## Description

H.264 is a popular video coding algorithm enabling high quality multimedia services on a limited bandwidth network. H264 Decoder is validated on DM6467 EVM with Code Composer Studio version 3.3.82.13 and code generation tools version 6.0.8.

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Summary of performance

**Table 1. Configuration Table**

CONFIGURATION	ID
H264 Baseline Profile Decoder	DM6467_BP_001

**Table 2. Cycles Information in MHz Profiled on 1000 MHZ DM6467 EVM**

CONFIGURATION ID	PERFORMANCE STATISTICS (IN MEGA CYCLES PER SEC) <sup>1</sup>				
	TEST DESCRIPTION	NON-BLOCKING DSP CYCLES@1000 MHZ		BLOCKING DSP CYCLES@1000 MHZ	
		AVG <sup>3</sup>	PEAK <sup>2</sup>	AVG <sup>3</sup>	PEAK <sup>2</sup>
DM6467_BP_001	station2_p1920x1088_24fps_420pl_313fr_1500_8Mbps_cbr <sup>4</sup>	678	708	918	1050
DM6467_BP_001	stockholm_p1280x720_30fps_420pl_302fr_RC0_QP25_FR30_BitRate1000000_test <sup>5</sup>	334	426	352	468
DM6467_BP_001	mobcal_p720x480_25fps_420pl_252fr_RC1_QP43_FR30_BitRate2000000_test <sup>6</sup>	127	136	163	168

<sup>1</sup> Measured with program memory, stack, and I/O buffers in external memory and with cache configuration 64 K bytes L2 cache, 32 K L1D and 32 K L1P cache.

<sup>2</sup> Peak values are calculated assuming that the most demanding frame is repeated 60 times in the sequence, rather than finding the most demanding 60 frames sequence in the bit-stream

<sup>3</sup> Average values are calculated based on the average of all frames in the sequence.

<sup>4</sup> This bitstream was made from a 24 fps 1920x1088 YUV sequence. However, the performance numbers are calculated assuming this bitstream is decoded at the 60 fps rate.

<sup>5</sup> This bitstream was made from a 30 fps 1280x720 YUV sequence. However, the performance numbers are calculated assuming this bitstream is decoded at the 60 fps rate.

<sup>6</sup> This bitstream was made from a 25 fps 720x480 YUV sequence. However, the performance numbers are calculated assuming this bitstream is decoded at the 60 fps rate.

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**Table 3. Memory Statistics – Generated with Code Generation Tools Version 6.0.8**

CONFIGURATION ID	MEMORY STATISTICS <sup>4</sup>				
	PROGRAM MEMORY	DATA MEMORY			TOTAL
		INTERNAL	EXTERNAL <sup>5</sup>	STACK	
DM6467_BP_001	274	56.38	13,612.86	4.50	13,947.73

<sup>4</sup> All memory requirements are expressed in kilobytes (1K-byte = 1024 bytes).

<sup>5</sup> Does not include frame buffers for 1080p resolution.

The program memory quoted also includes the HDVICP API's used by the decoder.

**Table 4. Internal Data Memory Split-up**



CONFIGURATION ID	CONFIGURATION ID	DATA MEMORY – INTERNAL <sup>7</sup>		
		SHARED		INSTANCE
		CONSTANTS	SCRATCH	
DM6467_BP_001	DM6467_BP_001	0.00	56.38	0.00

<sup>7</sup> All memory requirements are expressed in kilobytes.

**Table 5. External Data Memory Split-up**

CONFIGURATION ID	DATA MEMORY – EXTERNAL <sup>8</sup>		
	SHARED		INSTANCE
	CONSTANTS	SCRATCH	
DM6467_BP_001	274	0.00	13,612.86

<sup>8</sup> All memory requirements are expressed in kilobytes.

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**Notes**

The performance quoted in Table 2 is a result of below configuration.

- HDVICP
  - The entire HDVICP is a video resource and uses 16 K ITCM and 8 K DTCM.
  - The decoder is configured to run on either HDVICP-0 or HDVICP-1.
- Cache configuration

	Available	Used
L1 p (Program memory)	32 k	32 k – cache
L1d (Data memory)	32 k	32 k – cache
L2	128 k	64 k – cache

- DMA configuration

TC Q's	TC 0	TC 1	TC 2	TC 3	Total	Max*
<b>Usage</b>	not used	Writes to DSP L2 SRAM	DDR	the others	-	-
<b>Priority<sup>^</sup></b>	n/a	2	2	3	-	-
<b>EDMA channels</b>	0	3	12	8	23	64
<b>QDMA channels</b>	0	0	0	0	0	8
<b>Num PARAMS</b>	-	-	-	-	160	512

<sup>^</sup> Lesser number corresponds to higher TC priority. Default priority is 2. When different TC's have same priority, the arbitration order is TC0 > TC1 > TC2 > TC3.

\* Max corresponds to the maximum number of EDMA/QDMA channels or maximum number of PARAMS available on the chip. It does NOT indicate the maximum number requested by the codec.

- Code Placement
  - All the algorithm codes are placed in external memory. The performance quoted in Table 2 are sensitive to algorithm code placement. Refer to the sample linker file provided in the test application setup for algorithm code placement.

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## References

- ISO/IEC 14496-10: March 2005 (E) Rec. H.264 (E) ITU-T Recommendation
- H.264 High Profile Decoder User Guide

## Glossary

Constants	Elements that go into .const memory section
Scratch	Memory space that can be reused across different instances of the algorithm or across different algorithms
Shared	Sum of Constants and Scratch
Instance	Memory that contains persistent information - allocated for each instance of the algorithm

## Acronyms

625SD	Level 3.0 Maximum resolution format size 720x576
CIF	Common Intermediate Format
CPB	Coded Picture Buffer
D1	SDTV image resolution (720x480)
QCIF	Quarter Common Intermediate Format
QDMA	Quick Direct Memory Access
SDTV	Standard Definition Television
SEI	Supplemental Enhancement Information
VGA	Video Graphics Array (640x480 resolution)
VUI	Video Usability Information
XDM	eXpressDSP Digital Media
HD	High Definition

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