

H.264 High Profile Decoder (v01.10.05) on DM6467

Check for Samples:

FEATURES

- eXpressDSP™ Digital Media (XDM 1.0 IVIDDEC2) compliant
- Up to level 4 features of the High Profile (HP) supported
- Validated on DM6467 EVM
- Progressive, interlaced, Picture Adaptive Frame Field (PicAFF) and Macro-block Adaptive Frame Field (MBAFF) type picture decoding supported
- Multiple slices and multiple reference frames supported
- CAVLC and CABAC decoding supported
- All intra-prediction and inter-prediction modes supported
- Up to 16 MV per MB supported
- Frame based decoding supported

- Picture width greater than 64 pixels supported
- Tested for compliance with JM version 10.1 reference decoder
- Long term reference frame and adaptive reference picture marking supported
- Reference picture list reordering supported
- PCM macro block decoding supported
- Gaps in frame_num supported
- Error resiliency and concealment supported
- SEI and VUI parsing supported

DESCRIPTION

H.264 is a popular video coding algorithm enabling high quality multimedia services on a limited bandwidth network. H264 Decoder is validated on DM6467 EVM with Code Composer Studio version 3.3.49 and code generation tools version 6.0.8.

PRODUCT PREVIEW



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

eXpressDSP is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

Performance Summary

This section describes the performance of the H264 Decoder on DM6467 EVM.

Table 1. Configuration Table

CONFIGURATION	ID
H264 High Profile Decoder	DM6467_HP_001

Table 2. Cycles Information in MHz - Profiled on DM6467 EVM⁽¹⁾ with Code Generation Tools Version 6.0.8

CONFIGURATION ID	PERFORMANCE STATISTICS (MEGA CYCLES PER SECOND) ^{(2) (3)}				
	TEST DESCRIPTION	NON-BLOCKING DSP CYCLES@675MHz		BLOCKING DSP CYCLES@675MHz	
		AVERAGE ⁽⁴⁾	PEAK ⁽⁵⁾	AVERAGE ⁽⁴⁾	PEAK ⁽⁵⁾
DM6467_HP_001	BALLOONS.264; High Profile, 1920 X 1088, MBAFF, IPBB...	320.2	355.3	571.3	598.5
	fball_60.264; High Profile, 1920 X 1088, MBAFF, IPBB...	333.1	352.4	584.2	597.1
	letterman1_30.264; High Profile, 1920 X 1088, MBAFF, IPBB...	334.3	352.6	584.4	596.1

- (1) C64x+ is clocked at 675MHz. DDR is 32-bit, clocked at 310MHz, 8 bank. HDVICP is clocked at 337MHz.
 (2) Measured with program memory, stack, and I/O buffers in external memory and with cache configuration 64 K bytes L2 cache, 32 K L1D and 32 K L1P cache.
 (3) Average and peak MCPS measurements can vary by +/-5%.
 (4) Average values are calculated based on the average of all frames in the sequence.
 (5) Peak values are calculated assuming that the most demanding frame is repeated 30 times in the sequence, rather than finding the most demanding 30 frames sequence in the bit-stream.

Table 3. Memory Statistics - Generated with Code Generation Tools Version 6.0.8

CONFIGURATION ID	MEMORY STATISTICS ⁽¹⁾				
	PROGRAM MEMORY ⁽²⁾	DATA MEMORY			TOTAL
		INTERNAL ⁽³⁾	EXTERNAL ⁽⁴⁾	STACK	
DM6467_HP_001	300.38	22.63	24144.12	4.00	24462.47

- (1) All memory requirements are expressed in kilobytes (1K-byte = 1024 bytes).
 (2) Program memory quoted also includes the HDVICP APIs used by the decoder.
 (3) Internal memory is placed in L2 SRAM.
 (4) Includes frame buffers for 1080P resolution.

Table 4. Internal Data Memory Split-Up

CONFIGURATION ID	DATA MEMORY - INTERNAL ⁽¹⁾		
	SHARED		INSTANCE
	CONSTANTS	SCRATCH	
DM6467_HP_001	0	22.63	0

- (1) All memory requirements are expressed in kilobytes.

Table 5. External Data Memory Split-Up

CONFIGURATION ID	DATA MEMORY - EXTERNAL ⁽¹⁾		
	SHARED		INSTANCE
	CONSTANTS	SCRATCH	
DM6467_HP_001	207.70	0	23936.42

- (1) All memory requirements are expressed in kilobytes.

Notes

The performance values shown in [Table 2](#) is a result of the following configurations:

- HDVICP
 - The entire HDVICP is a video resource and uses 16K ITCM and 8K DTCM.
 - The decoder is configured to run either on HDVICP-0 or HDVICP-1.
- Cache configuration

Table 6. Cache Configuration

	AVAILABLE	USED
L1 p (Program Memory)	32K	32K – cache
L1d (Data Memory)	32K	32K – cache
L2	128K	64K – cache

- DMA configuration

Table 7. DMA Configuration

TC Qs	TC 0	TC 1	TC 2	TC 3	TOTAL	MAXIMUM ⁽¹⁾
Usage	Writes to L2 SRAM	Writes to HDVICP	Writes to HDVICP	Writes to HDVICP	-	-
Priority ⁽²⁾	3	2	2	3	-	-
EDMA channels	1	8	8	4	21	64
QDMA channels	0	0	0	0	0	8
Num PARAMS	-	-	-	-	159	512

(1) Maximum corresponds to the maximum number of EDMA/QDMA channels or maximum number of PARAMS available on the chip. It does not indicate the maximum number requested by the codec.

(2) Lesser number corresponds to higher TC priority. Default priority is 2. When different TCs have same priority, the arbitration order is TC0 > TC1 > TC2 > TC3.

- Code Placement

All the algorithm code are placed in external memory. The performance values in [Table 2](#) are sensitive to algorithm code placement. See the sample linker file provided in the test application setup for algorithm code placement.

References

- ISO/IEC 14496-10: March 2005 (E) Rec. H.264 (E) ITU-T Recommendation
- *H.264 High Profile Decoder on DM6467 User's Guide* (literature number: SPRUFE0A)

Glossary

TERM	DESCRIPTION
Constants	Elements that go into .const memory section
Scratch	Memory space that can be reused across different instances of the algorithm
Shared	Sum of Constants and Scratch
Instance	Persistent-memory that contains persistent information - allocated for each instance of the algorithm

Acronyms

ACRONYM	DESCRIPTION
625SD	Level 3.0 Maximum resolution format size 720x576
CIF	Common Intermediate Format
CPB	Coded Picture Buffer
D1	SDTV image resolution (720x480)
DMA	Direct Memory Access

ACRONYM	DESCRIPTION
EVM	Evaluation Module
HD	High Definition
HDVICP	High Definition Video and Imaging Co-Processor
MBAFF	Macro Block Adaptive Frame Field
PCM	Pulse Code Modulation
PicAFF	Picture Adaptive Frame Field
QCIF	Quarter Common Intermediate Format
QDMA	Quick Direct Memory Access
SDTV	Standard Definition Television
SEI	Supplemental Enhancement Information
SRAM	Static Random Access Memory
VGA	Video Graphics Array (640x480 resolution)
VUI	Video Usability Information
XDM	eXpressDSP Digital Media

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products

Audio	www.ti.com/audio
Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
RF/IF and ZigBee® Solutions	www.ti.com/lprf

Applications

Communications and Telecom	www.ti.com/communications
Computers and Peripherals	www.ti.com/computers
Consumer Electronics	www.ti.com/consumer-apps
Energy and Lighting	www.ti.com/energy
Industrial	www.ti.com/industrial
Medical	www.ti.com/medical
Security	www.ti.com/security
Space, Avionics and Defense	www.ti.com/space-avionics-defense
Transportation and Automotive	www.ti.com/automotive
Video and Imaging	www.ti.com/video
Wireless	www.ti.com/wireless-apps

TI E2E Community Home Page

e2e.ti.com

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2011, Texas Instruments Incorporated