EVM User's Guide: PGA300EVM, PGA305EVM, PGA900EVM

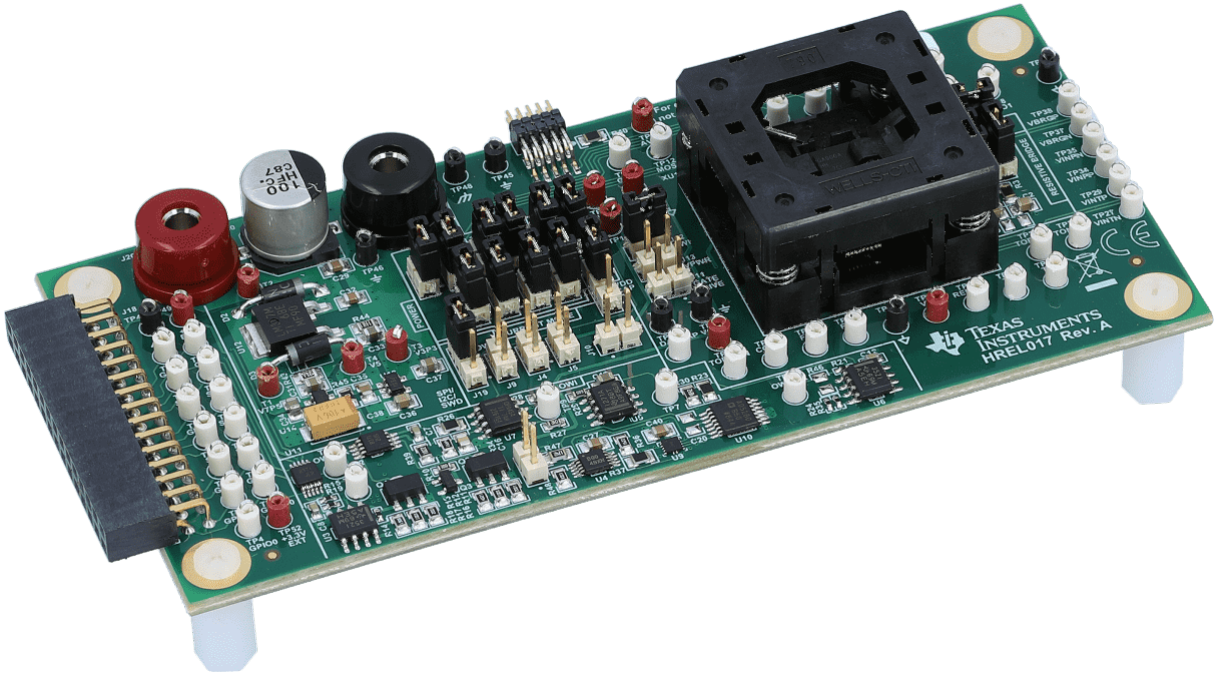
PGAx0xEVM-034 Evaluation Module

Description

The PGAx00 evaluation module (EVM) evaluates all the features of the PGA300 and PGA900 in either voltage mode or current mode. PGAx00EVM has a resistive bridge on board with a potentiometer allowing for differential input voltages to be adjusted by the user to emulate a pressure-sense element. The EVM also includes circuitry for I^2C and OWI communication.

Features

- Current-mode evaluation
- Voltage-mode evaluation
- XDS200 SWD interface
- OWI circuitry
- Circuit design is tested and includes GUI and getting-started guide



PGA900EVM

1 Evaluation Module Overview

1.1 Introduction

The PGAxxxEVM-034 supplies a platform to test the PGA900, PGA300, and PGA305 in the QFN package. The EVM is shipped as either the PGA900EVM-034, the PGA300EVM-034, or the PGA305EVM-034, with the name identifying the signal conditioner included in the EVM package. The PGAxxxEVM-034 supplies an interchangeable platform all of these devices can use.

Figure 1-1 shows the PGAxxxEVM-034 and labels the primary sections.

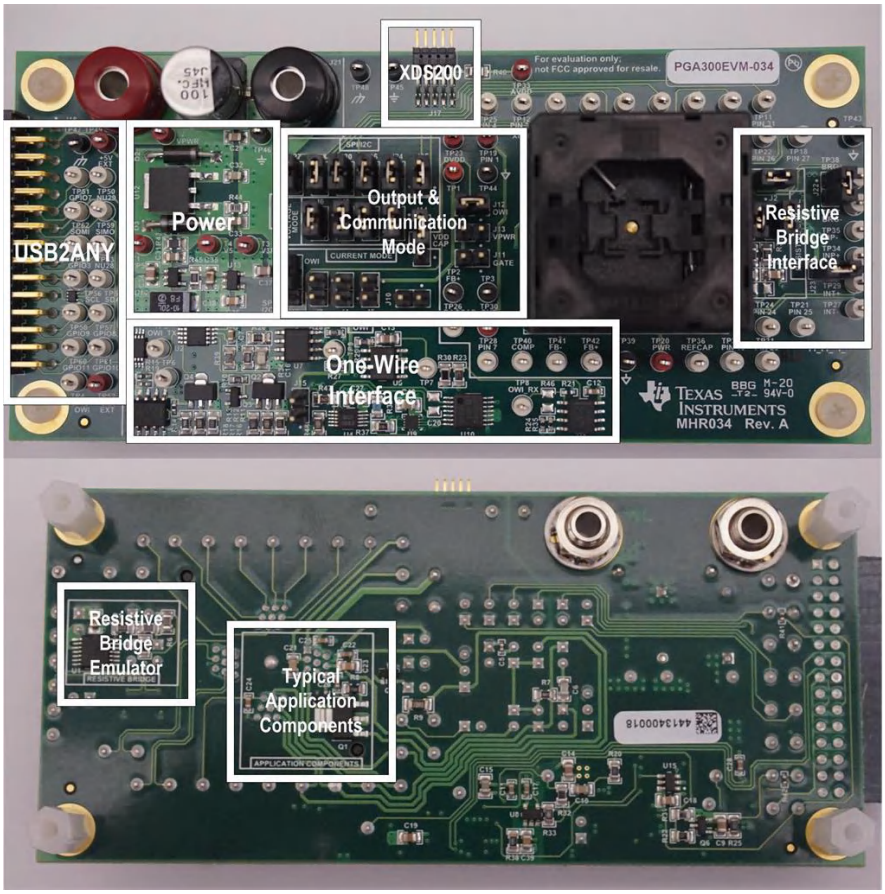


Figure 1-1. PGAxxxEVM-034

The PGAxxxEVM-034 is divided into six sections:

1. Interface boards and external power:
   a. USB2ANY connector
   b. XDS200 connector (single wire debugger)
   c. Banana connectors to power up EVM
2. Power:
   a. 7.5V, 5V, and 3.3V regulators
3. Mode selection:
   a. 4mA to 20mA loop (current mode)
   b. Voltage mode
4. OWI circuitry
5. Resistive bridge
6. Application components

The application components section only lists the required components for real-life applications using the PGA900/PGA300/PGA305 device. In this case, the application is configured for current mode.

Note

The PGA900, PGA300, and PGA305 have different features and pin functions, and some circuitry and communication features found on the PGAxxxEVM-034 are only applicable to the PGA900. Each device also has a unique Graphical User Interface (GUI) that communicates with the included USB2ANY board.

2 Hardware

2.1 Default Configuration

The EVM requires a 10 to 30V input applied to J20 and J21. Clamp the power supply current to 100mA. The shipped EVM is configured for voltage mode as shown in Table 2-1.

Table 2-1. Jumper Settings for PGAxxxEVM-034 in Voltage Mode

Jumper	Setting	Function
J12	Closed	PGAxxx powered up from OWI circuitry (VDD = 5V)
J1, J2, J3	Closed	Connect resistive bridge to PGA900
J6, J7, J8	Closed	Voltage mode with a 100nF load
J24, J25, J26, J27, J28, J30	Closed	SPI/I^2C/UART enabled (only applicable to PGA900)
J16	Closed	Connect ASIC_GND to IRETURN
J14	Pins 1-2 closed	Connect VDD cap to ASIC_GND
J19	Pins 2-3 closed	Connect USBGND to IRETURN

2.2 Inputs and Output Configurations

2.2.1 Pressure Input

The PGAxxxEVM-034 has a resistive bridge where one leg of the bridge can be changed using a digital potentiometer. The changing leg has two digital potentiometers connected in parallel in series with a 4.7kΩ resistor. J1 must be closed to connect the bridge voltage from the PGAxxx device to the resistive bridge. The J2 and J3 must also be closed to connect the bridge outputs to the PGAxxx. An RC filter is in series with each of the input pins in the PGAxxx with a cutoff frequency of approximately 106Hz. Figure 2-1 shows the pressure stimulus circuit in the PGAxxxEVM-034.

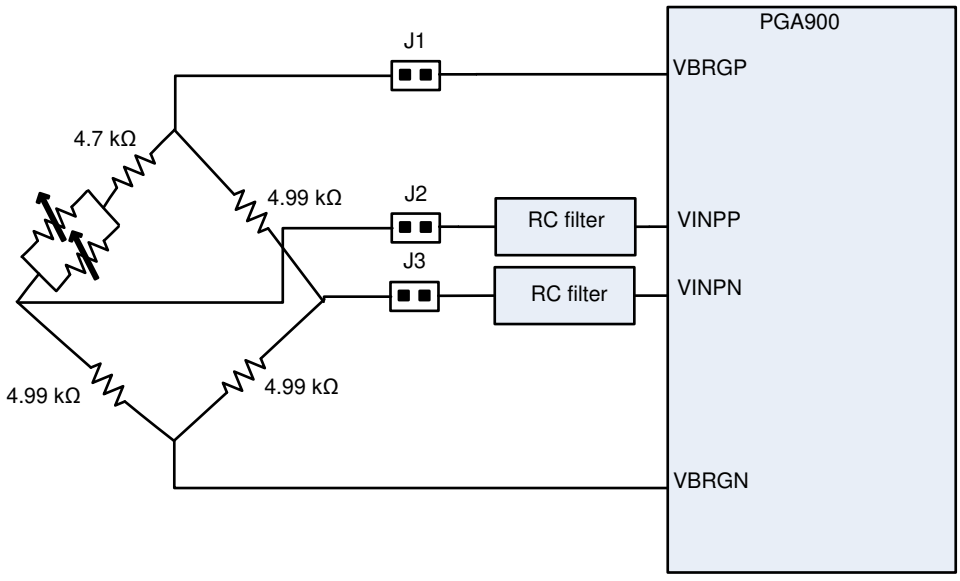


Figure 2-1. Pressure Stimulus in the PGAxxxEVM-034

2.2.2 Temperature Input

The PGAxxxEVM-034 does not have on-board stimulus for the temperature inputs of the PGAxxx, but the TP27 and TP29 on the far-right side of the board can be used to apply external signals.

2.2.3 Output

The PGAxxxEVM-034 can be configured for voltage or current mode (4mA to 20mA loop). Each mode requires different jumper settings as shown in the following sections.

2.2.4 Voltage Mode

The PGAxxxEVM-034 is by default configured in voltage mode with a 100nF load. A compensation capacitor and an isolation resistor are necessary for stability. Figure 2-2 shows the PGAxxx schematic for voltage mode and Table 2-1 shows all the jumpers necessary to configure the board in this mode. If the capacitive load is different from 100nF, then the isolation resistor and compensation capacitor values must be changed. Refer to the application note *PGA900 as a Capacitive Load Driver* (SLDA020) for more information.

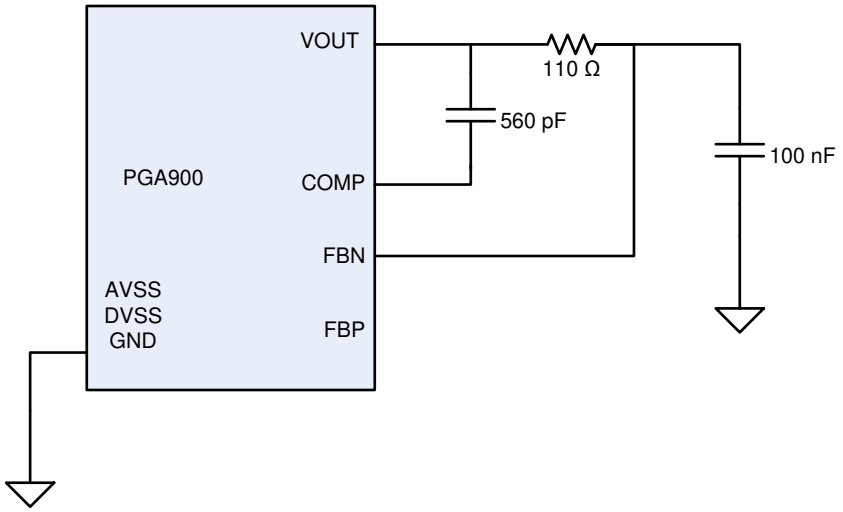


Figure 2-2. PGA900 in Voltage Mode Configuration

Note

If the designer wants the VDD to be higher than 5V in voltage mode, open J12 and close J13. VDD is equal to the power applied to the PGAxxxEVM-034.

2.2.5 Current Mode

When in current mode, the PGAxxxEVM-034 must be properly configured to separate the different negative references for all the voltage levels present in the board. Figure 2-3 shows the primary connections for current mode. The two scenarios in current mode are:

- Current mode using OWI
- Current mode using SPI/I^{2}C/SWD (only applicable to the PGA900 or the PGA305 in I^{2}C mode)

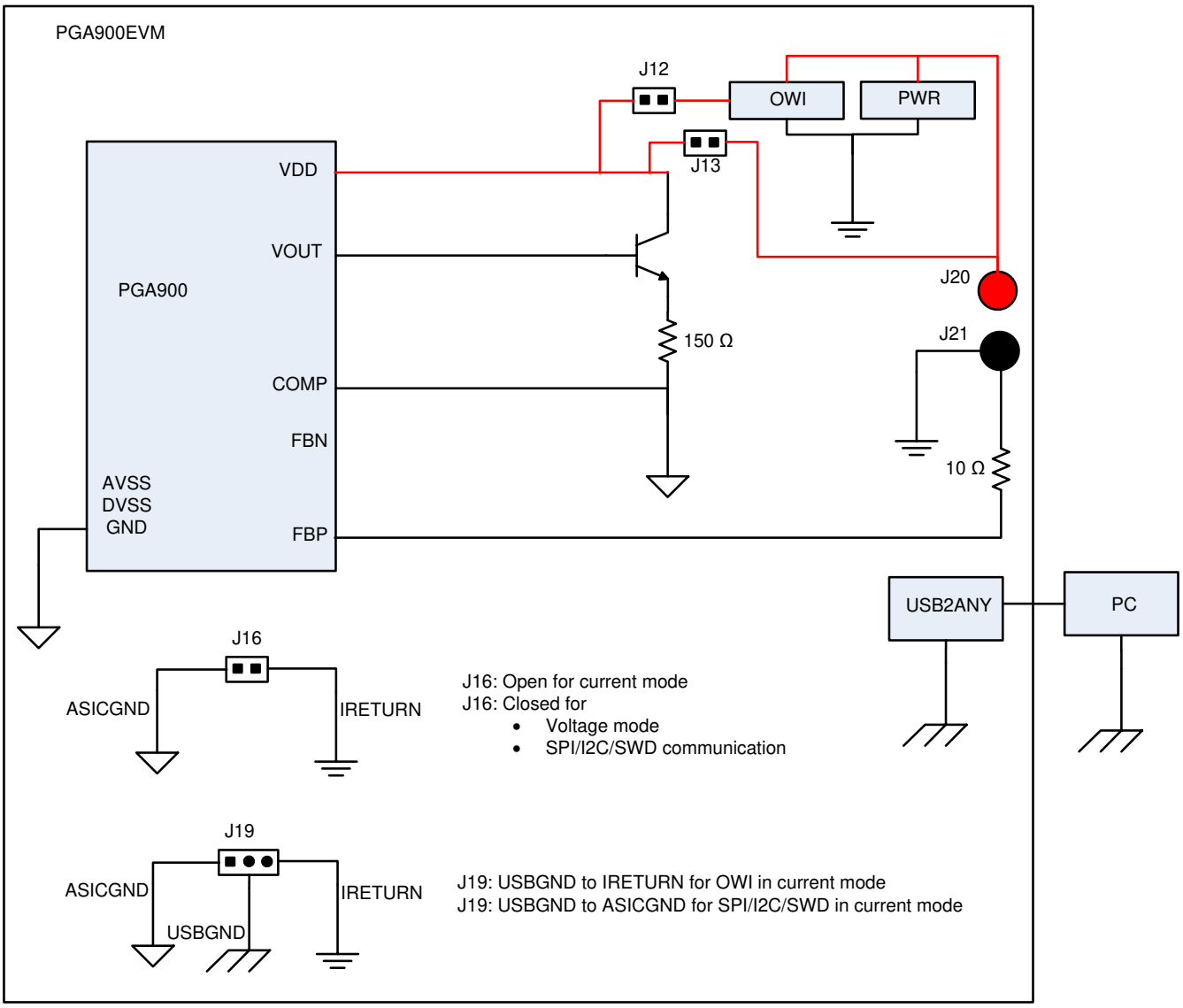


Figure 2-3. PGAxxxEVM-034 in Current Mode

Note

When in current mode, the input voltage to the EVM (J20 and J21) needs to be at least 20V.

2.2.6 OWI and SPI, I²C, SWD in 4mA to 20mA Current Loop

Remember that when in current mode, there are two different scenarios depending on whether OWI or SPI or I²C/SWD is used as the type of communication for the PGA900. The PGA300 only allows communication through OWI, so always follow the settings found on Table 2-3 when using the PGA300 in current mode. Table 2-2 shows the jumper settings necessary for each of these scenarios. Refer to Figure 2-3 for the locations of the jumpers. The PGA305 allows communication through OWI or through I²C. When using OWI communication with the PGA305 device in current mode, refer to the same settings used for the PGA300 listed earlier. For I²C communication with the PGA305 in current mode, use the same settings as those used for I²C communication with the PGA900 in current mode.

Table 2-2. Jumper Settings for PGA900EVM-034 in Current Mode Using SPI/I2C/SWD

Jumper	Setting	Function
J16	Open	Disconnect ASIC_GND from IRETURN
J19	Pins 1-2 closed	Connect USBGND to ASICGND
J13	Closed	Connect PGA900 VDD pin to EVM input voltage
J6	Open	Disconnect 180pF between COMP and VOUT
J9	Closed	Connect COMP to ASIC_GND
J4	Closed	Short out resistor at VOUT
J8	Open	Disconnect FBN from VOUT
J5	Closed	Connect VOUT to BJT
J7	Open	Lift 100nF Voltage-mode load Capacitor at base of BJT
J10	Closed	Connect FBP to IRETURN through 10Ω resistor
J14	Pins 1-2 closed	100nF capacitor from VDD to FBP and from DACCAP to FBP
J12	Open	Disconnect PGA900 VDD pin from OWI signal from EVM
J25, J27	Closed	If I²C is desired
J24, J26, J28, J30	Closed	If SPI/UART is desired

Table 2-3. Jumper Settings for PGAxxxEVM-034 in Current Mode Using OWI

Jumper	Setting	Function
J16	Open	Disconnect ASIC_GND from IRETURN
J19	Pins 2-3 closed	Connect USBGND to IRETURN
J13	Open	Disconnect PGA900 VDD pin from EVM input voltage
J6	Open	Disconnect 560pF between COMP and VOUT
J9	Closed	Connect COMP to ASIC_GND
J4	Closed	Short out resistor at VOUT
J8	Open	Disconnect FBN from VOUT
J5	Closed	Connect VOUT to BJT
J7	Open	Lift 100nF Voltage-mode load Capacitor at base of BJT
J10	Closed	Connect FBP to IRETURN through 10Ω resistor
J14	Pins 1-2 closed	100nF capacitor from VDD to FBP and from DACCAP to FBP
J12	Closed	Connect VDD in PGA900 to OWI signal from EVM
J25, J27	Open	Disconnect I²C pins between USB2ANY and PGA900
J24, J26, J28, J30	Open	Disconnect SPI/UART pins between USB2ANY and PGA900

The PGA300 and PGA305 are prepared for OWI communication and do not require additional device configuration.

For the PGA900, OWI in current mode can only be used with appropriate firmware programmed in the device. The firmware needs to:

1. Enable the OWI interrupt and service when the activation sequence on VDD is received by the device.
2. Set the deglitch time to the 1ms default time (OWI_DGL_CNT_SEL = 0).
3. Disconnect the DAC output from the loop by setting bit 0 of AMUX_CTRL to 0.
4. Enable the OWI transceiver and reset M0 by writing 0x03 to MICRO_INTERFACE_CONTROL register.

When in 4mA to 20mA loop configuration, there is additional current from ASIC_GND (GND of PGA900) to IRETURN (return path for the loop current) that is caused by the voltage difference created by the 40Ω resistor inside the PGA900 and the 10Ω (R9) EVM resistor. This additional current is due to the U11 (when in SPI/I2C/SWD communication) and U1 (digital potentiometer in the resistive bridge). Figure 2-4 and Figure 2-5 show this additional current. As a result, the designer needs vto lift J22 and J23 to isolate U1 and needs to use OWI when using the PGAxxxEVM-034 if the designer wants accurate calibration (firmware required) in 4mA to 20mA mode.

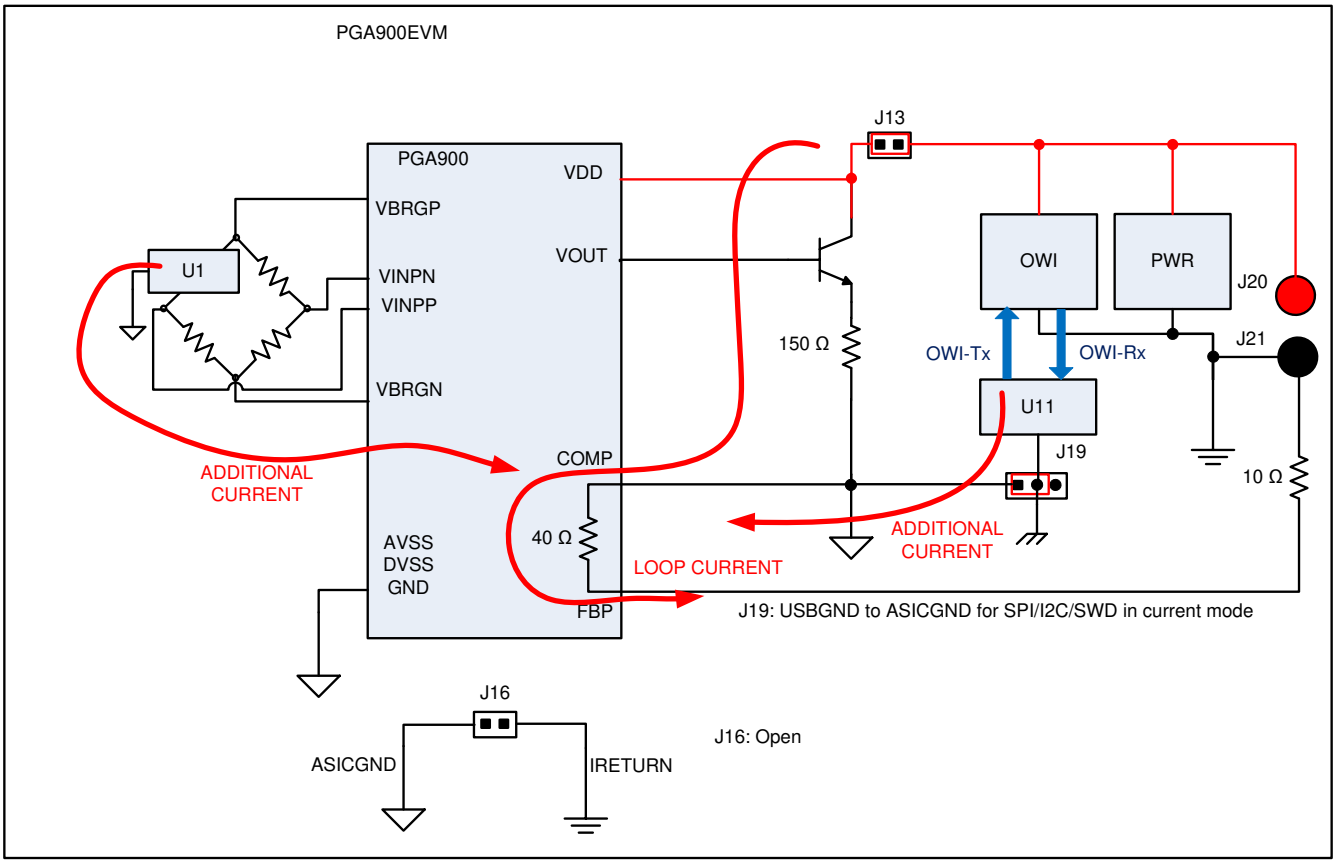


Figure 2-4. Additional Loop Current in 4mA to 20mA Mode When Using SPI, I2C, SWD as Digital Interface

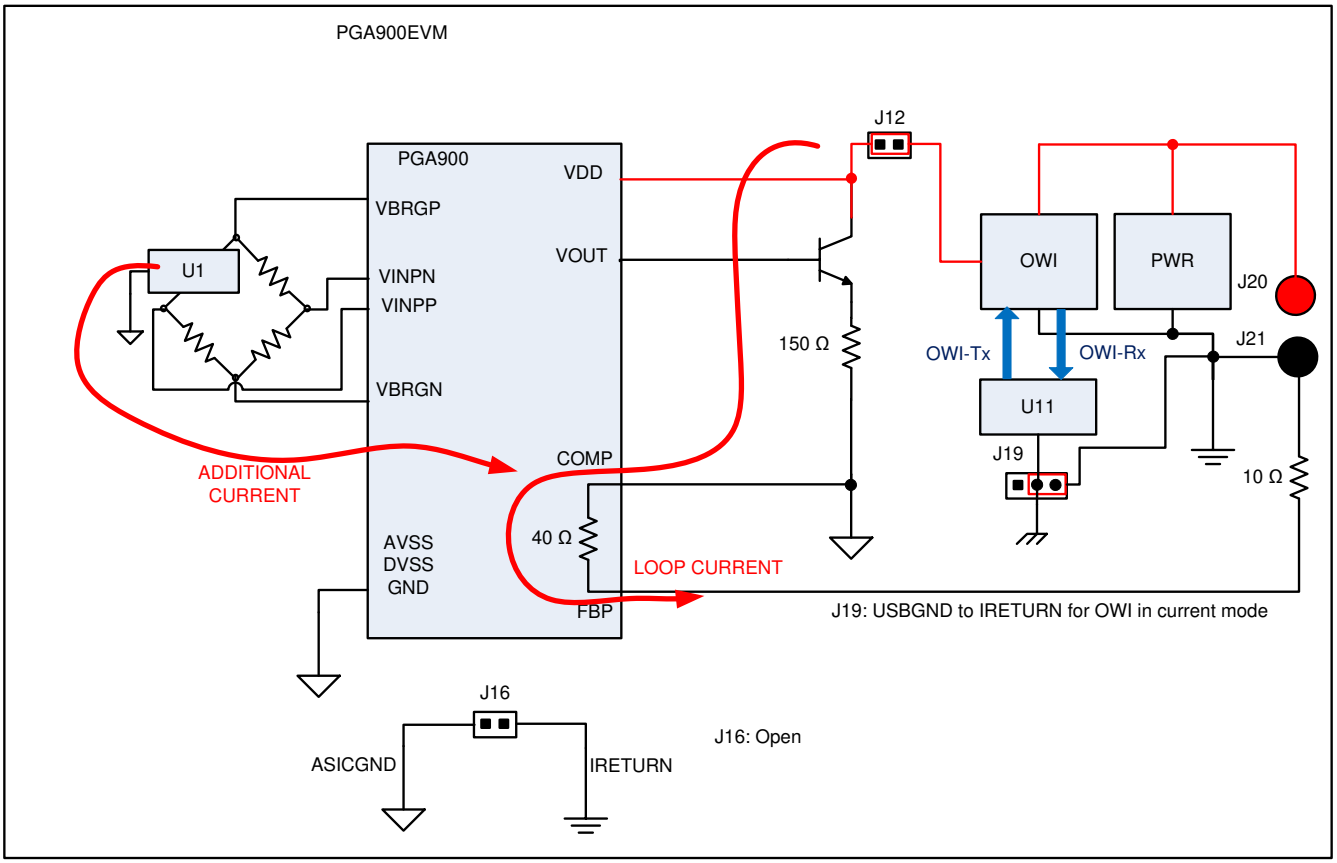


Figure 2-5. Additional Loop Current in 4mA to 20mA Mode When Using OWI as Digital Interface

2.3 OWI

The OWI circuitry in the PGAxxxEVM-034 allows the designer to communicate with the PGA900, PGA300, and PGA305 through voltage level translation and current sensing circuitry. The OWI circuitry is based on a summing amplifier using the OPA454. This is because the current mode application where the GND reference for the PGA900 (ASIC_GND) is at a higher potential than the reference for the OWI circuitry (IRETURN). This is due to the internal 40Ω resistor and the 10Ω (R9) EVM resistor connected to FBP. However, this resistor can be a higher value, and as expected, the potential difference is larger and is current-dependent. The summing amplifier principle compensates for these voltage differences so that the OWI logic levels (with respect to the ASIC_GND) always remain the same, regardless of current. The OWI circuitry, shown in Figure 2-6, consists of four primary blocks:

1. OWI write: UART data and activation pulses level translated to OWI voltage logic levels.
2. Offset voltage: Constant offset voltage selected by the user to compensate for constant drops from components such as diodes. This is only necessary when operating the device in current mode. In voltage mode, the offset voltage needs to be set to 0V.
3. Current compensating voltage: This additional voltage is only necessary when operating the device in current mode to compensate for the voltage difference between the PGA900 ground and the OWI circuitry ground due to the loop current. In voltage mode, the gain of the OPA734 needs to be set to unity gain.
4. OWI read: Current to voltage and voltage level translation to UART voltage logic levels.

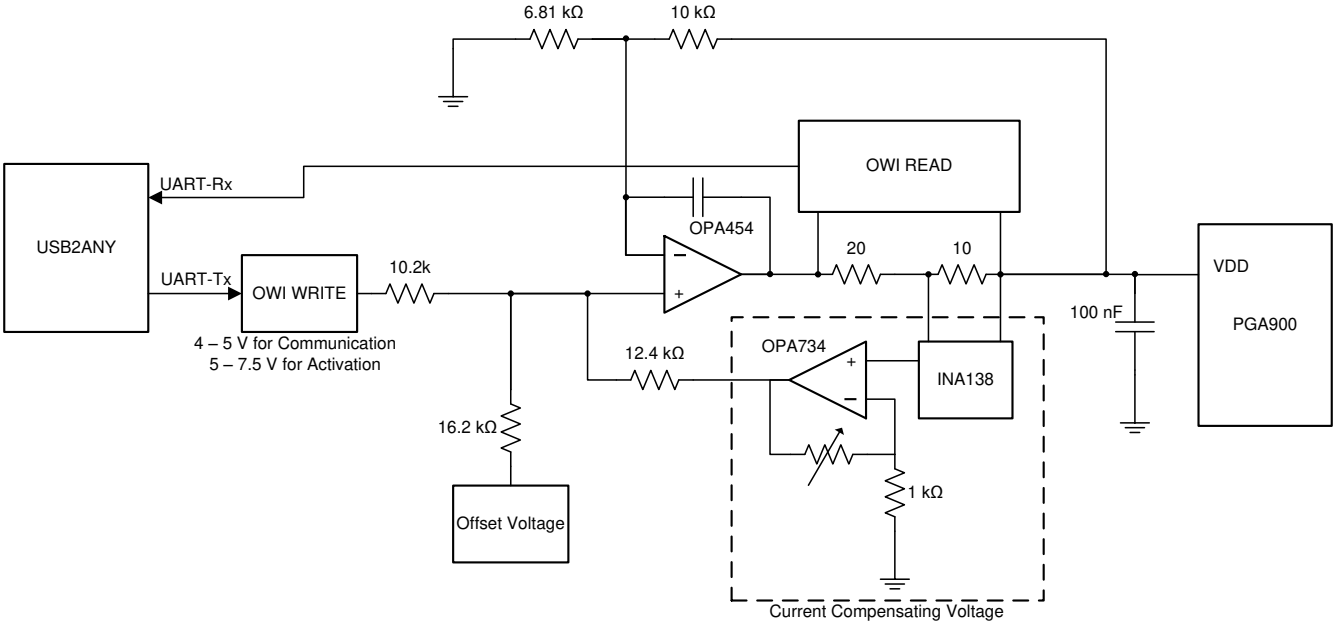


Figure 2-6. OWI Block Diagram

2.3.1 Activation Pulse

The activation pulse generated by the PGAxxxEVM-034 generates the OWI interrupt necessary to activate the OWI (with the proper firmware developed by the user). Figure 2-7 shows the activation pulse from the PGAxxxEVM-034.

- In the PGA900 and PGA305 GUIs, to use this activation pulse, select the *Through Pulse* option from the *OWI Activation Mode* menu and then click *OWI*. The duration of the activation pulse varies due to software delays, but the minimum requirement of 1 or 10ms is always met. If the pulse is not necessary, then OWI can also be enabled through I^2C. To select this option, select *Through I2C* from the *OWI Activation Mode* menu, and then click *OWI*.
- In the PGA300 GUI, the activation pulse is sent as soon as the designer presses *Activate OWI*. The pulse is sent as defined in the PGA300 data sheet.

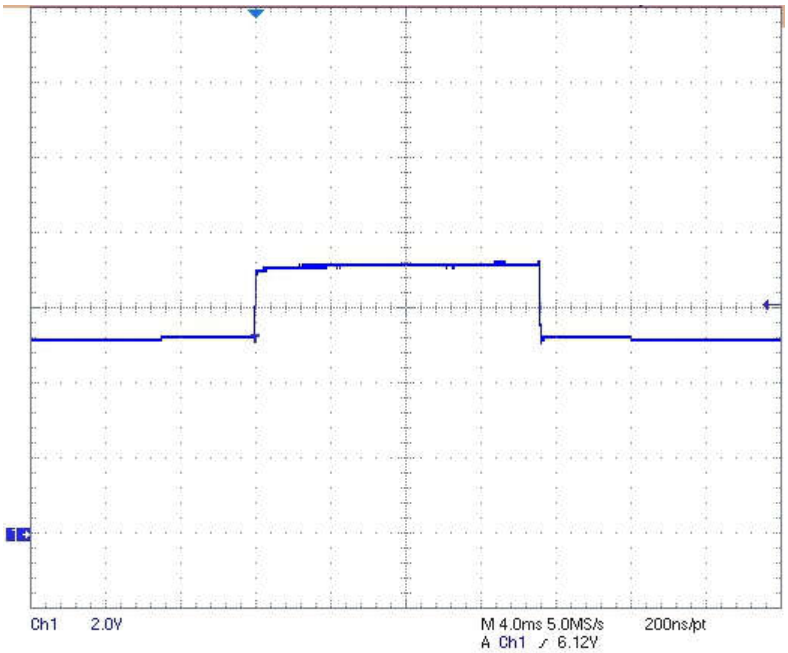


Figure 2-7. OWI Activation Pulse for the PGA900 Generated by the PGAxxxEVM-034 in Voltage Mode

2.3.2 Data Sent Through OWI

Data through OWI can be sent to the PGA900/PGA300/PGA305 at rates between 320 to 9600bps. Figure 2-8 shows data sent at 320bps.

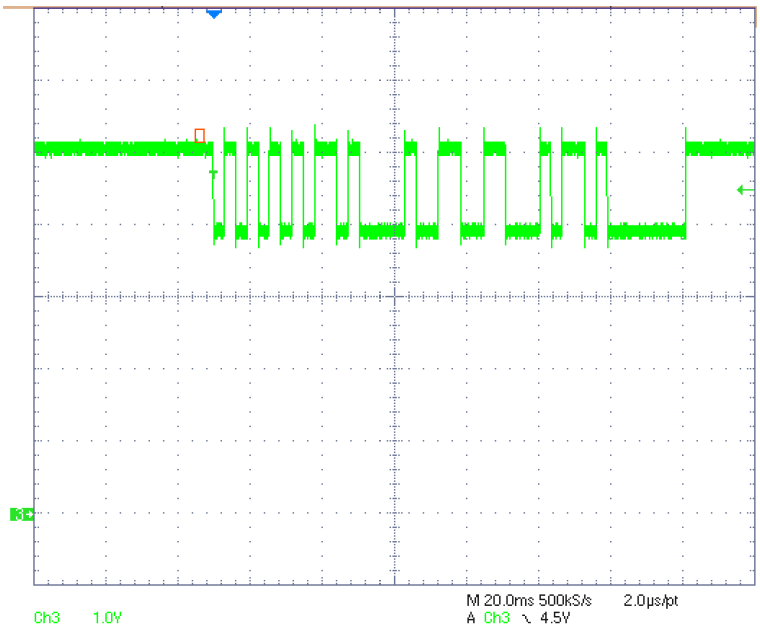


Figure 2-8. OWI Data at 320bps; Oscilloscope Probe is Connected at TP20 in the PGAxxxEVM-034

2.4 XDS200 and USB2ANY Connectors

The XDS200 is used for the single-wire debugging (SWD) feature of the PGA900. The designer must use a small breakout board (part of the XDS200 kit) to connect to J17 in the PGA900EVM-034. No external connections are necessary. Figure 2-9 shows the proper connection for the XDS200 emulator.

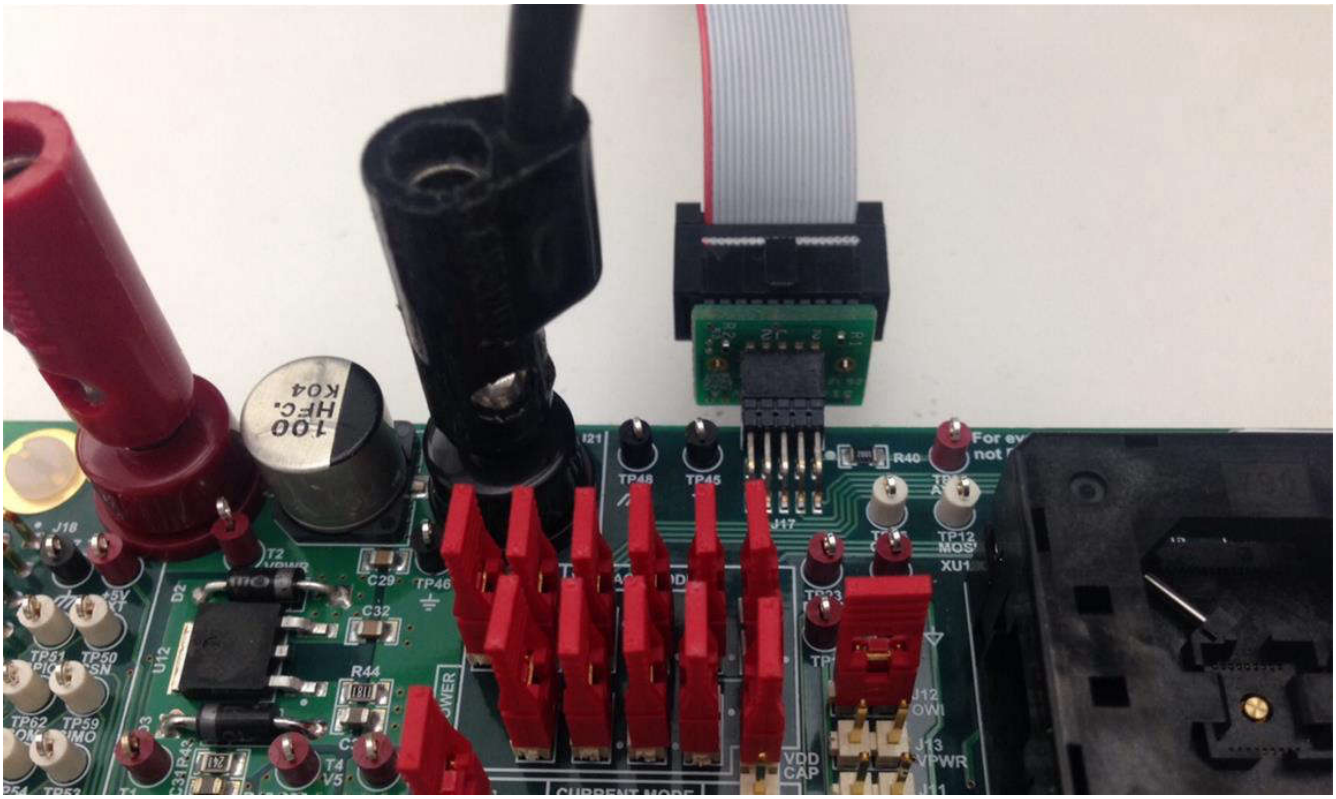


Figure 2-9. XDS200 Emulator Connection to the PGAxxxEVM-034

The USB2ANY is used for the different communication protocols supplied by the PGA900/PGA300/PGA305. The USB2ANY connects to J18 in the PGAxxxEVM-034 as shown in Figure 2-10. The USB2ANY hardware is based on the TI MSP430F5529, 16-bit microcontroller with integrated USB 2.0. The PCB is a two-layer, single-sided board with minimal component count. There are two versions of the USB2ANY, shown in Figure 2-11, one enclosed and one open. The functionality is the same for both.

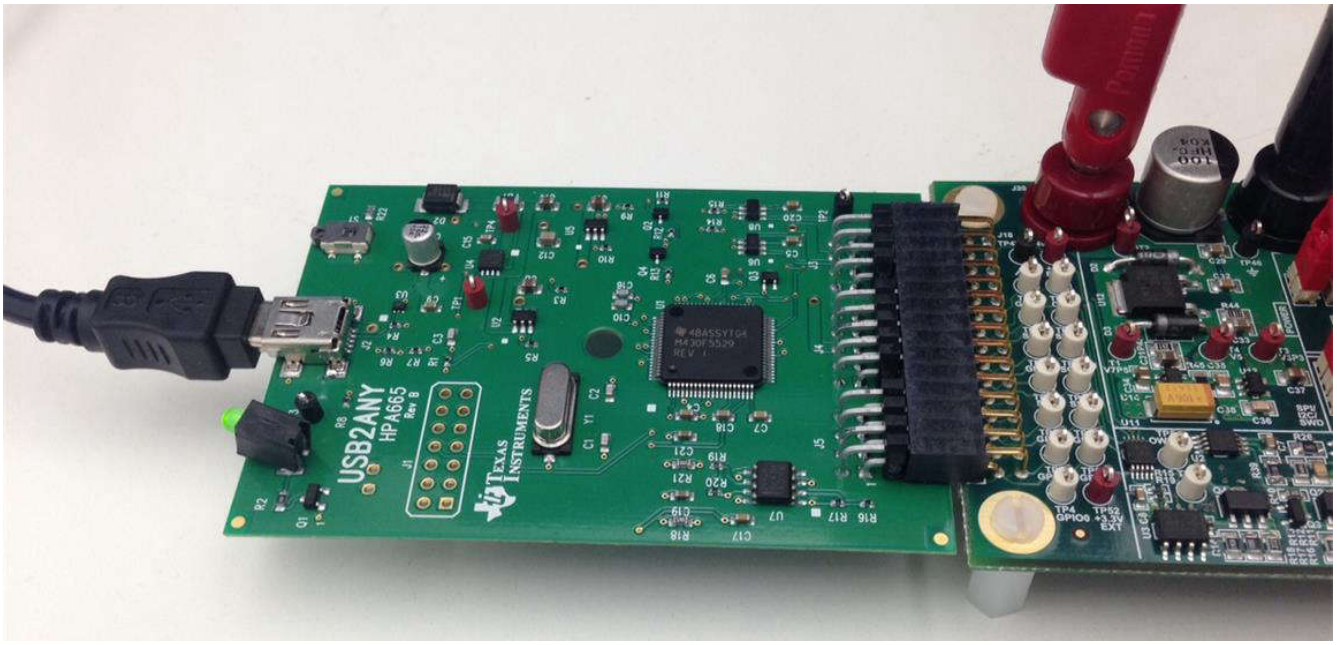


Figure 2-10. USB2ANY Connection to the PGAxxxEVM-034

Figure 2-11. USB2ANY

Figure 2-12 shows the pinout of the USB2ANY. The ribbon cable can only be connected one way to the USB2ANY due to a latch present in the cable. A USB cable is included to connect the device to the PC. No external supply is necessary.

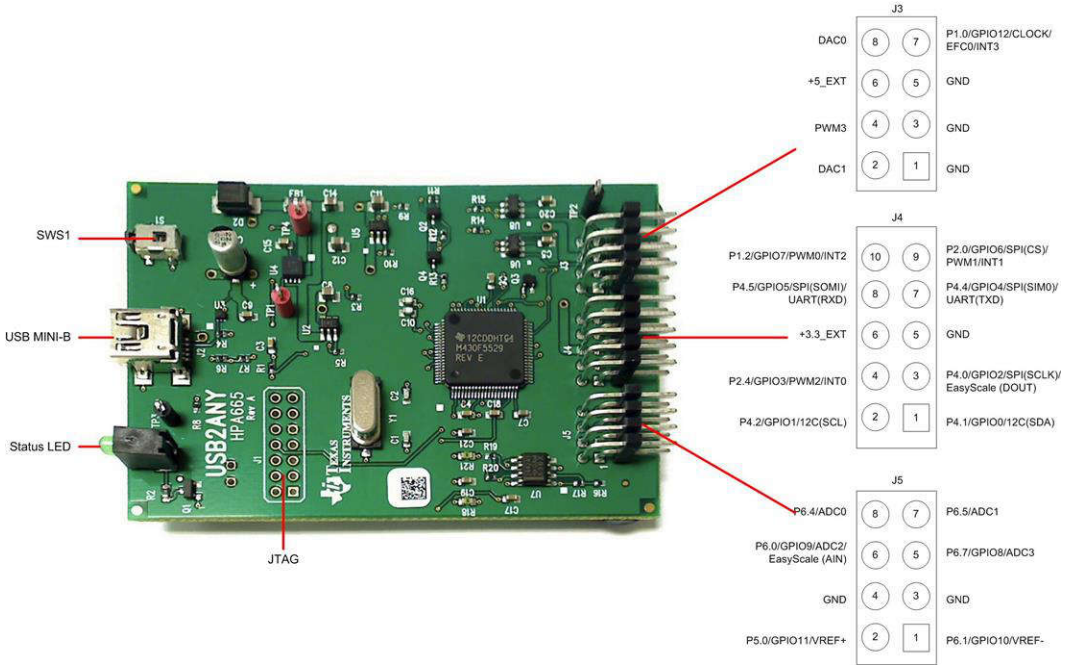


Figure 2-12. USB2ANY Pinout

2.5 Power Supplies in the PGAxxxEVM-034

The PGAxxxEVM-034 requires an input voltage between 10V to 30V to properly operate. Figure 2-13 shows the different power options in the PGAxxxEVM-034.

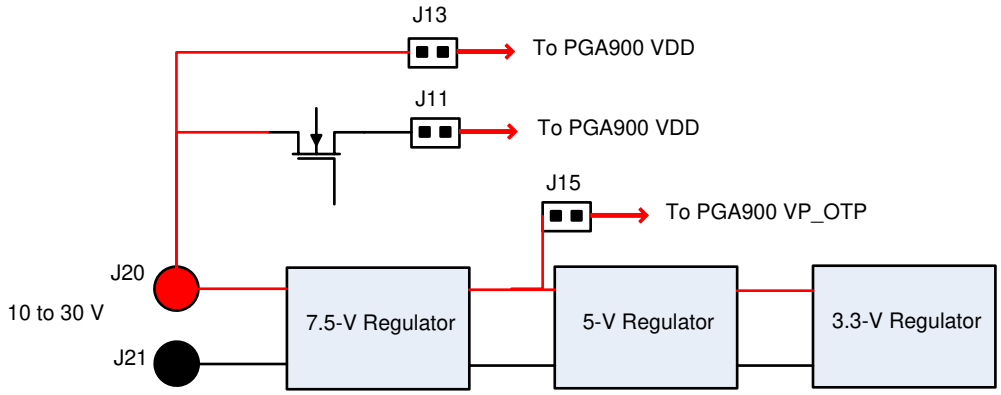


Figure 2-13. Power Distribution in PGAxxxEVM-034

Note

J15 must be closed during OTP programming. This is only applicable for the PGA900. The PGA300 has no OTP functionality.

3 Hardware Design Files

3.1 Schematics

Figure 3-1 through Figure 3-6 show the PGAxxxEVM-034 schematics.

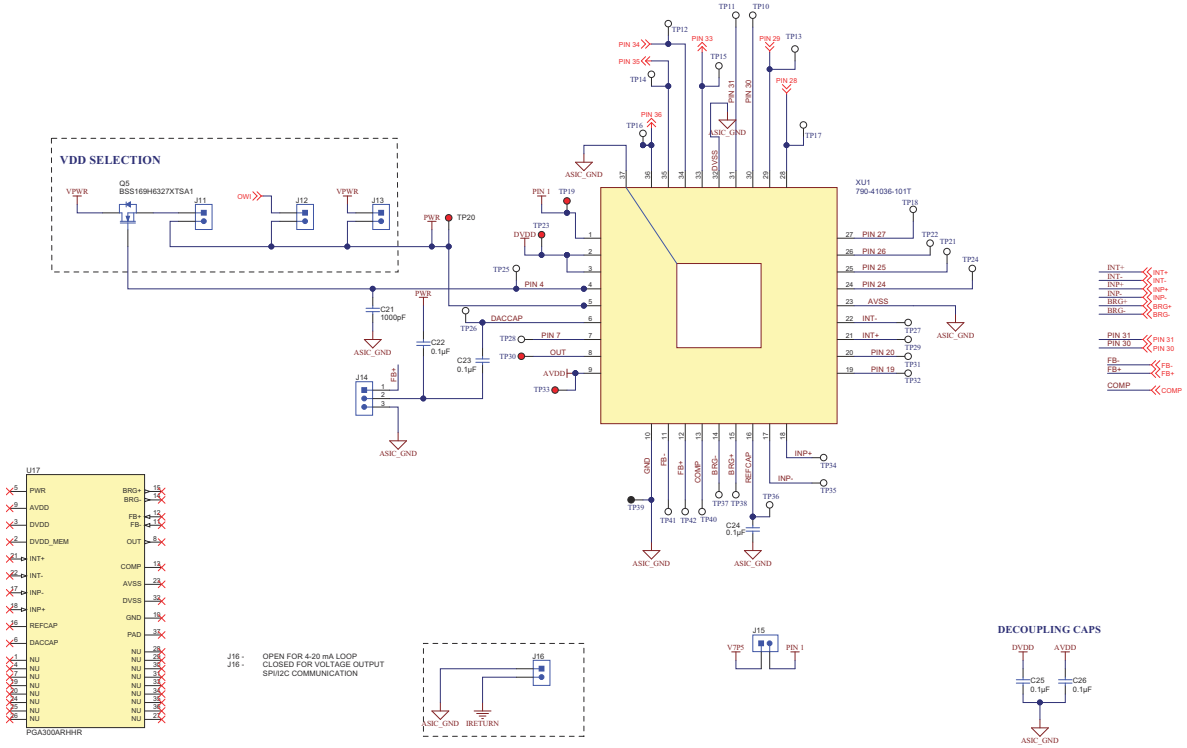


Figure 3-1. PGAxxxEVM-034 Main Schematic

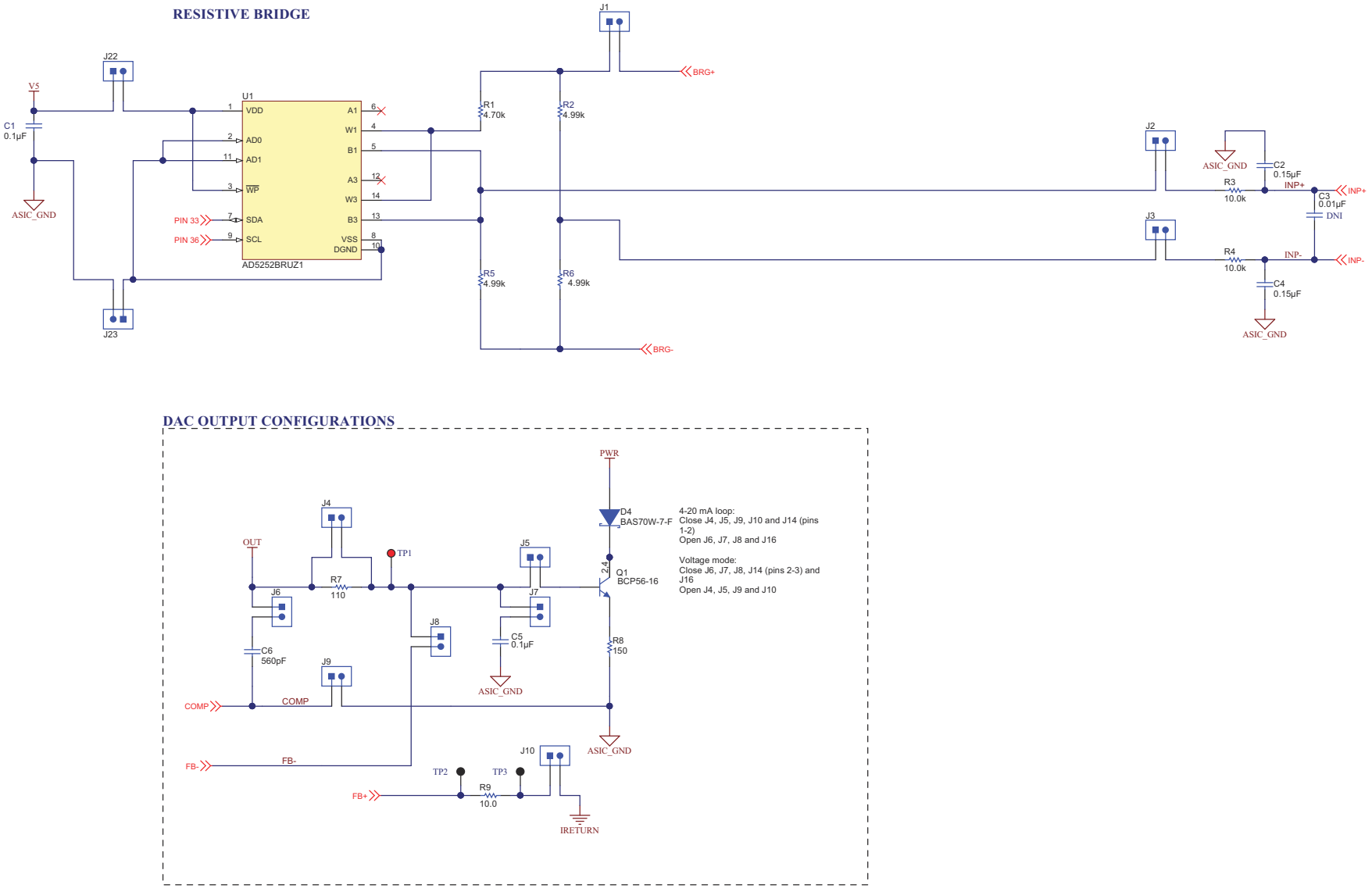


Figure 3-2. Input and Output Schematic

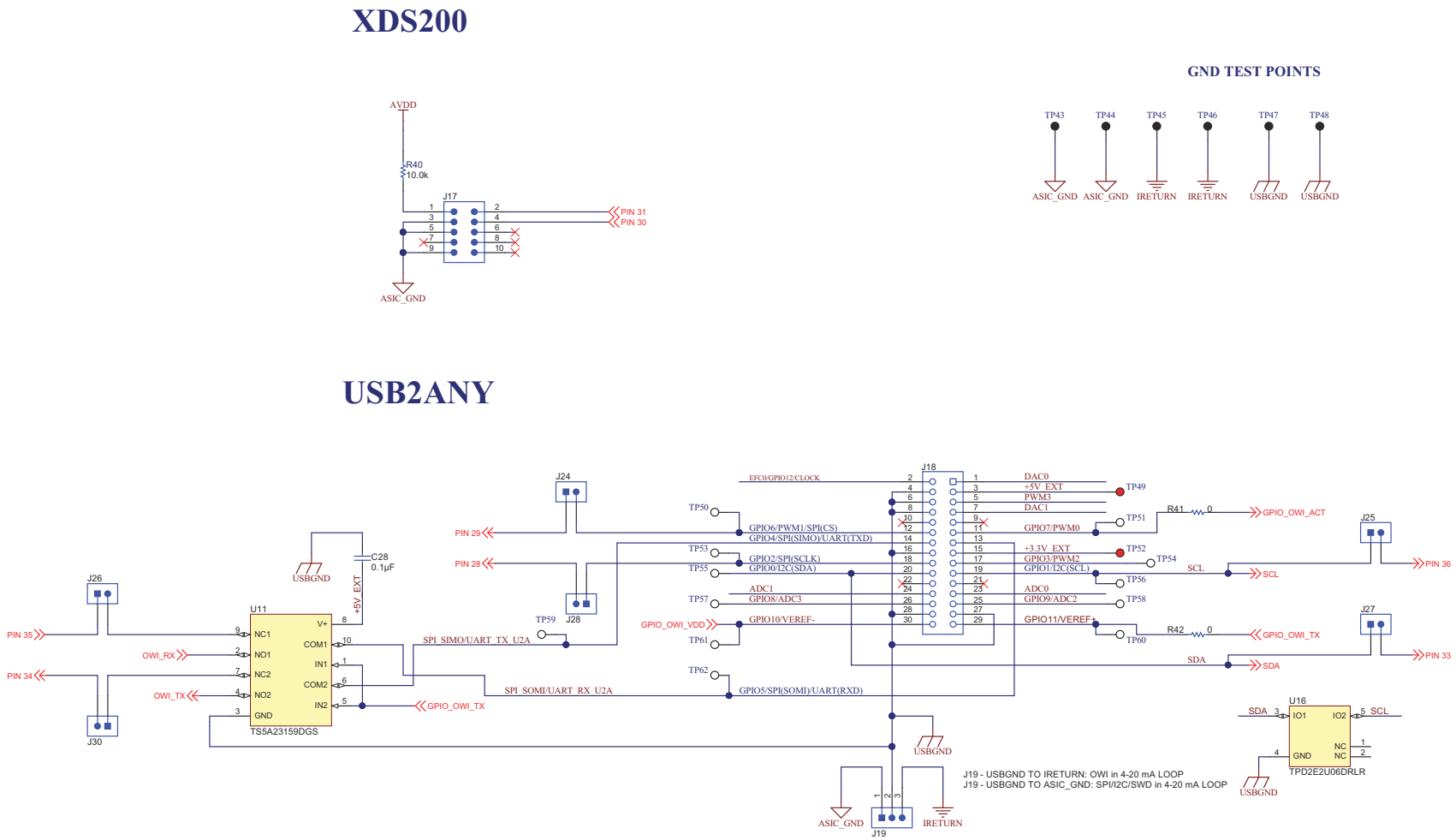


Figure 3-3. USB2ANY Schematic

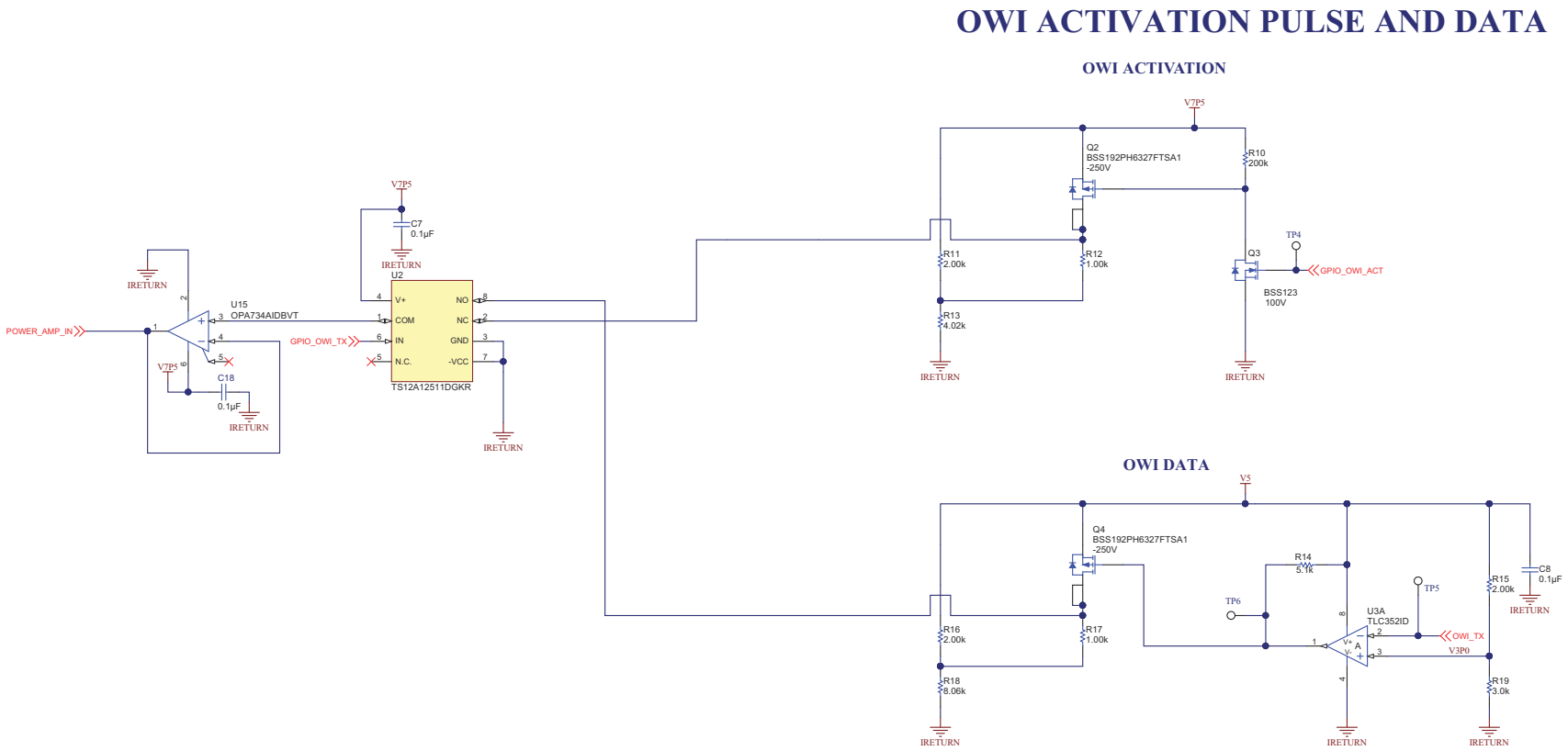


Figure 3-4. OWI Activation Pulse and Data Schematic

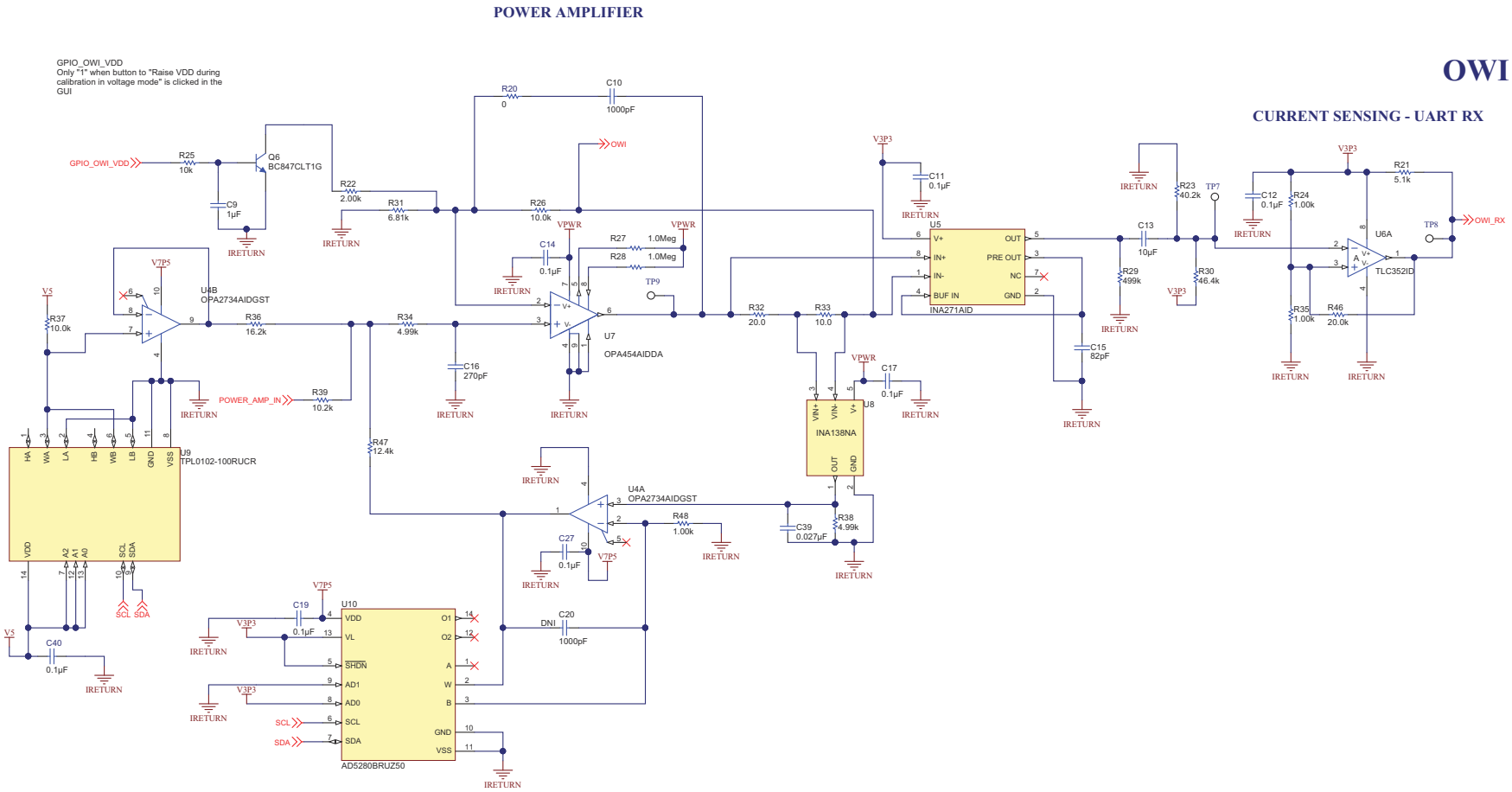


Figure 3-5. OWI Power Amplifier Schematic

POWER SUPPLIES

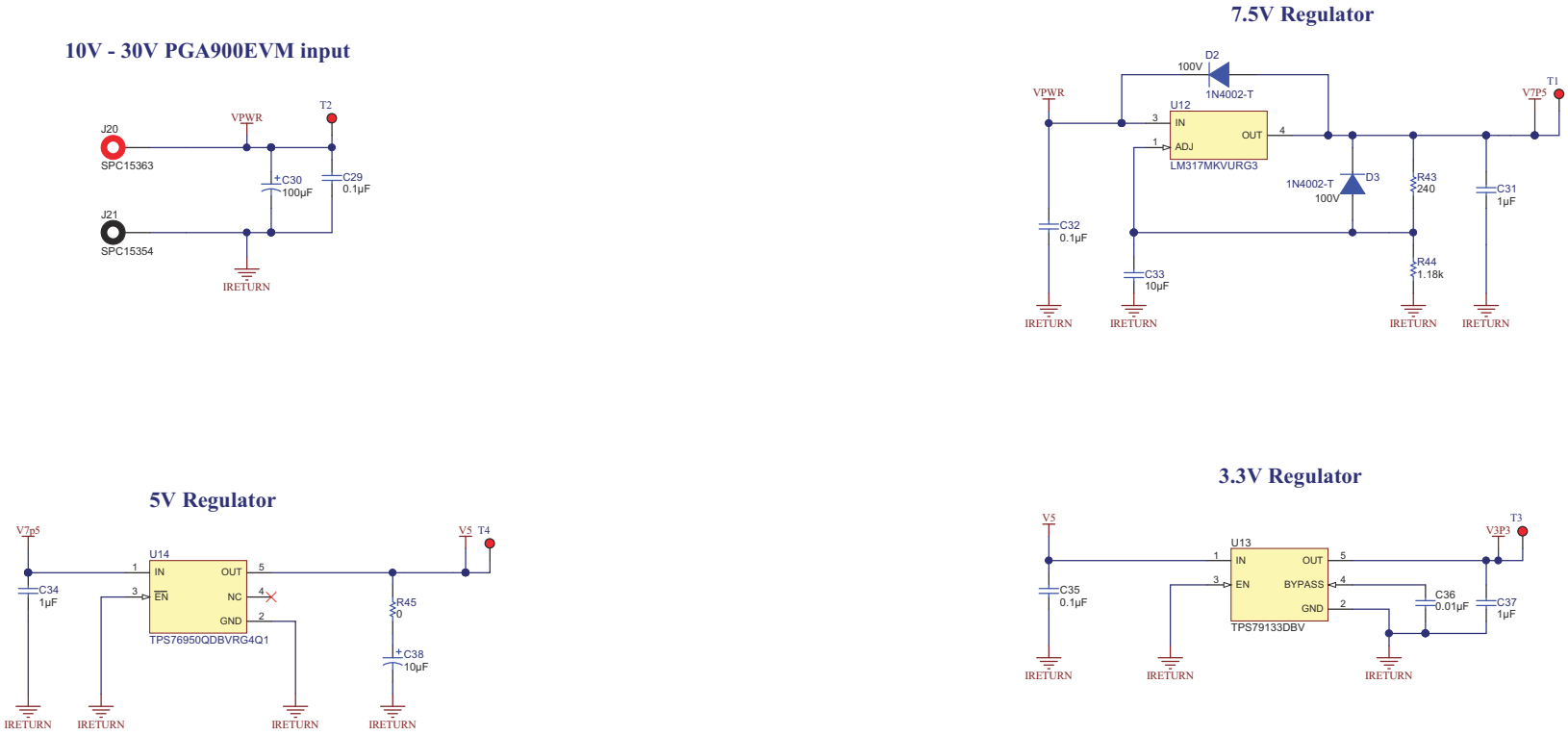


Figure 3-6. Power Supplies Schematic

4 Additional Information

4.1 Trademarks

All trademarks are the property of their respective owners.

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (August 2018) to Revision C (July 2024)	Page
• Added Selective Disclosure banner on document	1

Changes from Revision A (June 2016) to Revision B (August 2018)	Page
• Added references for PGA305EVM	2

Changes from Revision * (May 2015) to Revision A (June 2016)	Page
• Updated Table 2-2	6
• Added Table 2-3	6
• Additional current discussion when in 4mA to 20mA mode	6
• Added Figure 2-4	6
• Added Figure 2-5	6
• Added note regarding jumper for OTP voltage	14
• Updated designator for J16 in Figure 3-1	15
• Updated designators for text in DAC Output Configurations in Figure 3-2	15
• Updated designator for J19 in Figure 3-3	15

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265