User's Guide

AFE20408 Application User's Guide

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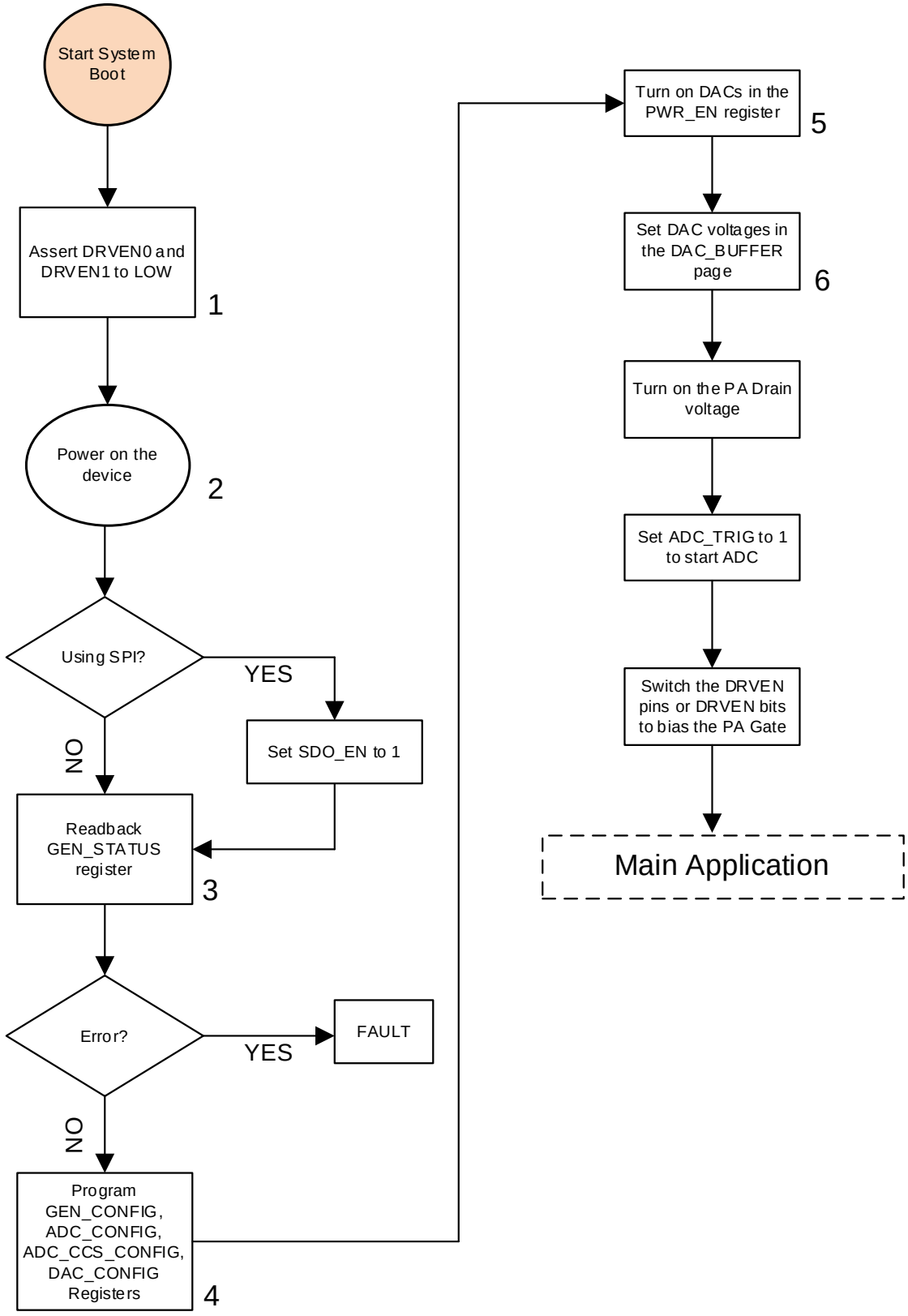
This document describes specific application use cases in detail. The document describes the AFE20408 start up sequence, main application loop, and the alarm control loop.

This user's guide is meant to be used alongside the AFE20408 datasheet.

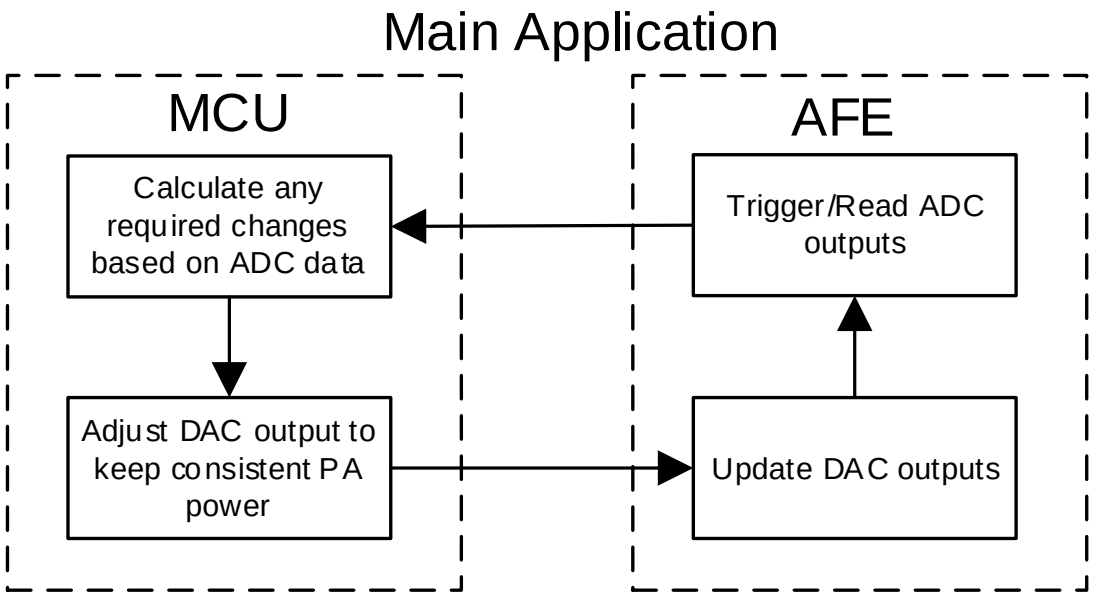
1 AFE20408 START UP Sequence



The start-up sequence flow chart gives a general overview of how to start up the device.

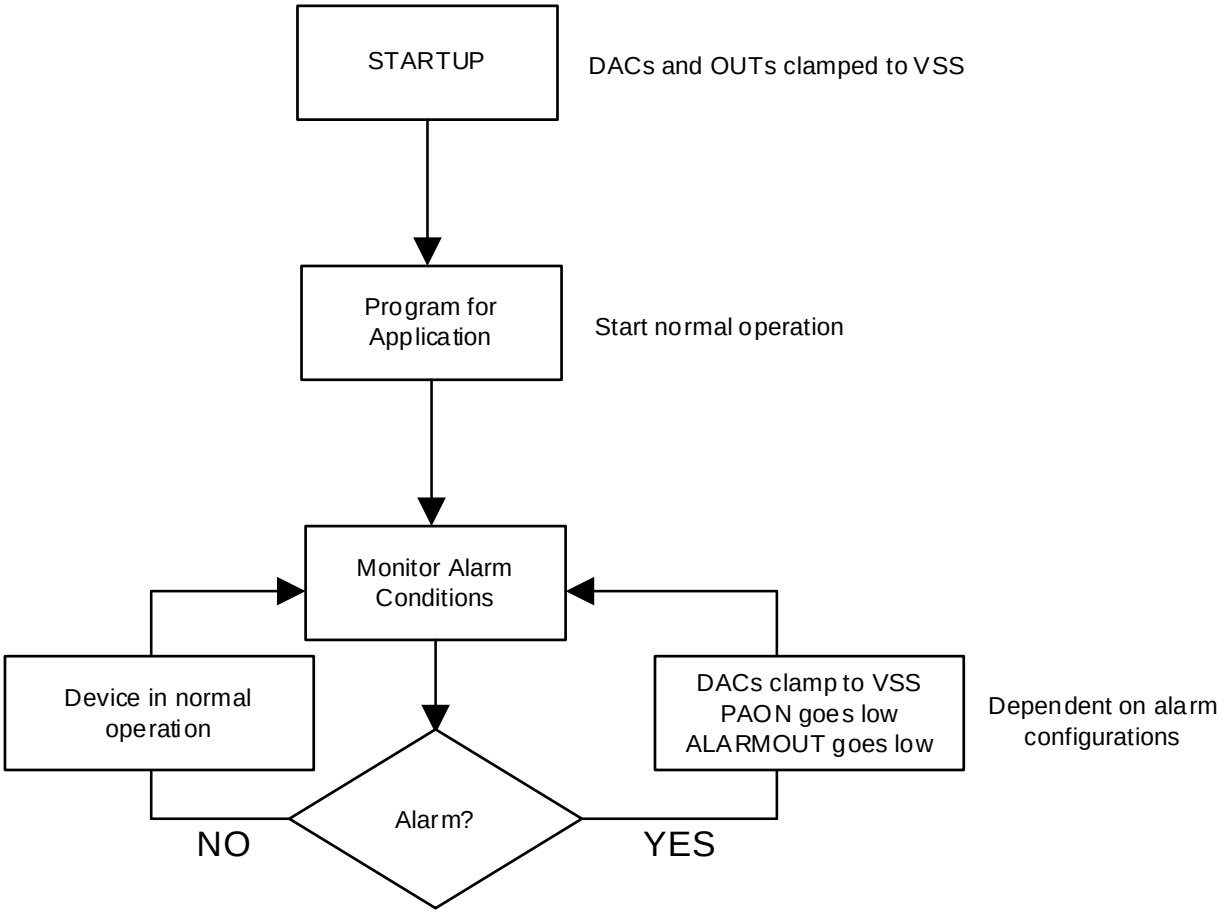
1) Make sure the DRVEN0 and DRVEN1 pins are set to LOW. This is to ensure the outputs stay clamped during startup.
2) Power on the AFE20408. The device does not have a required sequencing order. When the device starts up, all outputs (DACs, OUTs, and PAON pins) will be low. DACs and OUTs will be clamped to VSS and will stay that way until the AFE is programmed.
3) Use the MCU to read back the GEN_STATUS_REGISTER, register 0x03. Only the NVM_Loaded (bit 14) bit should be 1. If other bits are 1, then the AFE20408 has detected an alarm and needs to be debugged.
4) If there is no alarm, begin programming the AFE20408 for the application.
    a. Page 0 GEN_CONFIG: Configure the alarms and general device operation.
    b. Page 1 ADC_CONIG: Configure the ADC operation. This page includes low and high alarm thresholds for the ADC monitoring.
    c. Page 2 ADC_CCS_CONFIG: Configure the Custom Channel Sequencing for the ADC.
    d. Page 3 DAC_CONFIG: Configure the DAC operation.
5) Once the AFE is configured, the DACs are ready to be enabled. Turn on the DACs in the PWR_EN register, 0x08.
6) Set the desired DAC voltages in page 4, DAC_BUFFER. The DACs provide the pinch-off and bias voltages for the PA gate. At this time, the DACs will be on and set to the desired levels. The OUT pins (which is nominally used to bias the gates) will remain at the CLAMP voltage level (VSS or selected pinch-off DAC).
7) With the PA gate low, the PA drain can be provided to the PA. At this time, the user can decide to begin ADC monitoring.
8) Once the PA drain is applied, the PA gate can be turned on through switching the DRVEN pins or bits. The main application begins.

2 AFE20408 Main Application Example



The figure shows an example of an application flow using the AFE20408. The MCU in control of the AFE will send an ADC trigger command and read the ADC outputs. Using this data, the MCU will calculate adjustments to the PA gate "on" voltage to keep a consistent power level. The MCU then writes this update to the DAC buffers.

3 AFE20408 "State Machine"



The figure is a general example of the AFE20408 operational states. When the AFE turns on, all DACs and OUTs are clamped to VSS. The device stays in this state until the AFE20408 is programmed. In the main loop, the device is monitoring all configured alarm conditions. If the AFE detects an alarm, it will set all configured DACs, OUTs, and other pins to the clamp state. The device will stay in the alarm condition until either it is cleared by the MCU or it no longer detects the alarm condition.

Note that if the AFE20408 is cleared by the MCU, it will return to the alarm condition if the next ADC sequence continues to detect the alarm.