

EVM User's Guide: PGA302EVM

PGAxxEVM-037 Pressure Sensor Signal Conditioner Evaluation Module



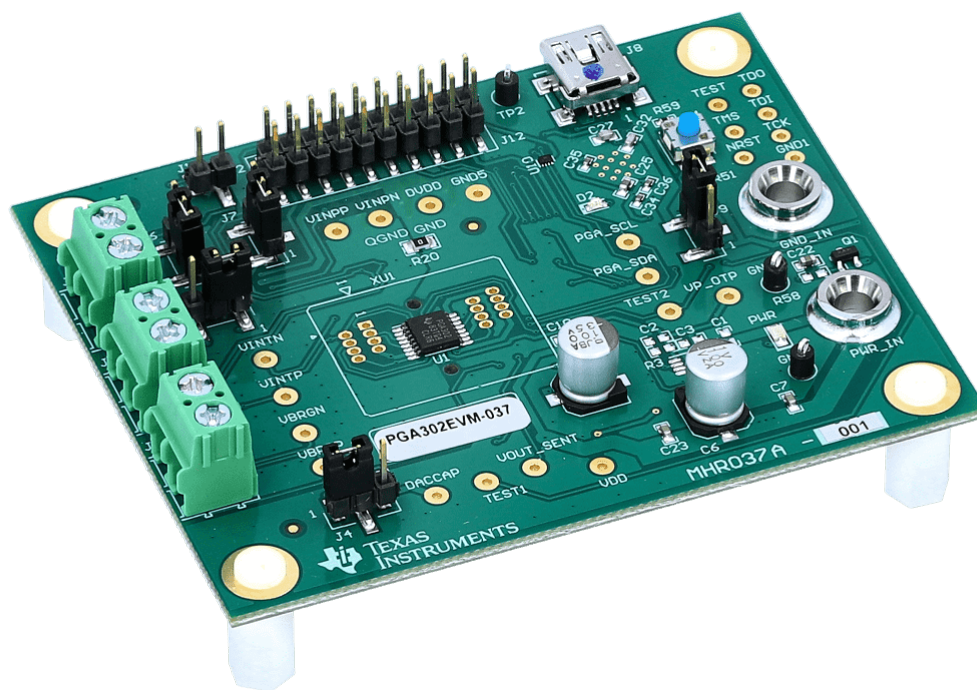
Description

The PGA302EVM-037 is an evaluation module (EVM) that provides a platform to test the PGA302 in the TSSOP package. PGA302EVM-037 is shipped with a PGA302 device soldered down on the board. The user is able to emulate a pressure sensor with an onboard resistive bridge controlled by a digital potentiometer, generate input voltages, and evaluate the voltage mode and digital outputs of the PGA302.

- Onboard resistive bridge emulator to simulate output from typical pressure sensor
- Connections for external temperature and pressure sensors, with onboard voltage excitation for resistive bridges
- Fully-tested EVM with available GUI software and USB interface and firmware

Features

- Access to all communication interfaces offered by PGA302EVM-037 including OWI and I²C



PGA302EVM-037

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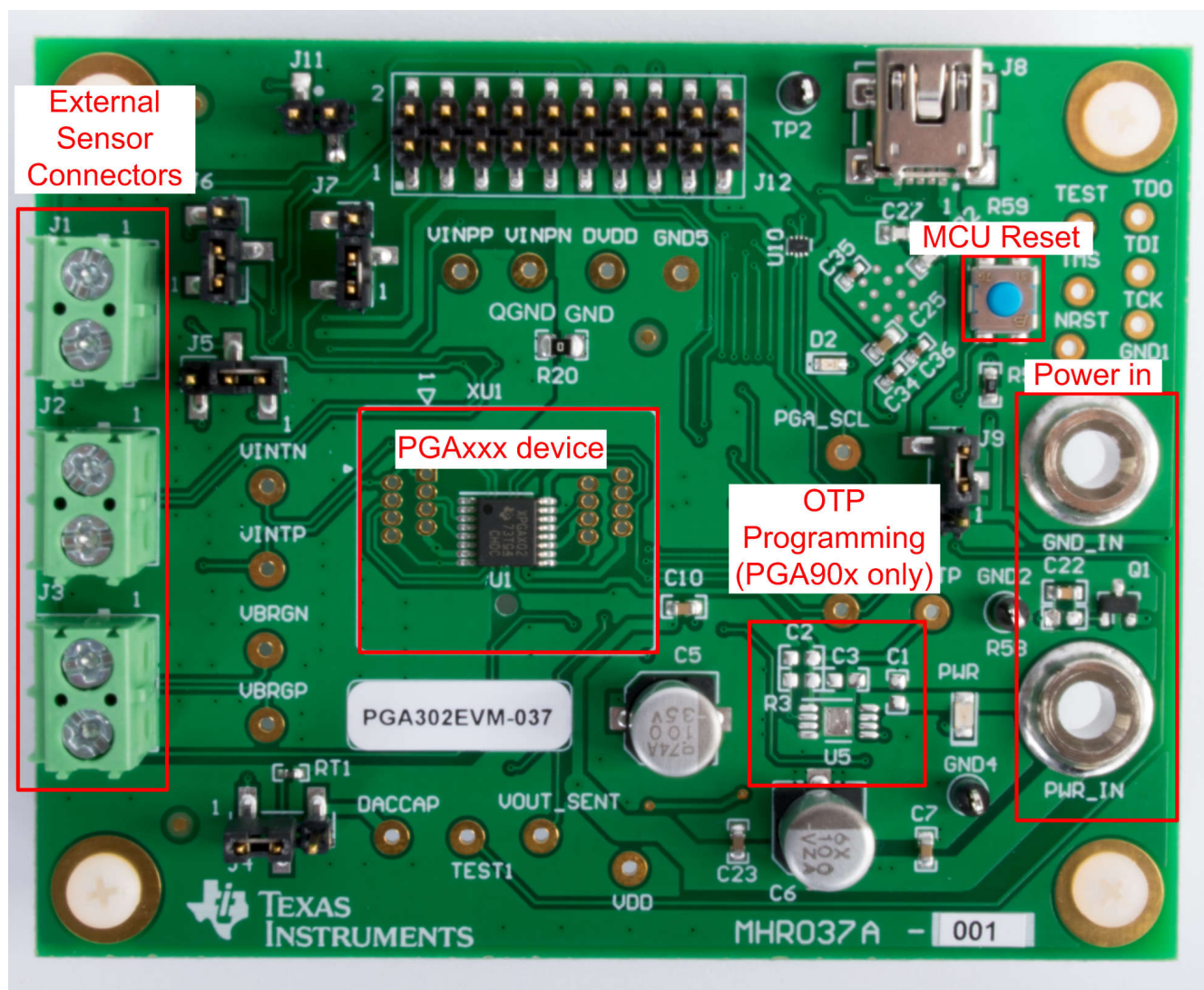
1 Evaluation Module Overview

1.1 Introduction

The PGAxxxEVM-037 provides a platform to test the PGA902, PGA904, and PGA302 in the TSSOP package. The EVM comes shipped as the PGA902EVM-037, the PGA904EVM-037, or the PGA302EVM-037, with the name indicating the associated device included with the EVM. The PGA902EVM-037 and PGA904EVM-037 includes a TSSOP socket, and can be used interchangeably for all three devices. This user's guide describes both the EVM hardware platform, and the graphical user interface (GUI) software used to configure and calibrate the PGAxxx pressure devices.

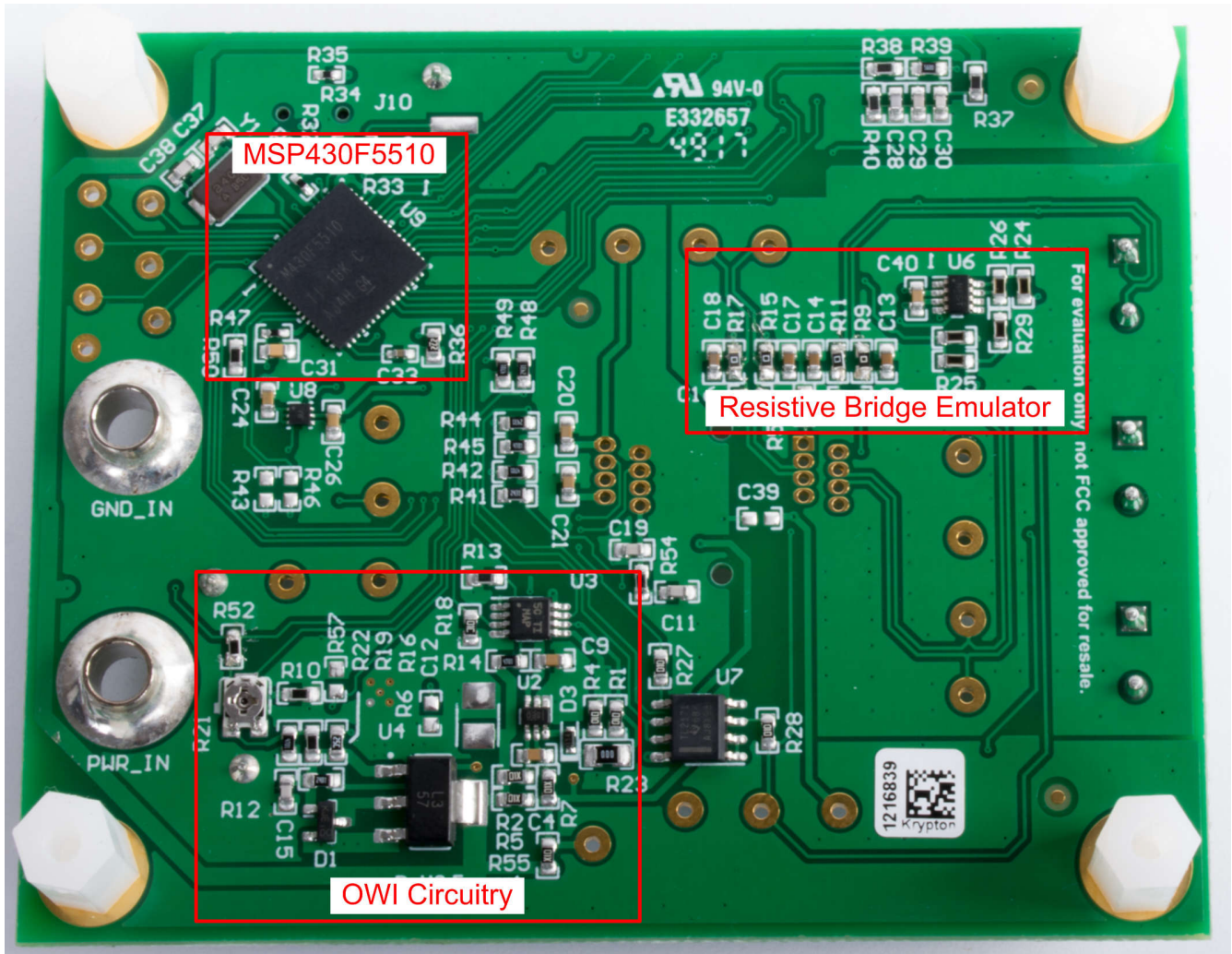
The PGAxxxEVM-037 is a fully-assembled evaluation module (EVM) designed to provide evaluation of the PGA902, PGA904, and PGA302 pressure sensor signal conditioner ICs. The user is able to configure the EVM by using any of the available digital interfaces (I2C, OWI, and SENT) depending on which device and EVM are being used. For ease of use, the most basic evaluation can be completed with only the PGAxxxEVM-037, a voltage supply capable of at least 7V output, and a Microsoft® Windows® PC with the PGAxxxEVM GUI installed.

Temperature and pressure inputs can be simulated by the onboard *Resistive Bridge Emulator* (see [Section 3.15.5](#)), or the user can connect external temperature and pressure sensors to evaluate the performance in conjunction with the PGAxxx device.



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Figure 1-1. PGA302EVM-037 Top Board Sections



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Figure 1-2. PGA302EVM-037 EVM Bottom Board Sections

The PGAXxxxEVM-037 is divided into the following sections:

1. Power
 - a. External power connectors
 - b. Onboard regulators
2. OWI Communication
3. MSP430F5510 Microcontroller
4. External resistive bridge interface
5. Resistive bridge emulator
6. Programming circuitry

Note

Pictured is a PGA302EVM-037 which does not include additional circuitry for firmware programming and SENT communication that is present on the PGA90xEVM-037. The PGA90xEVM-037 also includes a socket instead of a soldered down device.

2 Hardware

2.1 Default Configuration

The EVM requires a 7V to 28V input applied to PWR_IN and GND_IN. The power supply must be current limited to 100mA. The default jumper settings connect the resistive bridge emulator to the VBRG outputs and to the VINP inputs of the PGAx_{xx} device and are described in full in [Table 2-1](#).

Table 2-1. Default Jumper Settings

Jumper	Setting	Function
J4	Pins 1-2 Closed	Connect VINTP to RT1 10kΩ thermistor
J5	Pins 1-2 Closed	Connect top of resistive bridge emulator to VBRGP
J6	Pins 1-2 Closed	Connect resistive bridge emulator output to VINPP
J7	Pins 1-2 Closed	Connect resistive bridge emulator output to VINPN
J9	Pins 2-3 Closed	Power 3.3V LDO from VCC
J11	Open	Disconnect SENT output

Table 2-2. Additional Jumper Settings Description

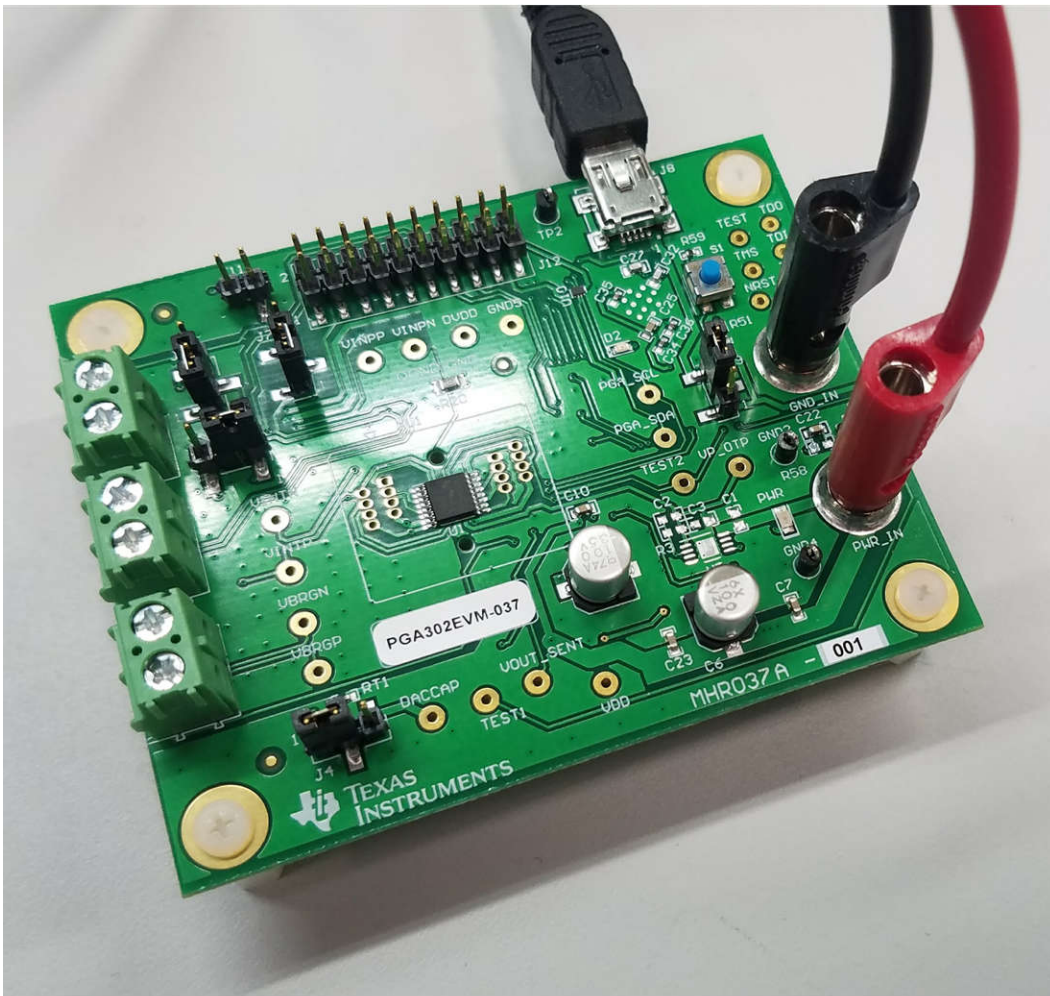
Jumper	Setting	Function
J4	Pins 2-3 closed	Connect DAC_CAP to RT1 10kΩ thermistor
J5	Pins 2-3 closed	Connect top of resistive bridge emulator to TEST1
	Open	Connect VBRGP to J3 pin 1
J6	Pins 2-3 closed	Connect resistive bridge emulator output to VINTP
	Open	Connect VINPP to J2 pin 1
J7	Pins 2-3 Closed	Connect resistive bridge emulator output to VINTN
	Open	Connect VINPN to J2 pin 2
J9	Pins 1-2 Closed	Power 3.3V LDO from USB VBUS
J11	Closed	Connect SENT output

2.2 EVM Setup and Operation

2.2.1 Quick Start Procedure

The PGAx_{xx}EVM-037 is designed to be ready for immediate evaluation out of the box with the onboard resistive bridge emulator as a simulation of a pressure sensor input. The following procedure details the steps necessary to begin evaluation with the PGAx_{xx}EVM-037 and the PGAx_{xx} EVM GUI.

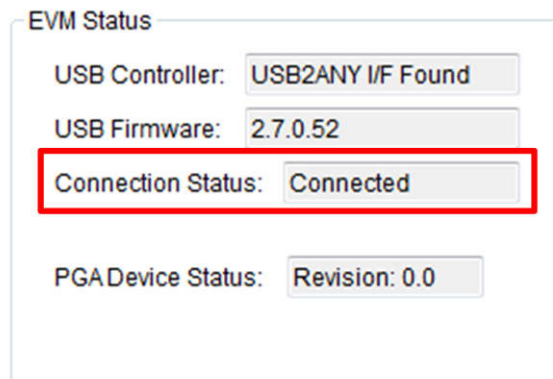
- Collect the following supplies:
 - PGAx_{xx}EVM-037
 - PC running Windows 7 or later
 - Micro-USB to USB cable
 - A single power supply unit, battery, or AC/DC adapter to provide a voltage output from 7V to 28V and a current output of up to 100mA.
- Follow the instructions in the *Installation* section (see [Section 3.1](#)) of the User's Guide to install and run the PGAx_{xx} EVM GUI.
- With the power supply off, connect the positive output of the supply to the PWR_IN connector on the EVM, and the power supply ground to the GND_IN connector. Only turn on the power supply output after connecting to the EVM.
- Plug the micro-USB cable into the USB port on the EVM, and the USB side of the cable into the PC. The EVM setup needs to look similar to the one shown in [Figure 2-1](#).



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Figure 2-1. EVM Quick Start Setup

5. Navigate to the GUI installation directory to run the PGxxx EVM GUI.
6. Verify that communication has been established between the EVM and the GUI by checking the *EVM Status* section in the main panel, or in the status bar on the bottom left of the GUI as shown in [Figure 2-2](#).

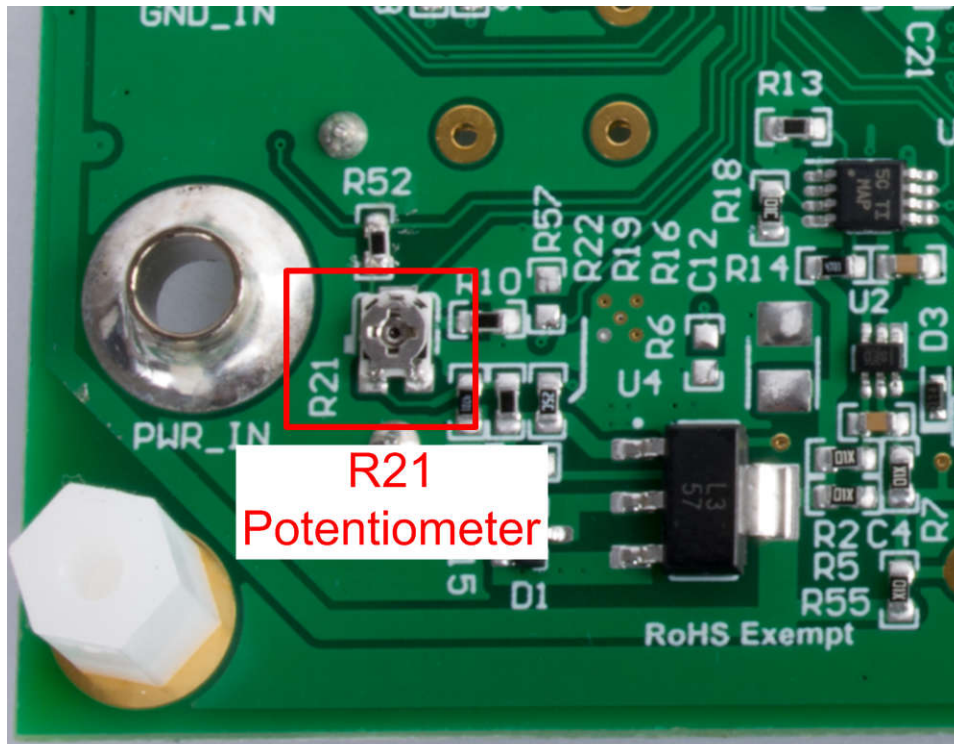


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Figure 2-2. EVM GUI Connection Status

2.2.2 VDD Voltage Setup

The OWI circuitry can be sensitive to component variances and loading. To verify proper voltage levels, a 10k Ω potentiometer (R21) must be adjusted by the user. The potentiometer is located on the bottom of the board (pictured in [Figure 2-3](#)) and must be adjusted while the PGxxxEVM-037 is powered up first by pulling the OWI_5P5 pin high with the *EVM Pin State* controls in the GUI (see [Section 3.3.2](#)), then by monitoring the voltage on the VDD test point or with the *Voltage Monitor* tab (see [Section 3.15.3](#)) and turning the potentiometer until VDD is between 4.5V and 5.5V.



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Figure 2-3. VDD Voltage Adjustment Potentiometer

2.2.3 Pressure Inputs

The PGAx_{xx}EVM-037 includes a resistive bridge emulator designed to simulate a typical 5kΩ pressure sensor topology. The variable leg consists of a digital potentiometer in parallel with a 2.61kΩ resistor, and the parallel components are in series with a 2.55kΩ resistor as shown in Figure 2-4.

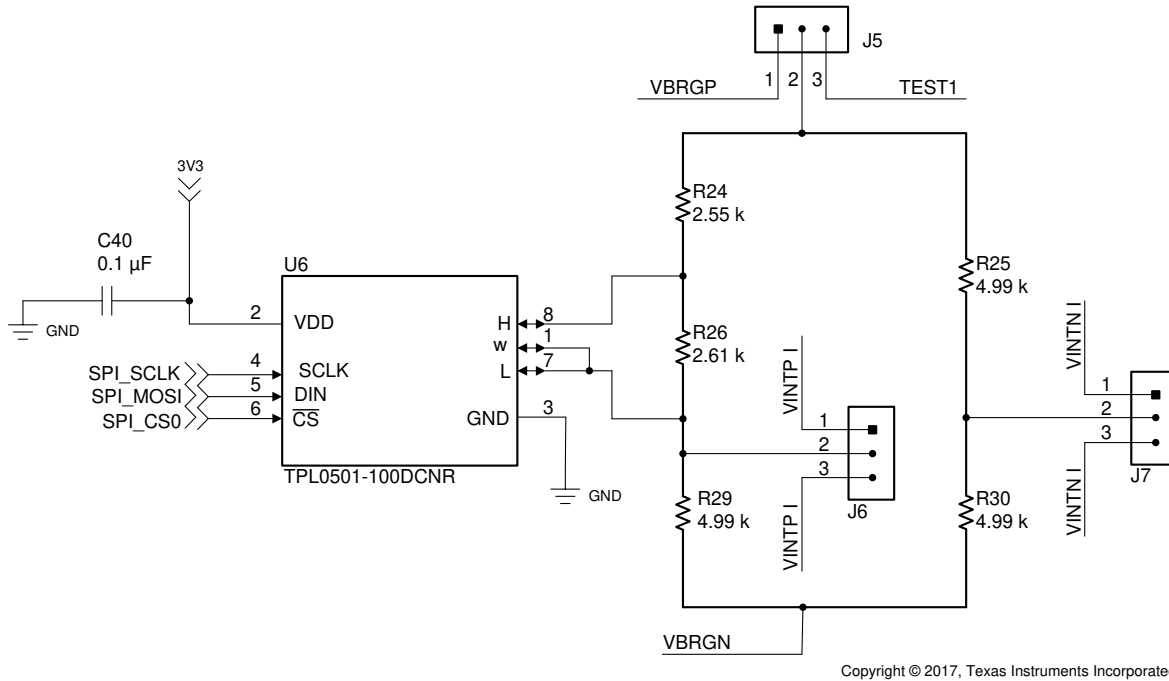


Figure 2-4. Schematic of Resistive Bridge Emulator

The default configuration of the EVM connects the PGAx_{xx} to the resistive bridge emulator with VBRGP and VBRGN supplying voltage, while VINPP and VINPN are connected to measure the differential voltage across the legs of the bridge. To use an external bridge or pressure sensor, remove the jumpers J5, J6, and J7. Next, connect the positive bridge voltage to J3 pin 1 (VBRGP) and the negative terminal of the bridge to J3 pin 2 (VBRGN). The differential voltage outputs of the bridge can be connected to J2, with pin 1 being VINPP and pin 2 being VINPN, as shown in Figure 2-5.

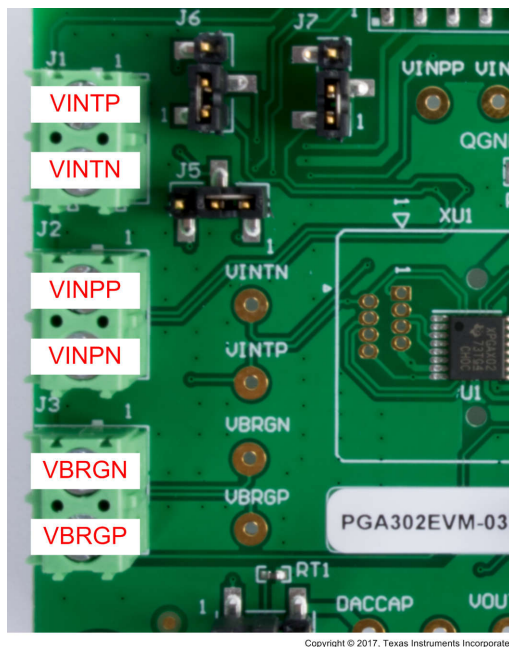


Figure 2-5. External Bridge Connections

2.2.4 Temperature Inputs

The external temperature sensor inputs can be connected to either the resistive bridge emulator, or to an external temperature sensor. By default, the EVM is configured with the external temperature sensor inputs, VINTP and VINTN, disconnected from the resistive bridge emulator, but accessible via J1 with pin 1 being VINTP and pin 2 being VINTN. To use the resistive bridge emulator to test the external temperature sensor measurement, place the jumpers as described in [Table 2-3](#).

Table 2-3. Jumper Settings to Connect Resistive Bridge to Temperature Inputs

Jumper	Setting	Function
J5	Open	Disconnect VBRGP from resistive bridge emulator
J6	Pins 2-3 closed	Connect resistive bridge emulator output to VINTP
J7	Pins 2-3 closed	Connect resistive bridge emulator output to VINTN

Note

This configuration connects an adjustable 10kΩ resistance between VINTP and VINTN as a test mode and is not intended for use as a functioning external temperature sensor.

2.2.5 Voltage Output

The PGAx_{xx} devices can output measured pressure and temperature values in analog voltage form via the 14-bit output DAC. On the PGAx_{xx}EVM-037, this VOUT voltage can be measured externally at the VOUT_SENT test point or through the GUI, which makes use of the internal ADC of the MSP430 to measure the voltage and display on the *Voltage Monitor* tab of the GUI.

3 Software

3.1 Installation

Download and install the GUI from www.ti.com. Navigate to the default installation path of the executable file by clicking on the *Windows Start* button. Click on *All Programs* and then navigate to the Texas Instruments folder to find the PGAxixGUI application shortcut.

3.2 GUI Navigation

The GUI is comprised of three main sections: the menu tree, the main control panel, and the tool panel as [Figure 3-1](#) shows. All PGA device settings are adjusted through the main control panel, which can be changed to display different groups of settings via the menu tree. The following sections describe the settings available in each item in the menu tree.

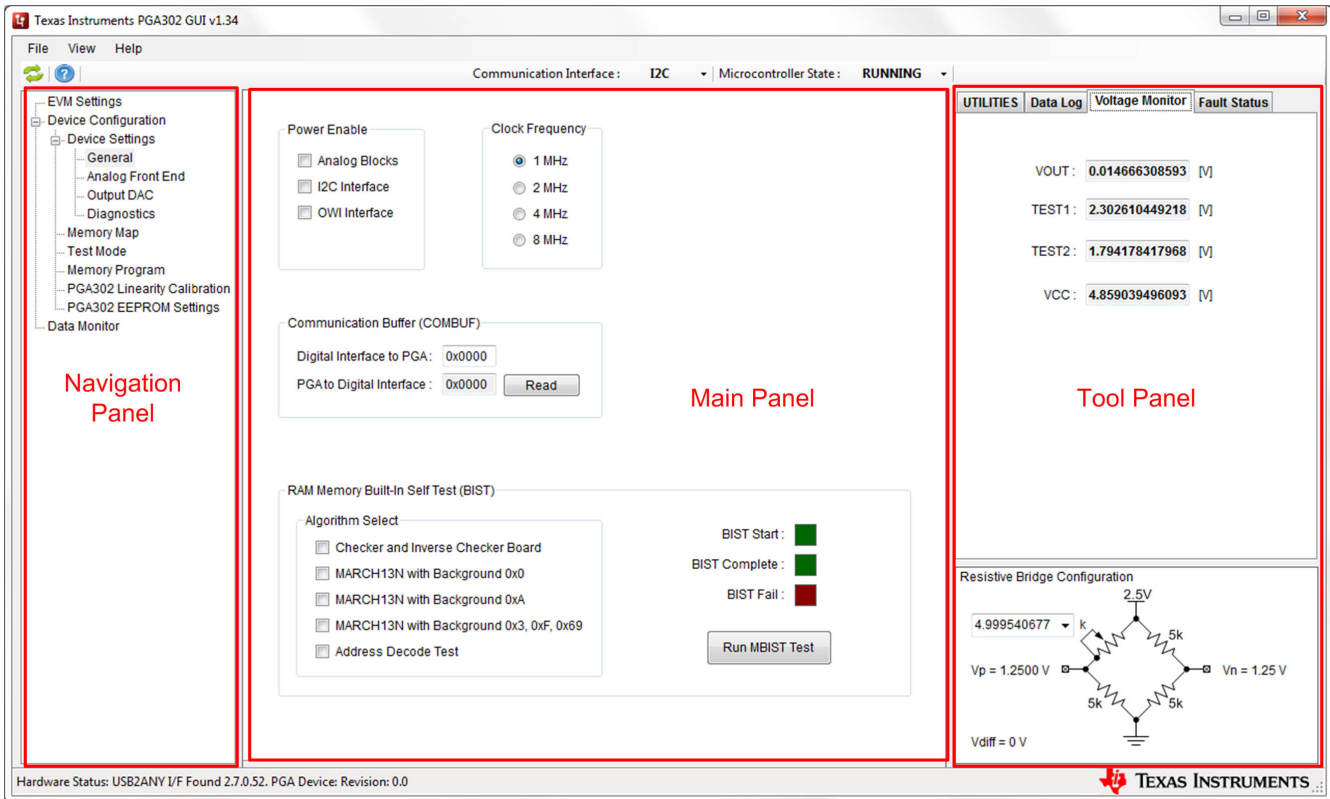


Figure 3-1. GUI Sections

3.3 EVM Settings Page

EVM Status

USB Controller:

USB Firmware:

Connection Status:

PGA Device Status:

EVM Pin State

VP_OTP_EN:

OWI_TX:

OWI_ACT:

OWI_5P5:

OWI Settings

OWI Baud Rate: bps

Stop Bits : bit

I2C Settings

I2C Frequency: kHz

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Figure 3-2. EVM Settings Page

3.3.1 EVM Status

The GUI can automatically detect the presence of the PGAxxxEVM. In the event of a successful or failed connection between the PC, MSP430F5510, and PGAxxxEVM-037, the EVM status fields are updated according to [Table 3-1](#).

Table 3-1. EVM Status Possibilities

EVM Status	Success	Failure
USB Controller	USB2ANY I/F Found	Not Detected
USB Firmware	2.7.0.52	N/A
Connection Status	Connected	N/A
PGA Device Status	Revision 0.0	Not available

Table 3-2. EVM Status Field Descriptions

EVM Status	Definition
USB Controller	The MSP430F5510 is programmed with TI's USB2ANY host interface (I/F) controller firmware. The GUI calls API functions for the USB2ANY to execute. The USB2ANY I/F is the only compatible USB controller for the PGAxxxEVM GUI.
USB Firmware	The USB2ANY firmware can be updated for improvements or bug fixes. Version 2.7.0.52 is the only firmware version tested and known to be working for the PGAxxxEVM GUI.
Connection Status	Typically, only one USB2ANY is connected to a PC, though the USB2ANY APIs are able to distinguish multiple USB2ANY devices on the same USB bus. For a single USB2ANY I/F, the status shows <i>Connected</i> , but for multiple, the status shows <i>Multiple Found</i> . TI recommends that a single USB2ANY I/F be connected to the PC during the evaluation of the PGAxxxEVM GUI.
PGA Device Status	When an I2C read command is successfully executed on the PGA device, the status is updated to <i>Ready</i> . If the status reads back <i>Not available</i> , then use the following checklist to troubleshoot: <ul style="list-style-type: none"> • Is the device seated properly in the socket (PGA902/904 only)? • Is the PGAxxx-037 EVM powered with a voltage of 7–28 V? • Is the power supply unit able to source at least 20mA? • If the device was powered after the GUI was first initialized, then click the application reset button to reconnect.

3.3.2 EVM Pin State

The *EVM Pin State* is automatically updated when the GUI is started and connected to a PGAxxx device. Any of the available pins can be changed by the user to either HIGH, LOW, or HIZ states.

3.3.3 OWI Settings

The following OWI settings are available:

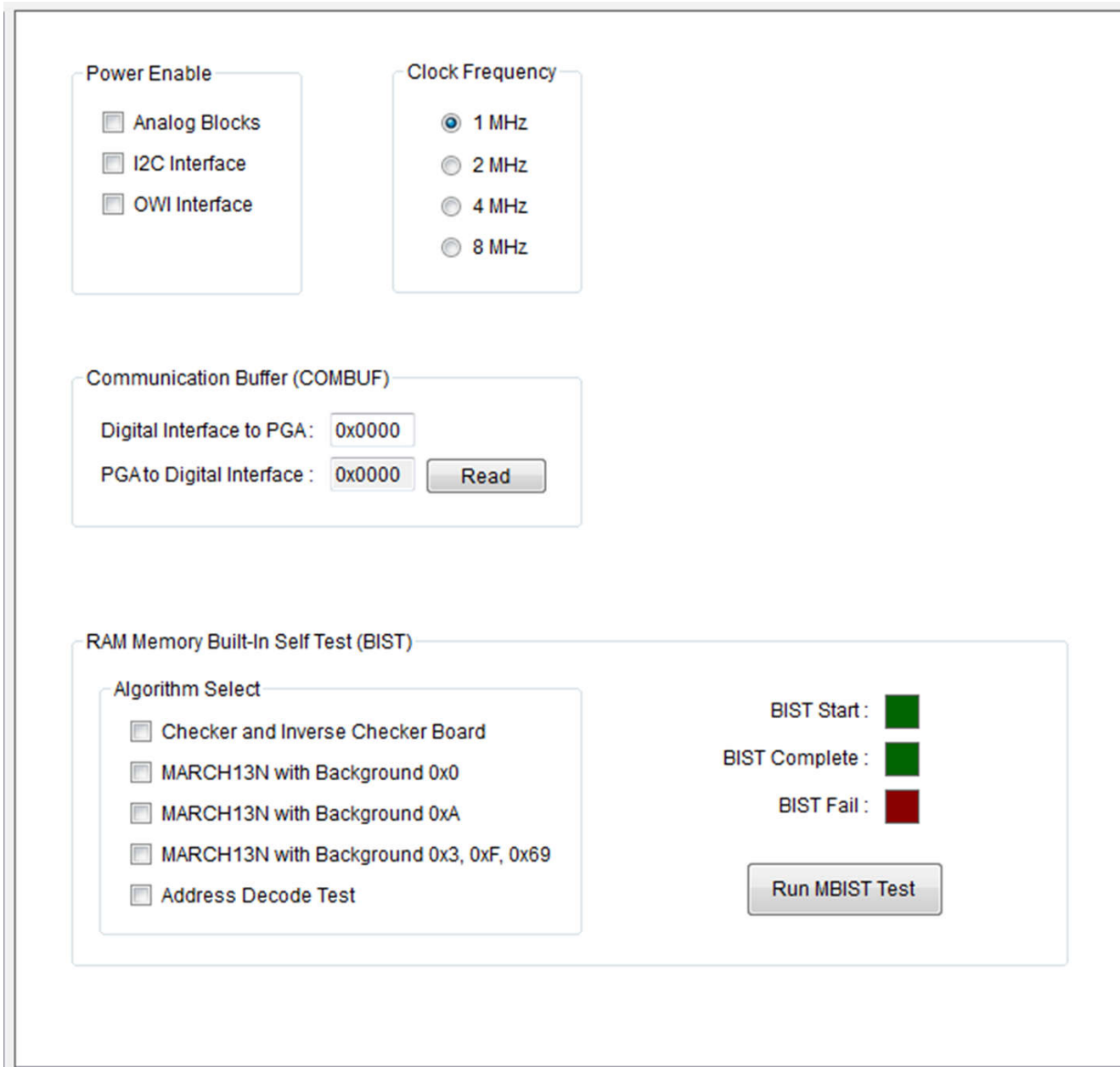
- **OWI Baud Rate:** Sets the baud rate for the OWI communication. The available options are 2400bps or 4800bps
- **Stop Bits:** Sets the number of stop bits for OWI communication. The available options are 1 or 2 stop bits.
- **Send VDD Activation Pulse:** Briefly raises the VDD voltage to 7V to initiate OWI communication. This is used to test if the OWI circuitry is functioning properly.
- **Send Register Activation Command:** For the PGA90x devices without programmed firmware, a register activation command is sent to activate the OWI transceiver circuitry within the device.

3.3.4 I2C Settings

The I2C frequency selection allows the user to select 100kHz, 400kHz, and 800kHz for I2C communication.

3.4 General Settings Page

[Figure 3-3](#) shows the *General Settings Page* window.



The screenshot displays the 'General Settings Page' with the following sections:

- Power Enable:** Three checkboxes for 'Analog Blocks', 'I2C Interface', and 'OWI Interface', all currently unchecked.
- Clock Frequency:** Four radio buttons for '1 MHz', '2 MHz', '4 MHz', and '8 MHz'. The '1 MHz' option is selected.
- Communication Buffer (COMBUF):** Two input fields: 'Digital Interface to PGA:' and 'PGA to Digital Interface:', both containing '0x0000'. A 'Read' button is positioned to the right of the second field.
- RAM Memory Built-In Self Test (BIST):**
 - Algorithm Select:** Five checkboxes for 'Checker and Inverse Checker Board', 'MARCH13N with Background 0x0', 'MARCH13N with Background 0xA', 'MARCH13N with Background 0x3, 0xF, 0x69', and 'Address Decode Test', all currently unchecked.
 - Status Indicators:** Three colored squares: a green square for 'BIST Start:', another green square for 'BIST Complete:', and a red square for 'BIST Fail:'.
 - Run MBIST Test:** A button located below the status indicators.

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Figure 3-3. General Settings Page**3.4.1 Power Enable**

Power can be disabled to specific blocks within the PGAx_{xx} device to decrease total power consumption. The analog blocks, I2C communication, OWI communication, and SENT OUTPUT (PGA904 only) can all be individually enabled or disabled to save power.

3.4.2 Clock Frequency

This section allows the user to control the clock frequency of the internal microcontroller.

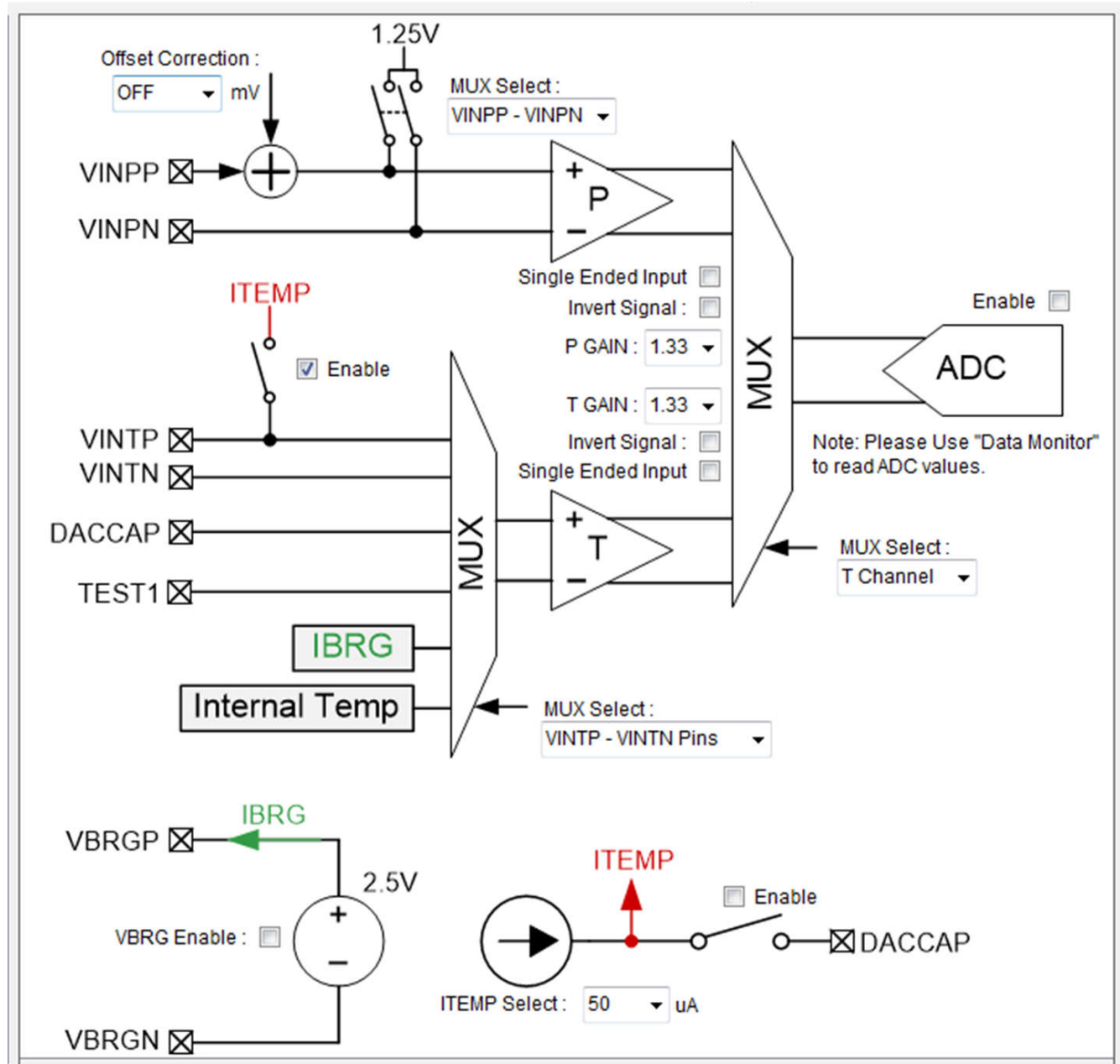
3.4.3 RAM Memory Built-In Self Test

A RAM Memory Built-In self test is available to make sure the RAM of the PGAx_{xx} device is functioning properly. The user can select one or more algorithms to test the memory. Once the test is begun by clicking the *START*

button, the GUI initiates each selected test in turn, and reports once all tests are complete and if any of the tests were failed.

3.5 Analog Front End Page

The analog front end panel allows the user to configure the AFE portion of the PGAxx device in an easy-to-use block diagram format (shown in Figure 3-4) as an initial test and debug measure. These same settings are available in the *PGA302 EEPROM Settings* page (PGA302 EVM GUI only), however the settings made in the *Analog Front End* page does not carry over to the EEPROM settings page, and must be repopulated to program the EEPROM for future use.



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Figure 3-4. Analog Front End Page

3.5.1 Offset Correction

The offset correction setting allows the user to adjust the voltage offset of the pressure inputs to account for minor offset errors and to make full use of the input range of the integrated ADC of the PGxxx. Offset correction values from -54.75 mV to $+54.75$ mV are available, or the offset correction can be turned off entirely.

3.5.2 Input Signal MUX Select and Additional Settings

The MUX select setting allows the user to choose the input type of the signal connected to the VINPP and VINPN pins of the device. For a differential signal, select VINPP – VINPN, and for single-ended signals the user can choose either VINPP – 1.25V, or 1.25V – VINPN depending on which of the input pins the signal is connected to. The *Single Ended Input* box must also be selected if using a single-ended input signal. Additionally, the input signal can be inverted if desired by checking the *Invert Signal* box. The *Single Ended Input* and *Invert Signal* check boxes are available for both the P Gain and T Gain input blocks, and can be configured separately.

3.5.3 P Channel and T Channel

Both the P Channel and T Channel blocks have adjustable gains with a range of 1.33V/V up to 200V/V to properly amplify any input signal to take advantage of the full input range of the ADC.

3.5.4 P/T Channel Select

The *P/T Channel MUX Select* allows the user to determine which input signals are directed to the ADC of the PGxxx device. In fixed-channel mode, either the P Channel or T Channel inputs can be directed to the ADC for sampling. The *Auto Scan* mode allows the ADC to sample from both the P Channel and the T Channel at user-defined intervals.

3.5.5 T Channel MUX Select

The T Channel MUX Select allows the user to determine which signals are passed through the T Channel to the ADC for sampling. The VINTP and VINTN pin option can be selected for use with an external temperature sensor, or other sensor. To use the internal temperature sensor of the PGxxx device, select the *Internal Temp Sense* option. The *Bridge Current* option allows the user to read the current through the internal VBRG voltage supply of the PGxxx device. Additionally, the TEST1 pin can be MUXed through to monitor a variety of internal signals for debugging purposes. The output of the TEST1 pin can be set on the *Test Mode* page (see [Section 3.10](#)). Finally, the DACCAP pin can be used as an additional input if desired, and can be sent through the MUX to the ADC for sampling.

3.5.6 Block Enable Check Boxes

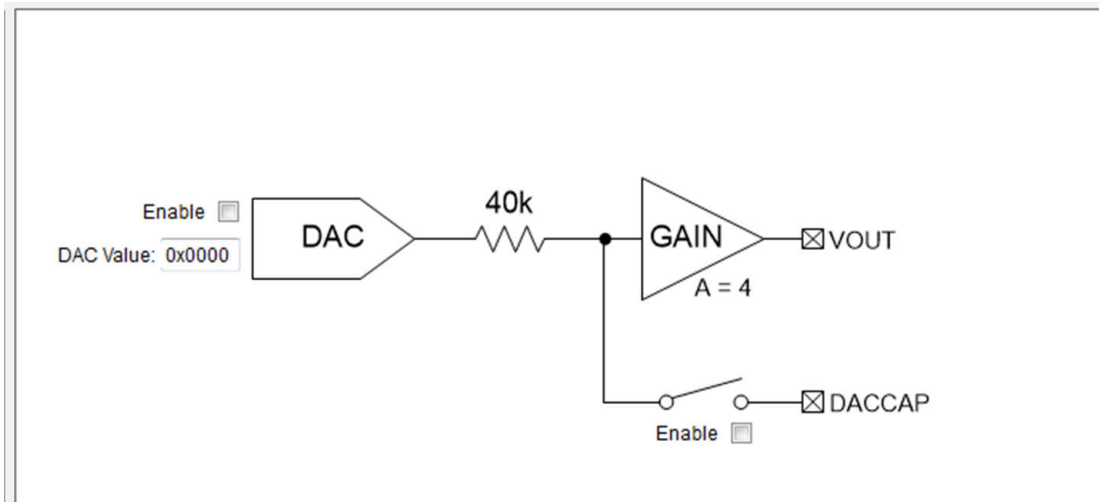
There are several block enable check boxes on the analog front end page. The ITEMP enable box turns on and connect the internal temperature sensor current source for use with external temperature sensors that need current excitation. The VBRG enable box activates the internal bridge voltage supply to provide voltage excitation for resistive bridge pressure sensors. The ADC is enabled with a check box, and finally the DACCAP can be connected with an enable check box to provide a low-pass filter to the DAC output buffer.

3.5.7 ITEMP Select

ITEMP select gives the user the option to select the current output of the ITEMP internal current source. The current source can supply 50 to 1000 μ A, or can be disabled with this control.

3.6 Output DAC Page

[Figure 3-5](#) illustrates the output DAC page.



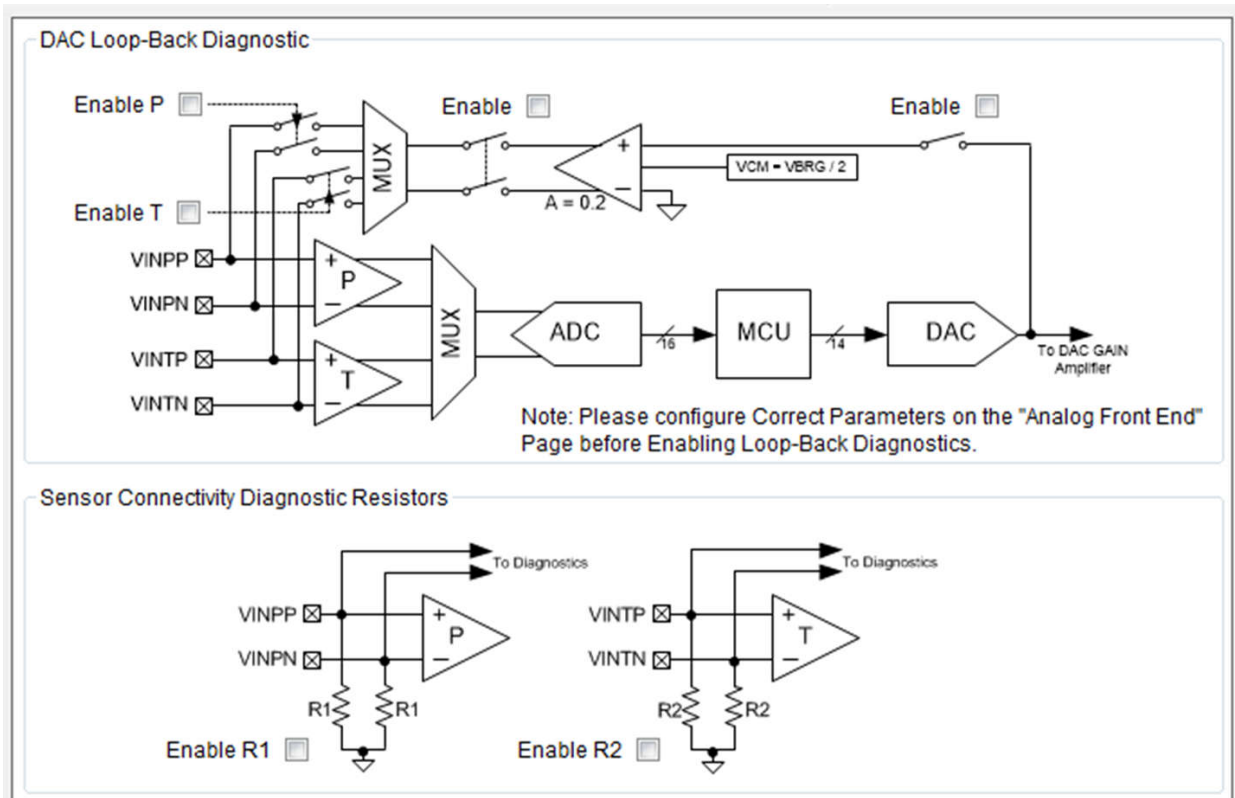
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Figure 3-5. Output DAC Page

The *Output DAC* page allows the user to quickly test the functionality of the output DAC by inputting specific DAC Values and monitoring the result at the VOUT pin. The output DAC and DACCAP connections can also be enabled or disabled from this page. To easily read the voltage on VOUT, the user can use the *Voltage Monitor* tab on the tool panel to the right.

3.7 Diagnostics Page

Figure 3-6 shows the diagnostics page.



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Figure 3-6. Diagnostics Page

3.7.1 DAC Loopback Diagnostics

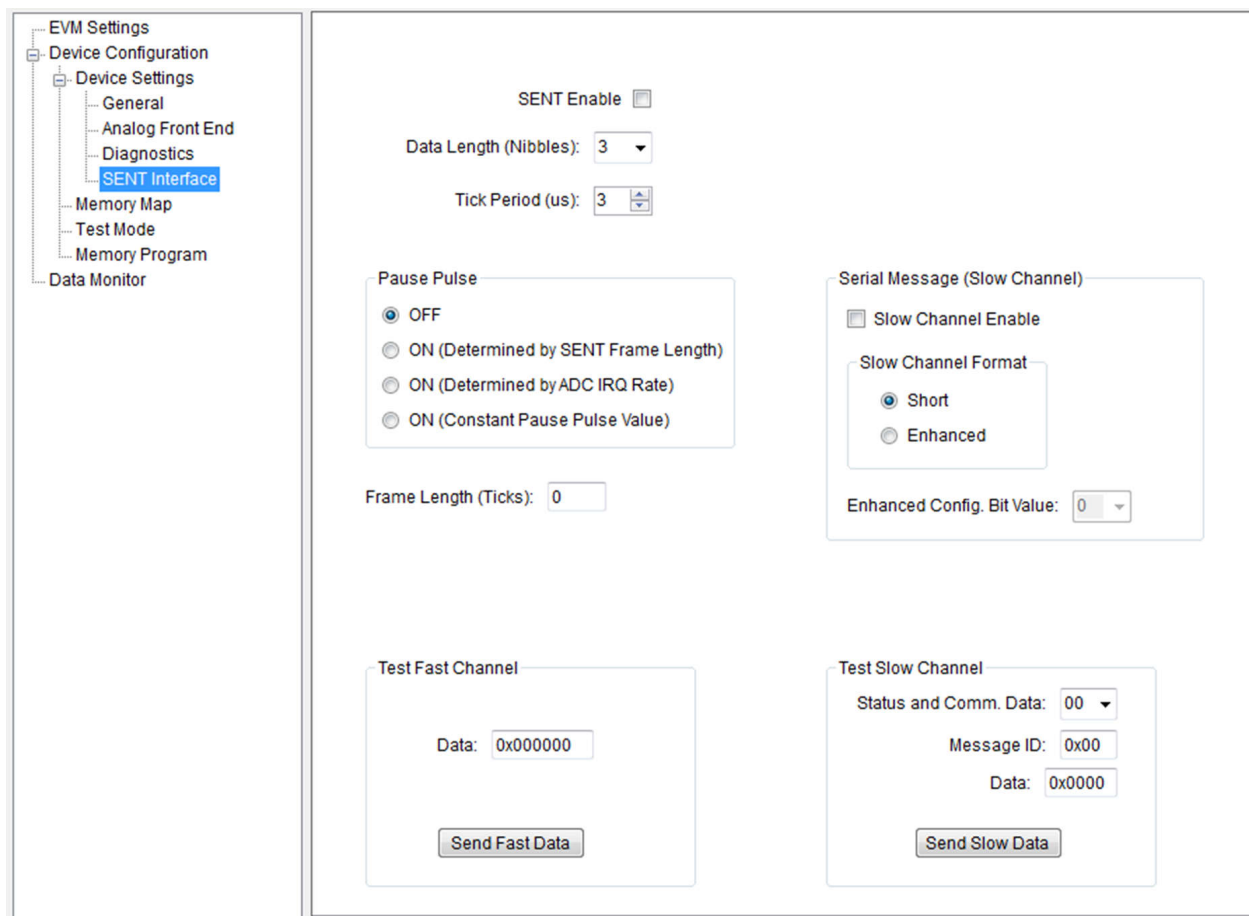
The *DAC Loopback Diagnostics* section allows the user to verify proper signal chain operation by reading the DAC output through the ADC. With the feedback loop enabled, the user can set a DAC value, and then read the resulting ADC value on the *Data Monitor* page (see [Section 3.14](#)) to check for agreement.

3.7.2 Sensor Connectivity Diagnostic Resistors Section

The *Sensor Connectivity Diagnostic Resistors* section allows the user to enable the sensor diagnostic resistors to monitor short and open conditions on the sensor input pins. The output of these diagnostics is available in the *Fault Status* tab of the tool panel to the right under the AFE Diagnostics Section. Short and open conditions can be determined using the VINTP, VINTN, VINPP, and VINPN undervoltage and overvoltage fault status bits in combination with the internal pulldown resistors.

3.8 SENT Interface Page (PGA 904 Only)

The *SENT Interface* page (see [Figure 3-7](#)) allows the user to control SENT settings, and to test communication on both the fast and slow communication channels.



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Figure 3-7. SENT Interface Page

Data length controls the number of fast data *Nibbles* (4 bits) that is sent within each transmission, and the *Tick* period determines the overall speed of the data output.

The pause pulse at the end of each data transmission can be either disabled or turned on with three options for how the length of the pause pulse is determined.

The serial message, or slow channel communication can be enabled and configured. The slow channel data is contained in small portions as part of the STATUS frame at the beginning of each transmission, when enabled.

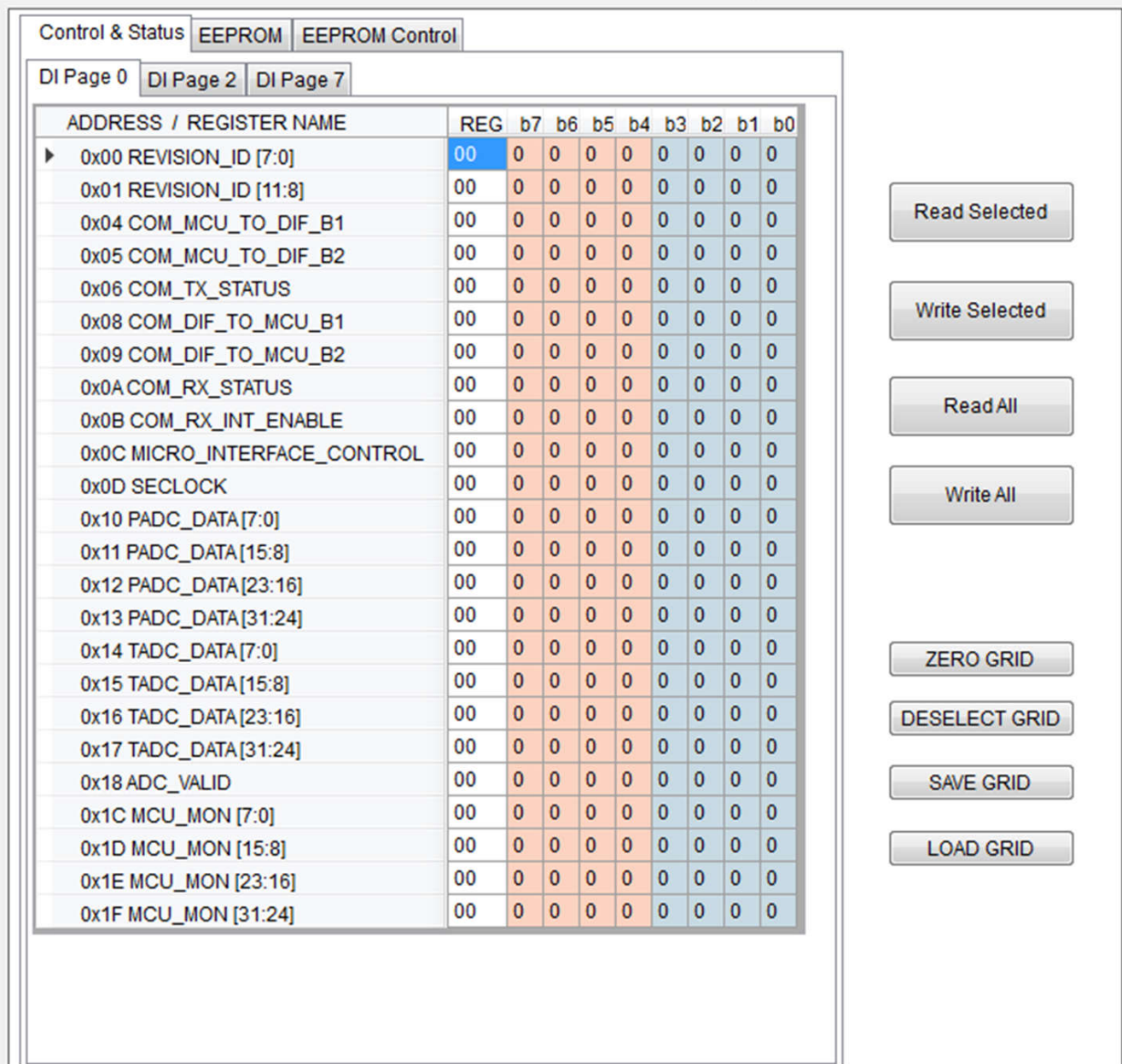
Short mode sends only 8 bits, while enhanced mode allows the user to send 12 or 16 bits depending on the *Enhanced Config Bit* value (0b0 = 12 bits and 0b1 = 16 bits).

Both the fast- and slow-channel communication can be tested from the SENT interface page. Note that when a test signal is begun, the test continuously output the test data until the SENT interface is disabled.

3.9 Memory Map Page

The *Memory Map*, shown in [Figure 3-8](#), allows low-level access to all available registers in the PGxxx device. Any changes made to the map on the left are not finalized until the user clicks either the *Write Selected* or *Write All* buttons to the right of the grid.

The user can save a grid or load a previously saved grid. Note that only the active tab is saved to a file when saving a grid. The file created when saving the EEPROM tab grid is interchangeable with the file created when saving the EEPROM settings on the *Memory Program* page (see [Section 3.11](#)).



The screenshot shows the 'EEPROM' tab selected in the 'Control & Status' section. Below it, 'DI Page 0' is selected. The main area contains a table with columns for 'ADDRESS / REGISTER NAME', 'REG', and bits 'b7' through 'b0'. The first row is selected, and its bits are highlighted in blue. To the right of the table are buttons for 'Read Selected', 'Write Selected', 'Read All', 'Write All', 'ZERO GRID', 'DESELECT GRID', 'SAVE GRID', and 'LOAD GRID'.

ADDRESS / REGISTER NAME	REG	b7	b6	b5	b4	b3	b2	b1	b0
▶ 0x00 REVISION_ID [7:0]	00	0	0	0	0	0	0	0	0
0x01 REVISION_ID [11:8]	00	0	0	0	0	0	0	0	0
0x04 COM_MCU_TO_DIF_B1	00	0	0	0	0	0	0	0	0
0x05 COM_MCU_TO_DIF_B2	00	0	0	0	0	0	0	0	0
0x06 COM_TX_STATUS	00	0	0	0	0	0	0	0	0
0x08 COM_DIF_TO_MCU_B1	00	0	0	0	0	0	0	0	0
0x09 COM_DIF_TO_MCU_B2	00	0	0	0	0	0	0	0	0
0x0A COM_RX_STATUS	00	0	0	0	0	0	0	0	0
0x0B COM_RX_INT_ENABLE	00	0	0	0	0	0	0	0	0
0x0C MICRO_INTERFACE_CONTROL	00	0	0	0	0	0	0	0	0
0x0D SECLOCK	00	0	0	0	0	0	0	0	0
0x10 PADC_DATA [7:0]	00	0	0	0	0	0	0	0	0
0x11 PADC_DATA [15:8]	00	0	0	0	0	0	0	0	0
0x12 PADC_DATA [23:16]	00	0	0	0	0	0	0	0	0
0x13 PADC_DATA [31:24]	00	0	0	0	0	0	0	0	0
0x14 TADC_DATA [7:0]	00	0	0	0	0	0	0	0	0
0x15 TADC_DATA [15:8]	00	0	0	0	0	0	0	0	0
0x16 TADC_DATA [23:16]	00	0	0	0	0	0	0	0	0
0x17 TADC_DATA [31:24]	00	0	0	0	0	0	0	0	0
0x18 ADC_VALID	00	0	0	0	0	0	0	0	0
0x1C MCU_MON [7:0]	00	0	0	0	0	0	0	0	0
0x1D MCU_MON [15:8]	00	0	0	0	0	0	0	0	0
0x1E MCU_MON [23:16]	00	0	0	0	0	0	0	0	0
0x1F MCU_MON [31:24]	00	0	0	0	0	0	0	0	0

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Figure 3-8. Memory Map Page

3.10 Test Mode Page

Analog Test Modes

Analog Output Test MUX Select: TEST1 Enable

Analog Input Test MUX Select: VINTP VINTN Enable

Note: The Analog Output Test MUX pin is TEST1, while the Analog Input Test MUX pins are VINTP and VINTN

Digital Test Modes

Digital Test Mode Enable

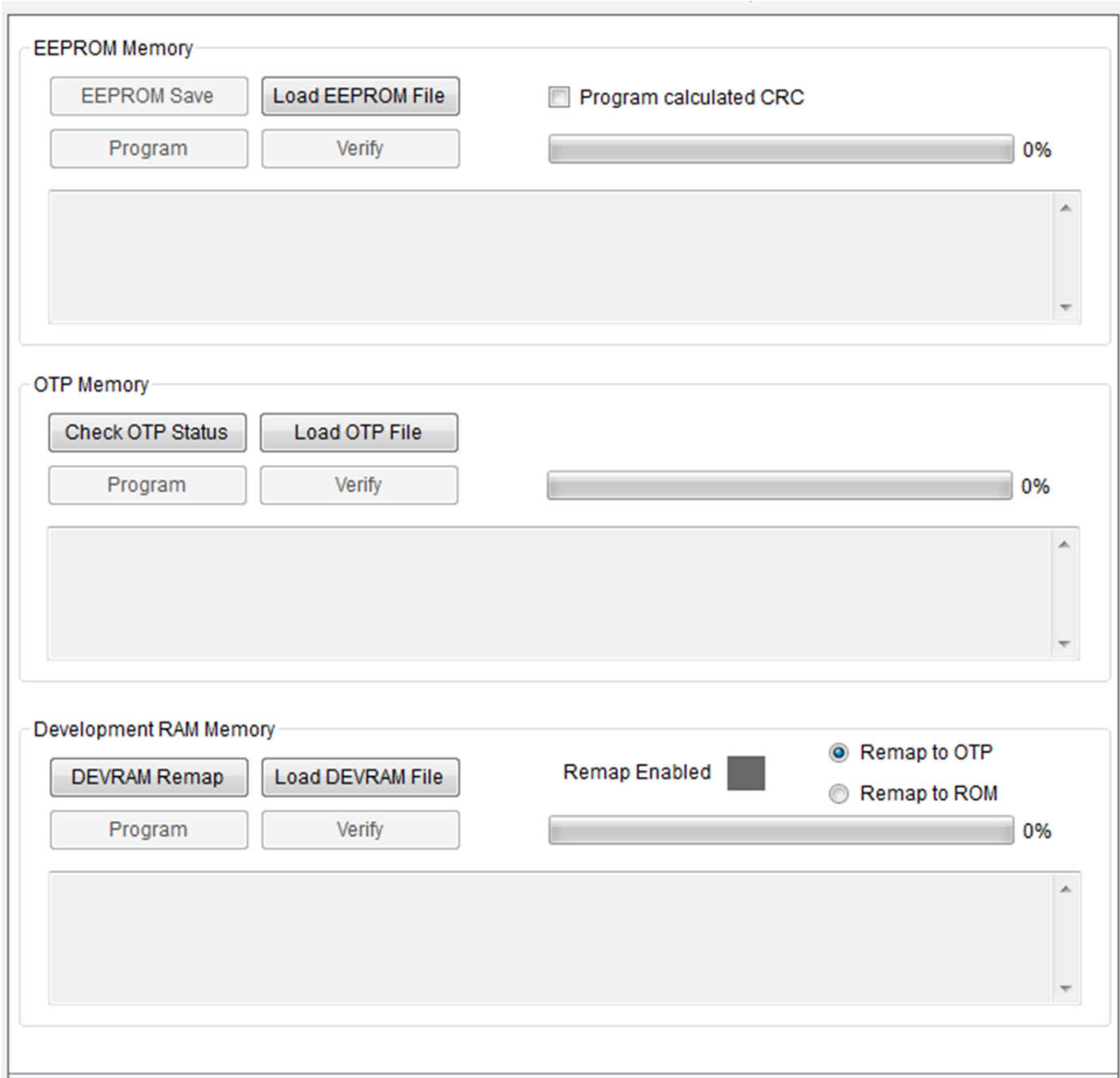
TEST1 Digital Output Test MUX Select:

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Figure 3-9. Test Mode Page

The *Test Mode* page (see [Figure 3-9](#)) provides access to the analog and digital test MUX settings of the PGAxXX device. The analog and digital test MUX outputs are output through the TEST1 pin, while the analog test MUX inputs are connected to the VINTP and VINTN pins. A variety of internal signals are accessible through these options for debugging purposes, but a full description of this functionality is outside the scope of this document.

3.11 Memory Program Page



The screenshot displays the Memory Program Page with three main sections:

- EEPROM Memory:** Includes buttons for 'EEPROM Save', 'Load EEPROM File', 'Program', and 'Verify'. A checkbox for 'Program calculated CRC' is present and unchecked. A progress bar shows 0% completion.
- OTP Memory:** Includes buttons for 'Check OTP Status', 'Load OTP File', 'Program', and 'Verify'. A progress bar shows 0% completion.
- Development RAM Memory:** Includes buttons for 'DEV RAM Remap', 'Load DEV RAM File', 'Program', and 'Verify'. A 'Remap Enabled' checkbox is checked. Two radio buttons are visible: 'Remap to OTP' (selected) and 'Remap to ROM'. A progress bar shows 0% completion.

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Figure 3-10. Memory Program Page

For the EEPROM Memory, the user can load or save a memory map file as well as program the calculated CRC. This is a good practice to verify the EEPROM after each programming procedure. Note that the file loaded and saved on this page is interchangeable with the file that can be loaded or saved on the *Memory Map* page when viewing the EEPROM tab.

Note

The OTP Memory and Development RAM Memory sections are only available in the PGA902 and PGA904 EVM GUIs.

The Check OTP Status button allows the user to see if the OTP memory has already been burned on the PGAxXX device. An OTP file can be loaded and then programmed and verified in the OTP Memory Section.

When using the DEVRAM, the DEVRAM memory space must be remapped to the OTP memory so that the microcontroller operates from the correct memory. Select the *Remap to OTP* radio button, and click the *DEVRAM Remap* button before continuing. Once completed, a DEVRAM file can be loaded, programmed, and verified.

3.12 PGA302 Linearity Calibration Page (PGA302 Only)

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Figure 3-11. PGA302 Linearity Calibration Page

One of the key features of the PGA302 pressure sensor signal conditioner is the preprogrammed firmware which includes linearization and temperature compensation algorithms to provide reliable results from a variety of pressure sensors in real world systems. To maximize the effectiveness of these algorithms, calibration of the PGA302 device for each sensor is critical. The PGA302 Linearity Calibration panel provides a simple interface

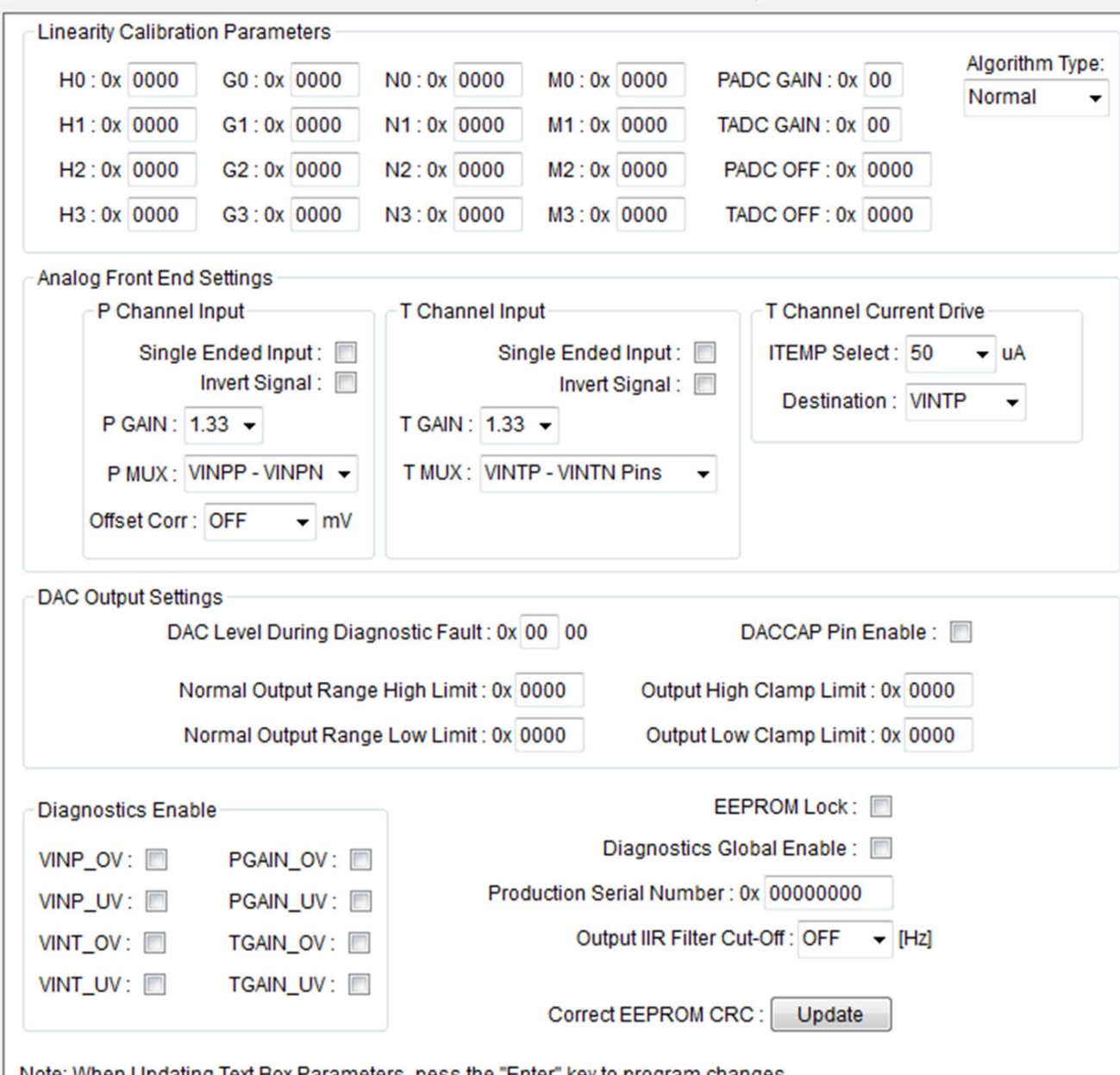
to calibrate the input and output stages of the PGA302 device with minimal external equipment. The following example procedure details the user through the calibration process by using the onboard resistive bridge to simulate a pressure sensor.

3.12.1 PGA302 Linearity Calibration Procedure

1. Follow the *PGAxxxEVM-037 Quick Start Procedure* ([Section 2.2.1](#)) to power up the EVM and establish communication with the PGAxxx device. Make sure that the jumpers are set to the default position as shown in [Table 2-1](#).
2. Place the microcontroller in *Reset* by clicking the *Microcontroller State* field.
3. Select the *Calibration Model* you wish to use. For this example, select “3 Pressure, 1 Temperature”
4. Click *START* at the bottom of the page, and follow the prompts from the message center below the *START* button.
5. Update the desired output voltage for Pressure 1 and click *NEXT* when finished. Repeat this process for Pressure 2 through Pressure 4. In this case (3 Pressure, 1 Temperature), Pressure 3 is not accessible for updating.
6. Update the desired DAC Code for Pressure 1 and click *NEXT* when finished. Repeat this process for Pressures 2 and 4.
7. Click *NEXT* again. Check the value in the Vout 1 row under the column Temp 2. This value is automatically populated with the Vout voltage output associated with the DAC code entered in the previous step. The voltage is measured by the ADC in the MSP430 microcontroller on the PGAxxxEVM-037. If you wish to verify the voltage with an external voltage meter, measure the voltage on the VOUT_SENT test point on the EVM. The voltage value can be left as is, or an updated value can be manually entered by the user. Once the value is set, click *NEXT*. Repeat this process for Vout 2, and Vout 4.
8. Before continuing, set the number of *Average Samples* to use in the *Advanced Settings* section of the page. This value can range from 1 to 128 and averages the number of samples selected to generate the ADC value populated in the calibration algorithm. Increasing the number of samples averaged increases the amount of time the ADC value to populate. For this example, the default value of 8 is selected.
9. Set the resistive bridge leg resistance to the desired value using the *Resistive Bridge Configuration* panel. For this example, use 5.0850k as the Pressure 1 value. Click *NEXT* when finished. The cell is populated automatically with the value read by the ADC. If the value does not populate properly, or if the value does not seem correct, then the *Data Monitor* page (see [Section 3.14](#)) can be used to help debug by reading the ADC values in real time. The value in the cell can be manually entered at any time by clicking the *Full Manual Data Entry* checkbox.
10. Set the resistive bridge leg resistance to the second pressure value. For this example, use 5.0806k. Once complete, click *NEXT* to populate the ADC value in the cell. Repeat this process for the third and final pressure point, using a resistive bridge leg resistance of 5.0713k.
11. After completing the pressure readings, click *NEXT* to populate the temperature cell. The cell is automatically populated with the ADC value read from the internal temperature sensor of the PGA302. Click *NEXT* again.
12. The VDD Supply Voltage field is now automatically populated with the value measured by the ADC of the MSP430. If desired, then the *VDD Supply Voltage* can be measured externally from the test point labeled *VDD* on the EVM, and entered manually into the calibration page. Click *NEXT* again.
13. Now, the desired *VDD Supply Voltage* field is populated. Click *NEXT* again.
14. Click *CALCULATE*. This uses the data generated through the calibration procedure to calculate the coefficient values for linearity and temperature compensation and display them in the message center at the bottom of the page. Click *PROGRAM* to program the values to the EEPROM.
15. Navigate to the *PGA302 EEPROM Settings* page to verify the coefficients have been populated in the *Linearity Calibration Parameters* section of the page. While on this page, click the *UPDATE* button to correct the EEPROM CRC value. The PGA302 device is now fully calibrated.
16. To test the results of the calibration click the *Microcontroller State* field to begin running the microcontroller, and navigate to the *Voltage Monitor* tab in the tool panel.
17. Select the second pressure point in the *Resistive Bridge Configuration* panel, by setting the resistance of the leg to 5.0806k. The VOUT voltage in the tool panel needs to match the voltage selected for the Pressure 2 output during the calibration procedure.

3.13 PGA302 EEPROM Settings Page (PGA302 Only)

Figure 3-12 illustrates the PGA302 EEPROM settings page.



Linearity Calibration Parameters

H0 : 0x 0000 G0 : 0x 0000 N0 : 0x 0000 M0 : 0x 0000 PADC GAIN : 0x 00 Algorithm Type: Normal

H1 : 0x 0000 G1 : 0x 0000 N1 : 0x 0000 M1 : 0x 0000 TADC GAIN : 0x 00

H2 : 0x 0000 G2 : 0x 0000 N2 : 0x 0000 M2 : 0x 0000 PADC OFF : 0x 0000

H3 : 0x 0000 G3 : 0x 0000 N3 : 0x 0000 M3 : 0x 0000 TADC OFF : 0x 0000

Analog Front End Settings

P Channel Input
 Single Ended Input
 Invert Signal
 P GAIN : 1.33
 P MUX : VINPP - VINPN
 Offset Corr : OFF mV

T Channel Input
 Single Ended Input
 Invert Signal
 T GAIN : 1.33
 T MUX : VINTP - VINTN Pins

T Channel Current Drive
 ITEMP Select : 50 uA
 Destination : VINTP

DAC Output Settings

DAC Level During Diagnostic Fault : 0x 00 00 DACCAP Pin Enable :

Normal Output Range High Limit : 0x 0000 Output High Clamp Limit : 0x 0000

Normal Output Range Low Limit : 0x 0000 Output Low Clamp Limit : 0x 0000

Diagnostics Enable

VINP_OV PGAIN_OV
 VINP_UV PGAIN_UV
 VINT_OV TGAIN_OV
 VINT_UV TGAIN_UV

EEPROM Lock :
 Diagnostics Global Enable :
 Production Serial Number : 0x 00000000
 Output IIR Filter Cut-Off : OFF [Hz]
 Correct EEPROM CRC :

Note: When Updating Text Box Parameters, press the "Enter" key to program changes.

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Figure 3-12. PGA302 EEPROM Settings Page

When making changes to any parameters on the PGA302 EEPROM settings page, the new settings are automatically burned to the EEPROM. No separate programming action is required. However, updating the CRC once any of the EEPROM settings have been changed is necessary, including at the end of a calibration procedure.

3.13.1 Linearity Calibration Parameters

The linearity calibration parameters are automatically set once the *Linearity Calibration Procedure* (see Section 3.12.1) has been completed. No user input is necessary; however, individual coefficients can be changed manually if desired.

3.13.2 Analog Front End Settings

The *Analog Front End Settings* are the same as those included in the *Analog Front End* block diagram panel. To program the settings in the EEPROM, they must be entered in the *PGA302 EEPROM Settings* panel. For a full description of the Analog Front End Settings, see [Section 3.5](#).

3.13.3 DAC Output Settings

The DAC Output Settings allow the user to configure the DAC output ranges as well as the DAC output level during a fault.

3.13.4 Diagnostics Enable

Allows the user to enable analog front end diagnostic bits to be viewed in the *Fault Status* tab. See [Table 3-3](#) for a description of diagnostic bits.

3.13.5 Other Settings

Other settings on this page include locking the EEPROM so that the values cannot be changed, enabling all diagnostics with a single check box, viewing the production serial number of the PGA302 device (read only), or setting the *IIR Filter Cutoff* frequency.

3.14 Data Monitor Page



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Figure 3-13. Data Monitor Page

The *Data Monitor* page (see [Figure 3-13](#)) allows users to see the ADC sample values being read in real time. Data can be read from the P Channel, the T Channel, or both on the same graph. The number of samples recorded can be adjusted from 128 to 4096. By default, the graph continually loops until stopped by the user, but by unchecking the *Loop* checkbox the samples stop when the record length is reached.

Data can be exported to a .txt file format by clicking the *Export Data* button. The file contains all of the data currently displayed in the plot in a comma separated value format with the sample number, the P channel value, and the T channel value for each sample for easy data manipulation.

3.15 Tool Panel

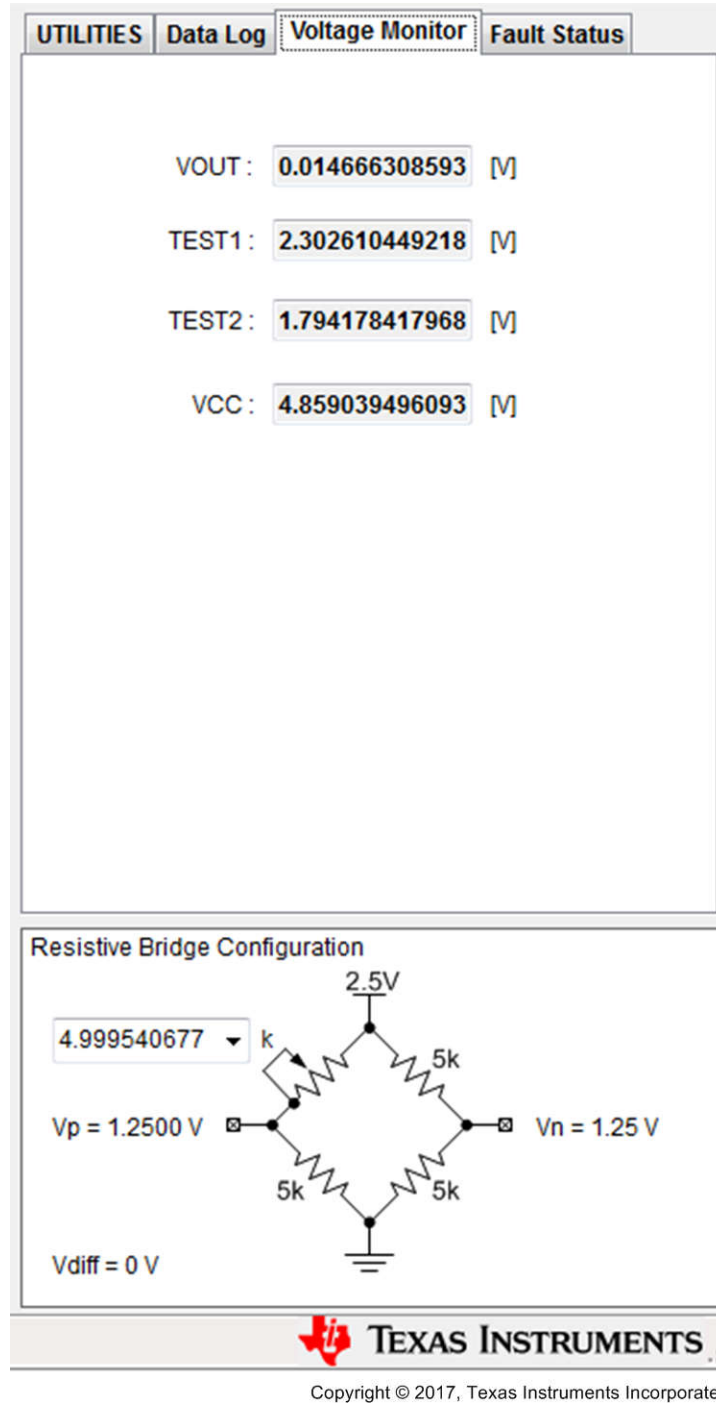
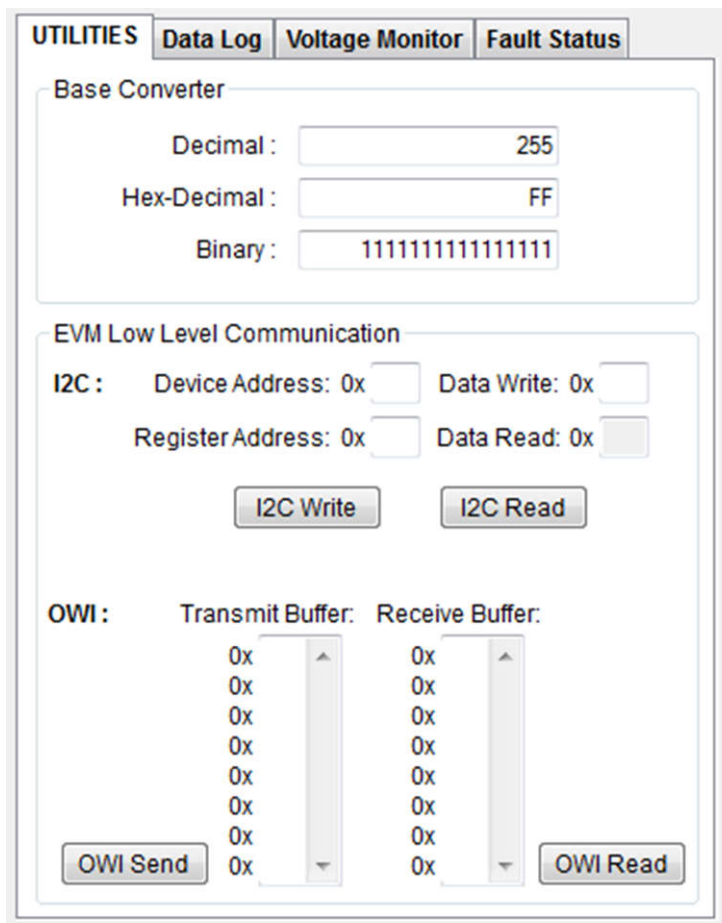


Figure 3-14. Tool Panel

3.15.1 Utilities Tab

The *UTILITIES* tab (see [Figure 3-15](#)) includes useful tools for interacting with the low level memory of the PGxxx device and for communication debugging purposes.



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Figure 3-15. UTILITIES tab

3.15.1.1 Base Converter

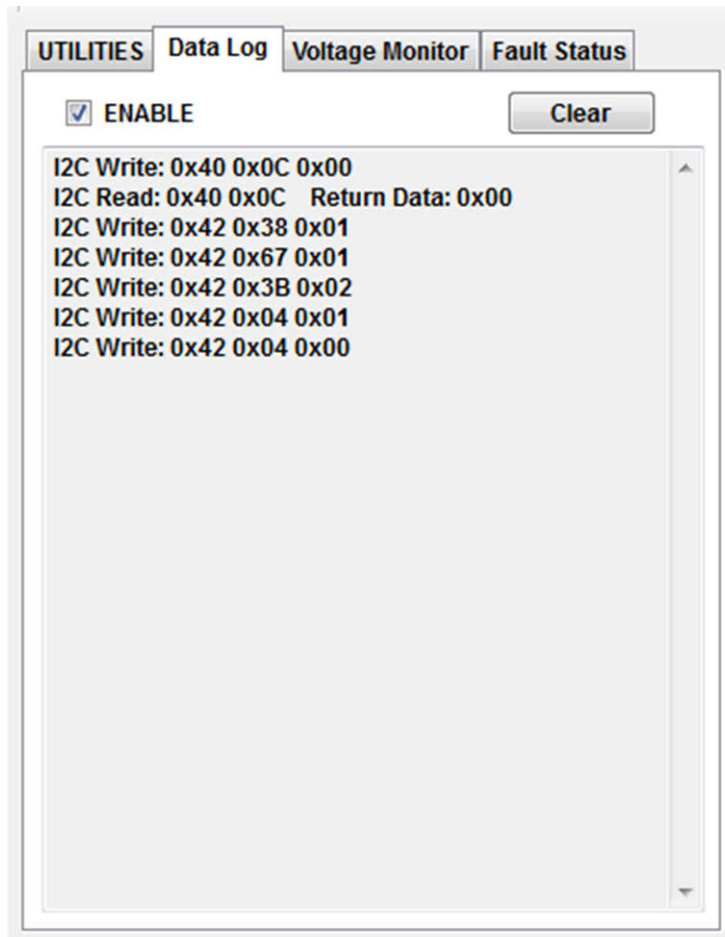
A base converter is included to quickly convert among decimal, hexadecimal, and binary number systems. Simply type a number into one of the three fields, and press the enter key to populate the converted values in the remaining two fields.

3.15.1.2 EVM Low-Level Communication

The *EVM Low-Level Communication* section allows for direct access to device registers, and provides an easy method to debug I2C and OWI communications. To configure a specific register enter the I2C device address, the PGxxx device register address desired, and the register value in the *Data Write* field then click the *I2C Write* button to send the data.

3.15.2 Data Log tab

The *Data Log* tab (see [Figure 3-16](#)) logs all communication functions between the GUI and the PGxxx device. Each line displays the communication type, followed by whether data was read or written, and finally the actual data in hexadecimal form.

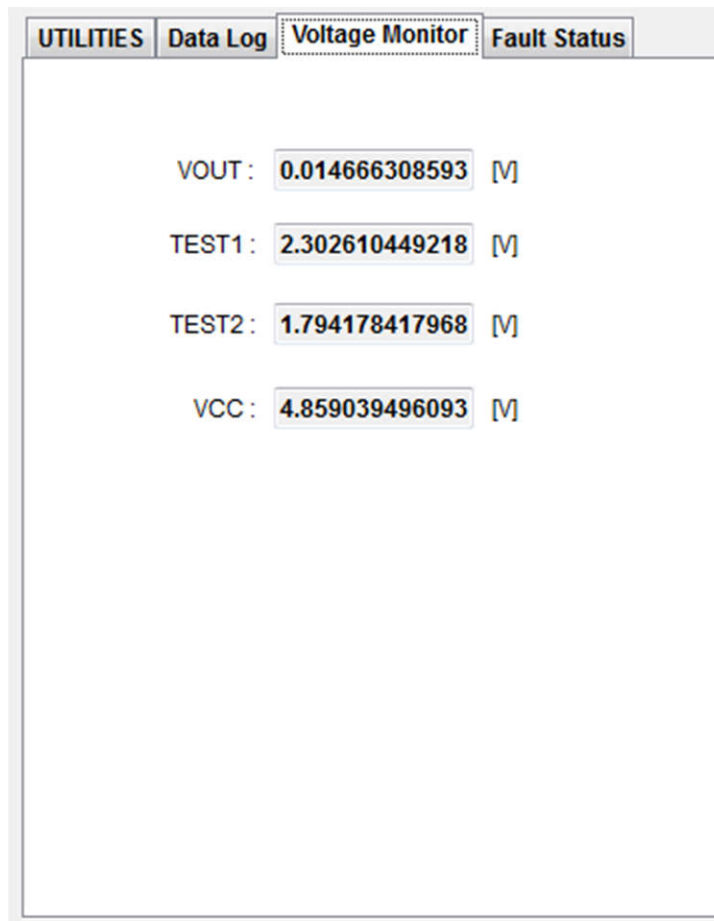


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Figure 3-16. Data Log Tab

3.15.3 Voltage Monitor Tab

The *Voltage Monitor* as illustrated in [Figure 3-17](#) provides a quick way to check vital system voltages for EVM functionality and debugging purposes. These voltages are measured via the ADC in the MSP430 microcontroller included on the EVM.

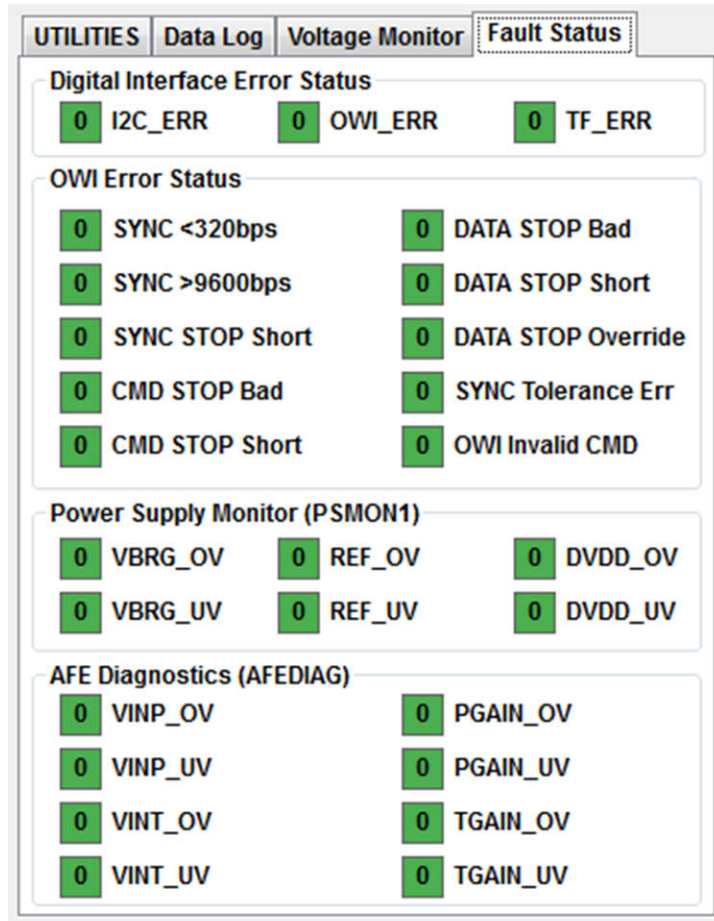


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Figure 3-17. Voltage Monitor Tab

3.15.4 Fault Status Tab

The *Fault Status* tab shown in [Figure 3-18](#) includes fault status registers for the digital interfaces, OWI status, the power supply monitor, and AFE diagnostics for quick diagnosis and debug of the most common device and EVM issues. [Table 3-3](#) describes the available fault status bits. Note that the *AFE Diagnostics* must be enabled in the EEPROM Settings before the diagnostics are updated in the *Fault Status* tab.



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Figure 3-18. Fault Status tab

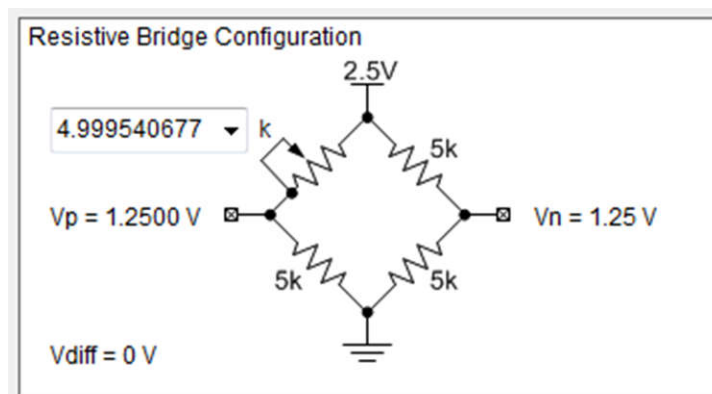
Table 3-3. Fault Status Indicators

Fault Indicator	Description
I2C_ERR	An error response on the access from I2C during access to the slave.
OWI_ERR	An error response on the access from OWI during access to the slave.
TF_ERR	Error response on the access from Trace FIFO
SYNC <320BPS	SYNC field data rate under 320 bits per second
SYNC >9600BPS	SYNC field data rate over 9600 bits per second
SYNC STOP Short	SYNC stop bit too short
CMD STOP Bad	Incorrect CMD stop bit value
CMD STOP Short	CMD stop bit too short
Data STOP Bad	Incorrect DATA stop bit value
Data STOP Short	DATA stop bit too short
Data STOP Override	DATA Field slave transmit value overdriven to dominant value during stop bit transmit.
SYNC Tolerance Err	Consecutive bits in the sync field are different by more than ±25% tolerance.
OWI Invalid CMD	OWI command field invalid. See device data sheet for available OWI commands.

Table 3-3. Fault Status Indicators (continued)

Fault Indicator	Description
VBRG_OV	Bridge Supply OV Flag; Bridge Supply voltage > 1.15 times nominal value.
VBRG_UV	Bridge Supply UV Flag; Bridge Supply voltage < 0.85 times nominal value
REF_OV	Reference OV Flag; Reference voltage > 1.1 times nominal value
REF_UV	Reference UV Flag; Reference voltage > 0.9 times nominal value
DVDD_OV	DVDD OV Flag; DVDD voltage > 1.15 times nominal value
DVDD_UV	DVDD UV Flag; DVDD voltage < 0.9 times nominal value
VINP_OV	Overvoltage on VINPP or VINPN pins
VINP_UV	Undervoltage on VINPP or VINPN pins
VINT_OV	Overvoltage on VINTP or VINTN pins
VINT_UV	Undervoltage on VINTP or VINTN pins
PGAIN_OV	Overvoltage at PGAIN output
PGAIN_UV	Undervoltage at PGAIN output
TGAIN_OV	Overvoltage at TGAIN output
TGAIN_UV	Undervoltage at TGAIN output

3.15.5 Resistive Bridge Configuration Panel



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Figure 3-19. Resistive Bridge Configuration Panel

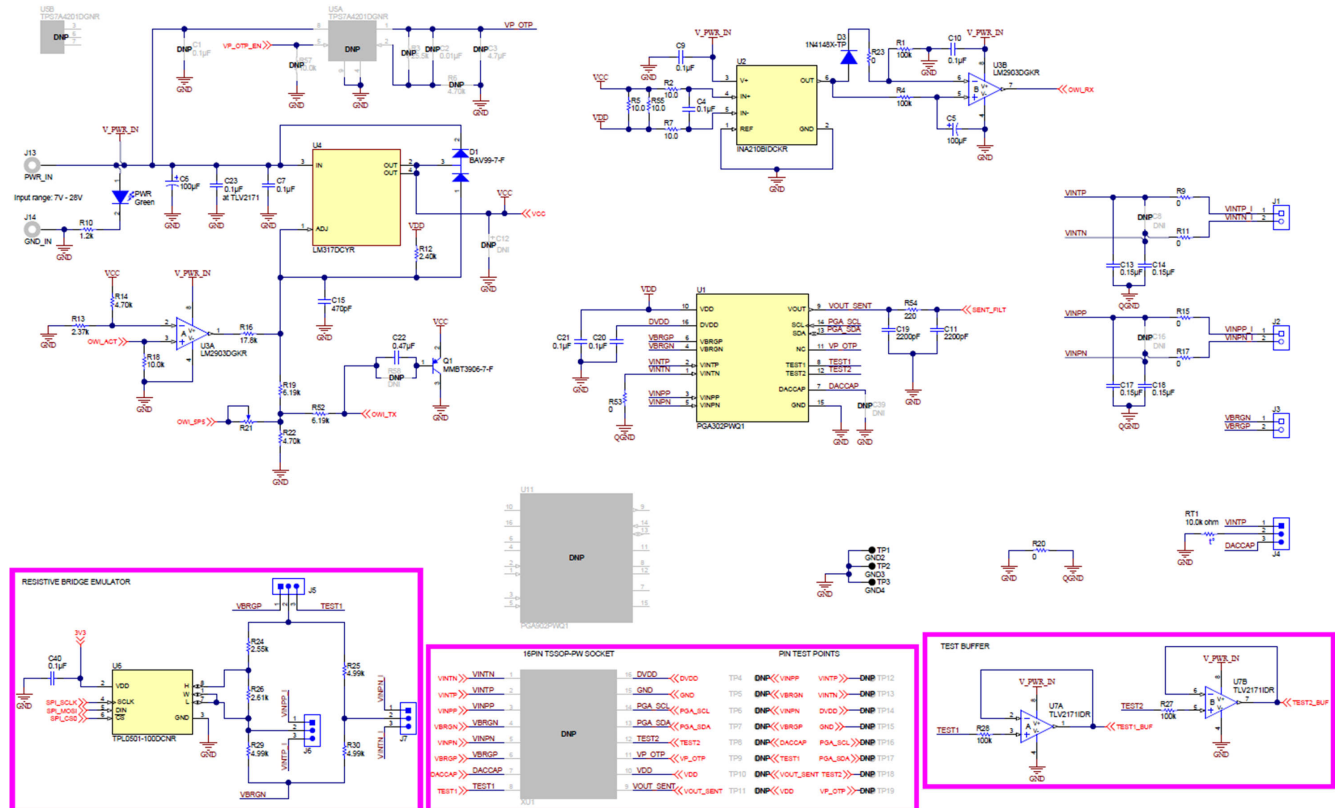
The *Resistive Bridge Configuration* panel allows the user to control the digital potentiometer that makes up one leg of the resistive bridge emulator on the EVM. This can be used to generate a differential voltage across the VINTP and VINTN or the VINPP and VINPN pins depending on the jumper configuration. The drop-down box allows the user to select a resistance in kΩ; the resulting change in the Vp voltage as well as the differential voltage of Vp – Vn are automatically updated in the schematic.

4 Hardware Design Files

4.1 Schematic

Note

The schematic pictured in [Figure 4-1](#) shows the board configuration for the PGA904EVM which includes additional components populated for OTP programming and a socket for the PGAxXX devices.



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Figure 4-1. PGA302EVM Schematic

Hardware Design Files

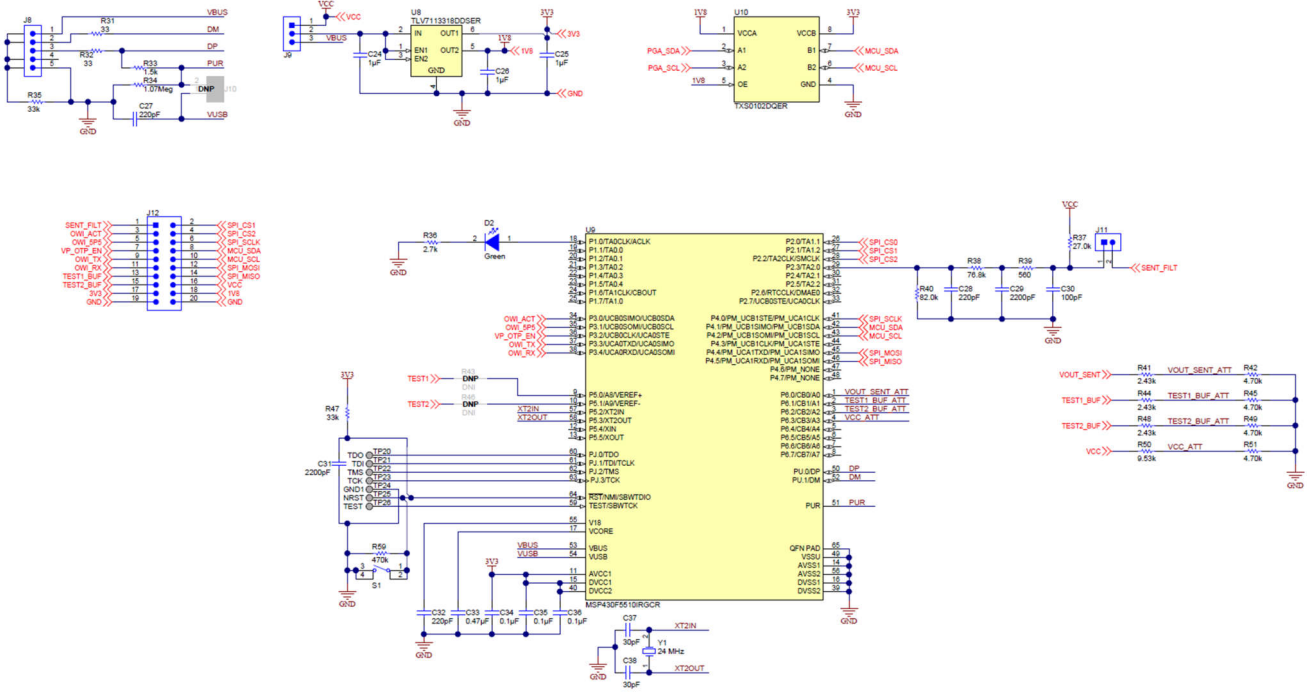
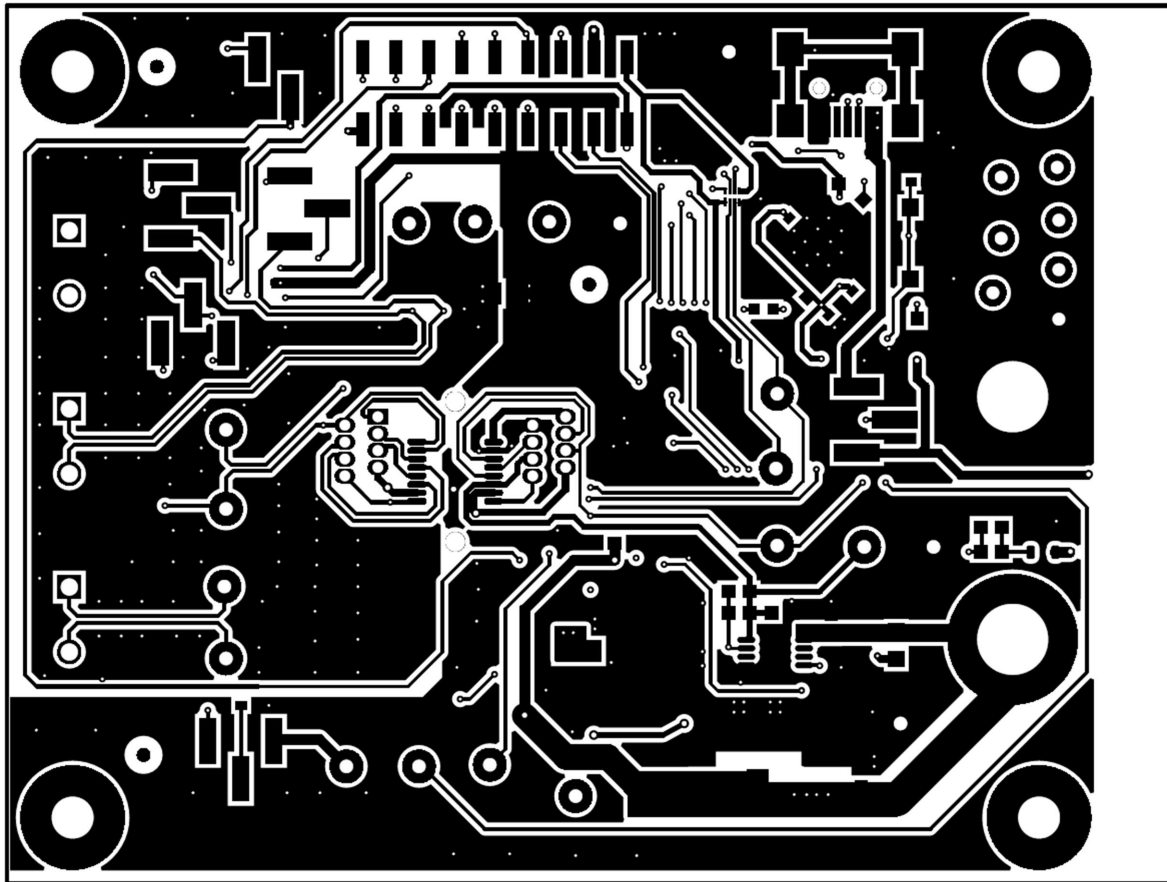


Figure 4-2. PGAxxEVM MSP430 Interface Schematic

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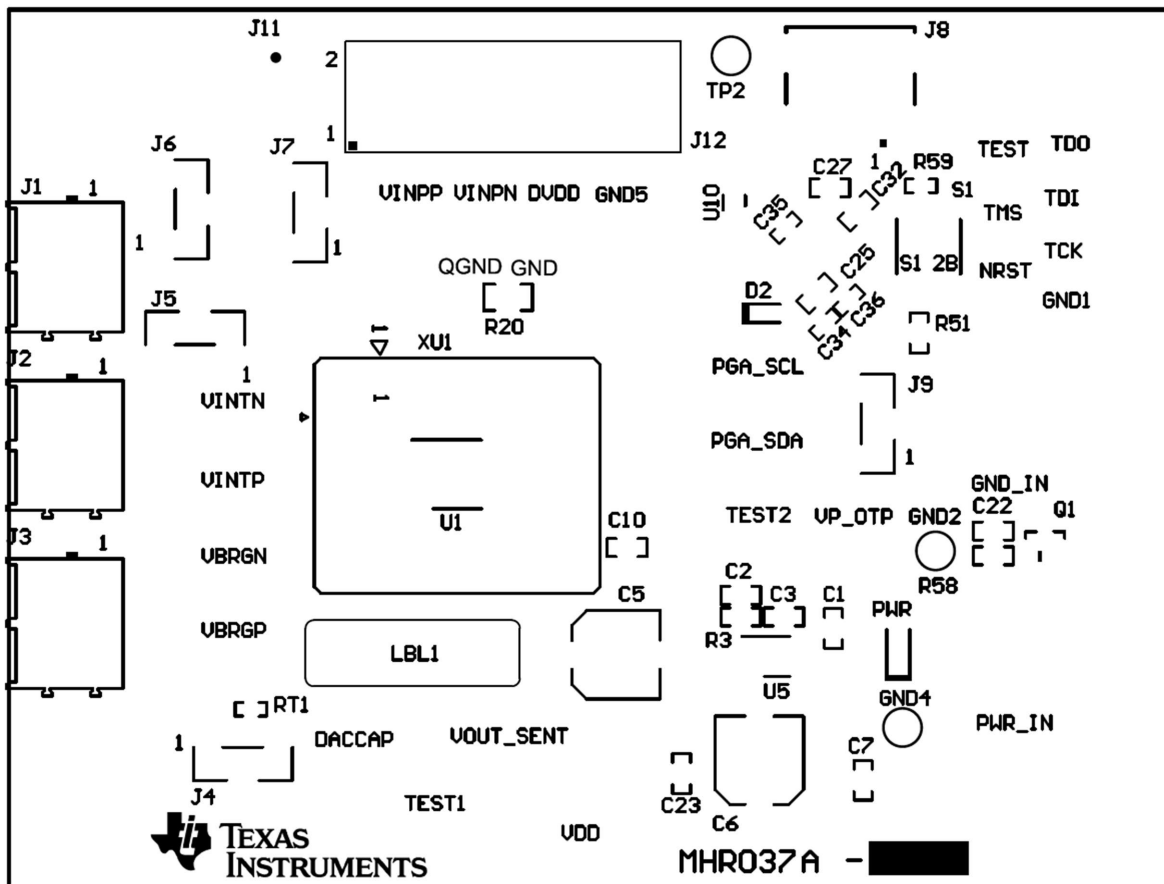
4.2 Board Layout

Figure 4-3 through Figure 4-6 illustrate the EVM PCB layouts.



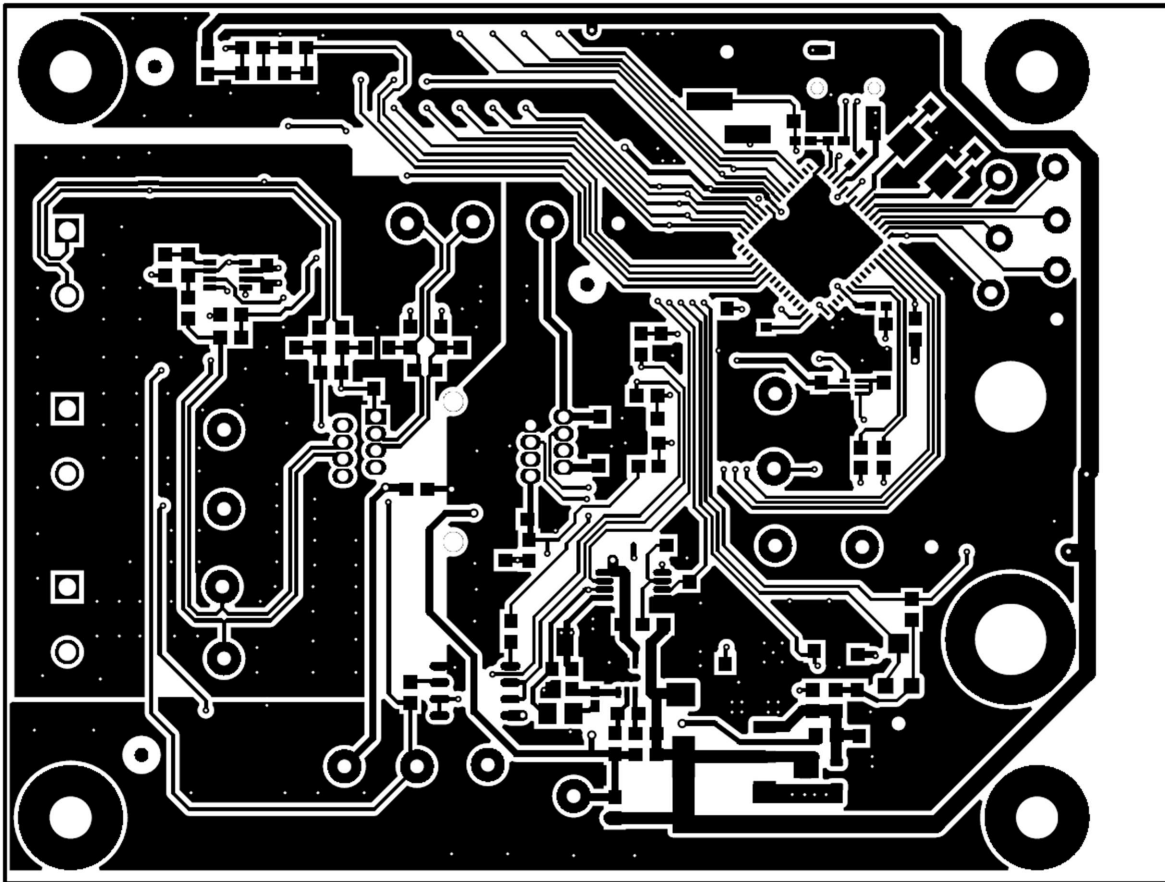
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Figure 4-3. Top Layer



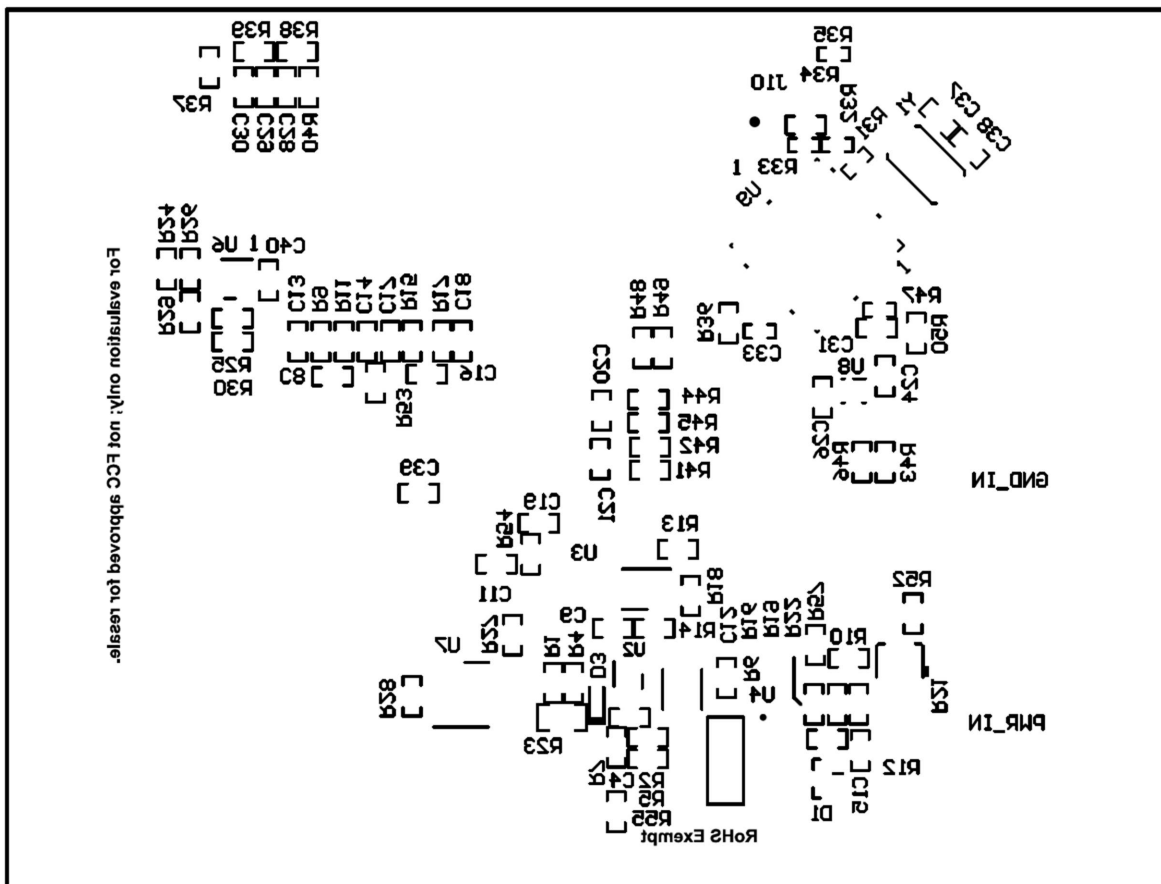
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Figure 4-4. Top Component Placement



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Figure 4-5. Bottom Layer



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Figure 4-6. Bottom Component Placement

4.3 Bill of Materials

Note

The bill of materials in [Table 4-1](#) shows the components for the PGA904EVM-037. The PGA302EVM-037 and PGA904EVM-037 contain fewer components, but any component present on all three boards have the same value and part number.

Table 4-1. Bill of Materials⁽¹⁾

Designator	QTY	Value	Description	Package Reference	Part Number	Manufacturer	Alternate Part Number	Alternate Manufacturer
!PCB1	1		Printed Circuit Board		MHR037	Any		
C4, C7, C9, C10, C20, C21, C23, C40	8	0.1uF	CAP, CERM, 0.1µF, 50V, ±10%, X7R, 0603	0603	C0603C104K5RACTU	Kemet		
C5	1	100uF	CAP, AL, 100µF, 35V, ±20%, SMD	F80	EMVA350ADA101MF80G	Chemi-Con		
C6	1	100uF	CAP, AL, 100µF, 35V, ±20%, 0.34 ohm, SMD	F80	EMZA350ADA101MF80G	Chemi-Con		
C11, C19, C29	3	2200pF	CAP, CERM, 2200pF, 50V, ±10%, X7R, 0603	0603	C0603C222K5RAC	Kemet		
C13, C14, C17, C18	4	0.15uF	CAP, CERM, 0.15µF, 16V, +80/-20%, Y5V, 0603	0603	C0603C154Z4VACTU	Kemet		
C15	1	470pF	CAP, CERM, 470pF, 50V, ±10%, X7R, 0603	0603	C0603C471K5RACTU	Kemet		
C22	1	0.47uF	CAP, CERM, 0.47µF, 10V, ±10%, X5R, 0603	0603	C0603C474K8PACTU	Kemet		
C24, C25, C26	3	1uF	CAP, CERM, 1µF, 16V, ±10%, X5R, 0603	0603	C0603C105K4PACTU	Kemet		
C27, C32	2	220pF	CAP, CERM, 220pF, 50V, ±1%, C0G/NP0, 0603	0603	06035A221FAT2A	AVX		
C28	1	220pF	CAP, CERM, 220pF, 50V, ±10%, C0G/NP0, 0603	0603	C0603C221K5GACTU	Kemet		
C30	1	100pF	CAP, CERM, 100pF, 50V, ±5%, C0G/NP0, 0603	0603	C0603C101J5GAC	Kemet		
C31	1	2200pF	CAP, CERM, 2200pF, 50V, ±10%, X7R, 0603	0603	C0603X222K5RACTU	Kemet		
C33	1	0.47uF	CAP, CERM, 0.47µF, 10V, ±10%, X5R, 0402	0402	C1005X5R1A474K050BB	TDK		
C34, C35, C36	3	0.1uF	CAP, CERM, 0.1µF, 10V, ±10%, X5R, 0402	0402	C1005X5R1A104K	TDK		
C37, C38	2	30pF	CAP, CERM, 30pF, 50V, ±5%, C0G/NP0, 0603	0603	GRM1885C1H300JA01D	Murata		
D1	1	75V	Diode, Switching, 75V, 0.3A, SOT-23	SOT-23	BAV99-7-F	Diodes Inc.		
D2	1	Green	LED, Green, SMD	1.6x0.8x0.8mm	LTST-C190GKT	Lite-On		
D3	1	75V	Diode, Switching, 75V, 0.3A, SOD-523	SOD-523	1N4148X-TP	Micro Commercial Components		
H1, H2, H3, H4	4		Machine Screw, Round, #4-40 x 1/4, Nylon, Phillips panhead	Screw	NY PMS 440 0025 PH	BandF Fastener Supply		
H5, H6, H7, H8	4		Standoff, Hex, 0.5"L #4-40 Nylon	Standoff	1902C	Keystone		
J1, J2, J3	3		Thermal Block, 5mm, 2-pole, TH	TH, 2-Leads, Body 10x9mm, Pitch 5mm	1935161	Phoenix Contact		
J4, J5, J6, J7, J9	5		Header, 100mil, 3x1, Gold, SMT	Samtec_TSM-103-01-X-SV	TSM-103-01-L-SV	Samtec		
J8	1		Conn Rcpt Mini USB2.0 Type B 5POS SMD	USB Mini Type B	1734035-2	TE Connectivity		
J11	1		Header, 100mil, 2x1, Gold with Tin Tail, SMT	2x1 Header	TSM-102-01-L-SV	Samtec		
J12	1		Header, 100mil, 10x2, Tin, SMT	1000x180x290mil	TSM-110-01-T-DV-P	Samtec		
J13, J14	2		Standard Banana Jack, Uninsulated, 5.5mm	Keystone_575-4	575-4	Keystone		
LBL1	1		Thermal Transfer Printable Labels, 0.650" W x 0.200" H - 10,000 per roll	PCB Label 0.650"H x 0.200"W	THT-14-423-10	Brady		
PWR	1	Green	LED, Green, SMD	2x1.25mm	LG R971-KN-1	OSRAM		

Table 4-1. Bill of Materials⁽¹⁾ (continued)

Designator	QTY	Value	Description	Package Reference	Part Number	Manufacturer	Alternate Part Number	Alternate Manufacturer
Q1	1	40V	Transistor, PNP, 40V, 0.2A, SOT-23	SOT-23	MMBT3906-7-F	Diodes Inc.		
R1, R4, R27, R28	4	100k	RES, 100 k, 1%, 0.1 W, 0603	0603	RC0603FR-07100KL	Yageo America		
R2, R5, R7, R55	4	10.0	RES, 10.0, 1%, 0.1 W, 0603	0603	RC0603FR-0710RL	Yageo America		
R9, R11, R15, R17, R53	5	0	RES, 0, 5%, 0.1 W, 0603	0603	RC0603JR-070RL	Yageo America		
R10	1	1.2k	RES, 1.2 k, 5%, 0.1 W, 0603	0603	RC0603JR-071K2L	Yageo America		
R12	1	2.40k	RES, 2.40 k, 1%, 0.1 W, 0603	0603	RC0603FR-072K4L	Yageo America		
R13	1	2.37k	RES, 2.37 k, 1%, 0.1 W, 0603	0603	RC0603FR-072K37L	Yageo America		
R14, R22, R42, R45, R49, R51	6	4.70k	RES, 4.70 k, 1%, 0.1 W, 0603	0603	RC0603FR-074K7L	Yageo America		
R16	1	17.8k	RES, 17.8 k, 1%, 0.1 W, 0603	0603	RC0603FR-0717K8L	Yageo America		
R18	1	10.0k	RES, 10.0 k, 1%, 0.1 W, 0603	0603	RC0603FR-0710KL	Yageo America		
R19, R52	2	6.19k	RES, 6.19 k, 1%, 0.1 W, 0603	0603	RC0603FR-076K19L	Yageo America		
R20	1	0	RES, 0, 5%, 0.125 W, 0805	0805	RC0805JR-070RL	Yageo America		
R21	1		TRIMMER 10K OHM 0.1W	3.8x3.6mm	TC33X-2-103E	Bourns		
R23	1	0	RES, 0, 5%, 0.125 W, 0805	0805	CRCW08050000Z0EA	Vishay-Dale		
R24	1	2.55k	RES, 2.55 k, 0.1%, 0.1 W, 0603	0603	RT0603BRD072K55L	Yageo America		
R25, R29, R30	3	4.99k	RES, 4.99 k, 0.1%, 0.1 W, 0603	0603	RT0603BRD074K99L	Yageo America		
R26	1	2.61k	RES, 2.61 k, 0.1%, 0.1 W, 0603	0603	RT0603BRD072K61L	Yageo America		
R31, R32	2	33	RES, 33 ohm, 5%, 0.063W, 0402	0402	CRCW040233R0JNED	Vishay-Dale		
R33	1	1.5k	RES, 1.5k ohm, 5%, 0.063W, 0402	0402	CRCW04021K50JNED	Vishay-Dale		
R34	1	1.07Meg	RES, 1.07Meg ohm, 1%, 0.1W, 0603	0603	CRCW06031M07FKEA	Vishay-Dale		
R35, R47	2	33k	RES, 33k ohm, 5%, 0.063W, 0402	0402	CRCW040233K0JNED	Vishay-Dale		
R36	1	2.7k	RES, 2.7 k, 5%, 0.1 W, 0603	0603	RC0603JR-072K7L	Yageo America		
R37	1	27.0k	RES, 27.0 k, 1%, 0.1 W, 0603	0603	RC0603FR-0727KL	Yageo America		
R38	1	76.8k	RES, 76.8 k, 1%, 0.1 W, 0603	0603	RC0603FR-0776K8L	Yageo America		
R39	1	560	RES, 560, 1%, 0.1 W, 0603	0603	RC0603FR-07560RL	Yageo America		
R40	1	82.0k	RES, 82.0 k, 1%, 0.1 W, 0603	0603	RC0603FR-0782KL	Yageo America		
R41, R44, R48	3	2.43k	RES, 2.43 k, 1%, 0.1 W, 0603	0603	RC0603FR-072K43L	Yageo America		
R50	1	9.53k	RES, 9.53 k, 1%, 0.1 W, 0603	0603	RC0603FR-079K53L	Yageo America		
R54	1	220	RES, 220, 1%, 0.1 W, 0603	0603	RC0603FR-07220RL	Yageo America		
R59	1	470k	RES, 470 k, 1%, 0.0625 W, 0402	0402	RC0402FR-07470KL	Yageo America		
RT1	1	10.0k ohm	Thermistor NTC, 10.0k ohm, 1%, 0402	0402	NCP15XH103F03RC	Murata		
S1	1		Switch, Tactile, SPST-NO, 0.1A, 16V, SMT	4.93x4.19x6.2 mm	7914G-1-000E	Bourns		
SH-J4, SH-J5, SH-J6, SH-J7, SH-J9	5		Shunt, 100mil, Gold plated, Black	Shunt 2 pos. 100 mil	881545-2	TE Connectivity		
TP1, TP2, TP3	3	Black	Test Point, Miniature, Black, TH	Black Miniature Test point	5001	Keystone		
U1	1		Sensor Signal Conditioner with 0-5V Ratiometric Output, PW0016A (TSSOP-16)	PW0016A	PGA302PWQ1	Texas Instruments		
U2	1		Voltage Output, Low- or High-Side Measurement, Bidirectional, Zero-Drift Series, Current-Shunt Monitor, DCK0006A (SOT-6)	DCK0006A	INA210BIDCKR	Texas Instruments	INA210BIDCKT	Texas Instruments
U3	1		DUAL DIFFERENTIAL COMPARATORS, DGK0008A	DGK0008A	LM2903DGKR	Texas Instruments		Texas Instruments

Table 4-1. Bill of Materials⁽¹⁾ (continued)

Designator	QTY	Value	Description	Package Reference	Part Number	Manufacturer	Alternate Part Number	Alternate Manufacturer
U4	1		3-TERMINAL ADJUSTABLE REGULATOR, DCY0004A	DCY0004A	LM317DCYR	Texas Instruments	LM317DCY	Texas Instruments
U6	1		256 Taps Single Channel Digital Potentiometer With SPI, DCN0008A	DCN0008A	TPL0501-100DCNR	Texas Instruments		
U7	1		36V, Single-Supply, Low-Power Operational Amplifier for Cost-Sensitive Systems, D0008A (SOIC-8)	D0008A	TLV2171IDR	Texas Instruments		
U8	1		Dual Output High PSRR LDO, 200mA, Fixed 3.3, 1.8V Output, 2 to 5.5V Input, 6-pin WSON (DSE), -40 to 125 degC, Green (RoHS and no Sb/Br)	DSE0006A	TLV7113318DDSER	Texas Instruments	Equivalent	Texas Instruments
U9	1		25MHz Mixed Signal Microcontroller with 32 KB Flash, 4096 B SRAM and 47 GPIOs, -40 to 85 degC, 64-pin QFN (RGC), Green (RoHS and no Sb/Br)	RGC0064B	MSP430F5510IRGCR	Texas Instruments	Equivalent	Texas Instruments
U10	1		2-Bit Bidirectional Voltage-Level Translator for Open-Drain and Push-Pull Application, DQE0008A	DQE0008A	TXS0102DQER	Texas Instruments		
Y1	1		Crystal, 24MHz, 18pF, SMD	ABM3	ABM3-24.000MHZ-D2Y-T	Abracon Corporation		
C1	0	0.1uF	CAP, CERM, 0.1µF, 50V, ±10%, X7R, 0603	0603	C0603C104K5RACTU	Kemet		
C2, C8, C16	0	0.01uF	CAP, CERM, 0.01µF, 25V, ±5%, C0G/NP0, 0603	0603	C0603H103J3GACTU	Kemet		
C3	0	4.7uF	CAP, CERM, 4.7µF, 10V, ±10%, X5R, 0603	0603	C0603C475K8PACTU	Kemet		
C12	0	1uF	CAP, TA, 1µF, 35V, ±10%, 1.7 ohm, SMD	3528-21	T495B105K035ATE1K7	Kemet		
C39	0	2200pF	CAP, CERM, 2200pF, 50V, ±10%, X7R, 0603	0603	C0603C222K5RAC	Kemet		
FID1, FID2, FID3, FID4, FID5, FID6	0		Fiducial mark. There is nothing to buy or mount.	Fiducial	N/A	N/A		
J10	0		Header, 100mil, 2x1, Gold with Tin Tail, SMT	2x1 Header	TSM-102-01-L-SV	Samtec		
R3	0	25.5k	RES, 25.5 k, 1%, 0.1 W, 0603	0603	RC0603FR-0725K5L	Yageo America		
R6	0	4.70k	RES, 4.70 k, 1%, 0.1 W, 0603	0603	RC0603FR-074K7L	Yageo America		
R43, R46	0	0	RES, 0, 5%, 0.1 W, 0603	0603	RC0603JR-070RL	Yageo America		
R57	0	10.0k	RES, 10.0 k, 1%, 0.1 W, 0603	0603	RC0603FR-0710KL	Yageo America		
R58	0	4.70Meg	RES, 4.70M, 1%, 0.1W, 0603	0603	RC0603FR-074M7L	Yageo America		
U5	0		Single Output LDO, 50mA, Adjustable 1.175 to 26V Output, 7 to 28V Input, 8-pin MSOP (DGN), -40 to 125 degC, Green (RoHS and no Sb/Br)	DGN0008B	TPS7A4201DGNR	Texas Instruments	Equivalent	Texas Instruments
U11	0		Sensor Signal Conditioner with 0-5V Ratiometric Output, PW0016A (TSSOP-16)	PW0016A	PGA902PWQ1	Texas Instruments		
XU1	0		Socket, SOP-16, 0.65mm Pitch, TH	Socket, 16-Leads, Body 17.6X21.5mm, Pitch 0.65mm	OTS-16(28)-0.65-01	Enplas Tech Solutions		

(1) Unless otherwise noted in the Alternate Part Number or Alternate Manufacturer columns, all parts can be substituted with equivalents.

5 Additional Information

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6 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (December 2017) to Revision A (July 2024)	Page
• Added <i>Selective Disclosure</i> banner on document.....	1

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