

PRU-ICSS HSR-PRP DAN Firmware Data Sheet

FEATURES

- RTOS support for AMIC1x, AM3x, AM4x, AM5x & K2G devices.
- RT-Linux support for AM57xx devices.
- The implementation is as per IEC 62439-3 Ed 2.0.
 - HSR as per clause 5
 - PRP as per clause 4
- LRE implemented completely in firmware
- HSR - High-Availability Seamless Redundancy
 - Operates as a DANH
 - Support for modes – H, T, U and N as per standard
 - Two ports as per standard, Port A and Port B
 - Modes can be changed at runtime
- PRP – Parallel Redundancy Protocol
 - Operates as a DANP
 - Two ports as per standard, Port A and Port B
- Quality of Service (QoS)
 - Two priority receive queues on host port, each queue 6 KB in size
 - Four priority transmit queues on each physical port, each queue 3 KB in size
 - Support for QoS based on 3-bit VLAN PCP i.e. No of levels supported : 8
 - Number of host queues : 2 | 4 QoS levels per host queue
 - Number of port queues : 4 | 2 QoS levels per port queue
- Node Table
 - Total 128 entries on AMICx, AM335x, AM437x
 - Total 256 entries on AM57xx & K2G
 - Hash Table for faster lookup
 - O(1) complexity
- Node forget time of 60 sec
- Node Table statistics
- Support for Multicast Filtering
 - Supported on all devices
 - Hash Table for faster lookup
 - O(1) complexity
- Support for VLAN Filtering for host port
 - Supported on all devices
 - Hash Table for faster lookup
 - O(1) complexity
- Host Rx interrupt pacing
 - Supported on all devices
 - Individual interrupt per port
 - Pacing timer configurable per port
- Duplicate Discard Table
 - Duplicate discard on Port to Host path (HSR and PRP)
 - Duplicate discard table on Port to Port path (HSR)
 - Data integrity (CRC) check during port to port forwarding, except cut through (HSR)
- PHY Configuration
 - Duplex : Full/Auto
 - Speed : 100/Auto
 - 10mbps and Half duplex modes are not supported
- Statistics
 - Supports all MIB statistics as per standard
 - Node Table statistics for debugging
 - Self-configuring
- PTP/1588 – Time Synchronization
 - PTP Slave and Master mode
 - Supports P2P clock.
 - PTP over 802.3 (Annex F)
 - Transparent Clock supported
 - Ordinary Clock supported
 - Single and Two step clock supported
 - Peer delay Response is always sent as two-step

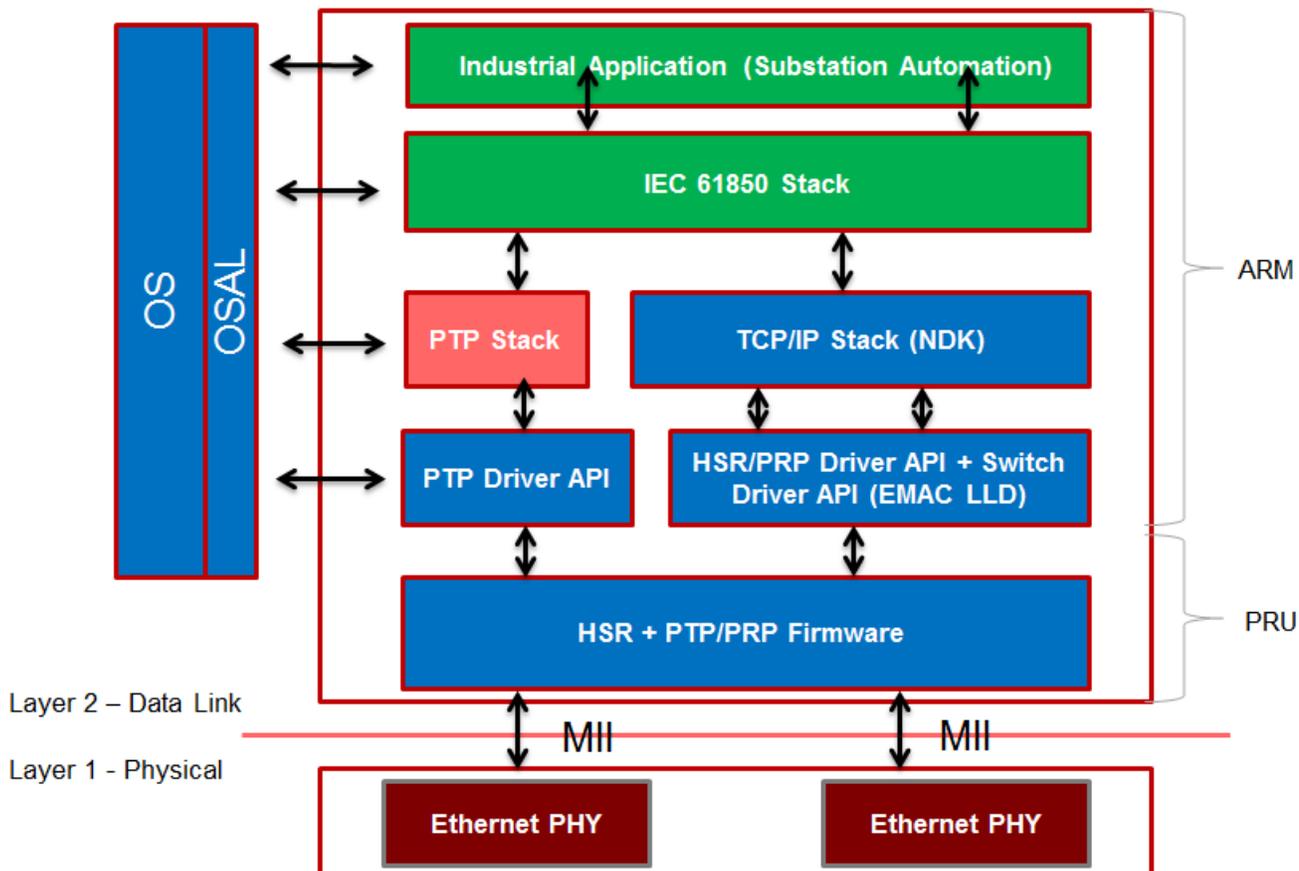


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- 1 ms buffering per port
- Multicast and Broadcast storm prevention per port
- Interrupt for Link loss detection.
 - Link loss detection in under 200us
 - Callback API's to perform tasks related to change in network topology
- PHY Configuration
 - Duplex : Full/Auto
 - Speed : 100/Auto
 - 10mbps and Half duplex modes are not supported

Description

PRU-ICSS HSR PRP DAN firmware implements HSR + PTP and PRP DANH and DANP functionality respectively integrated into AM335x, AM437x and AM57x class of devices. PRU-ICSS HSR PRP software from TI can be used by customers to add HSR/PRP DAN functionality on top of Processor SDK to Sitara processors.



HSR and PRP are Layer 2 redundancy protocols, they exist as a LRE between the MAC and Network layer above providing a transparent view of the MAC below to the application. Every packet is duplicated by the HSR/PRP driver on it's way out and only a single copy of the duplicates arriving is forwarded to Host.

The HSR/PRP driver layer replaces the Rx and Tx API's from EMAC LLD with it's own implementation of Rx and Tx functions. The API structure remains the same but the internals change to provide an LRE. Other tasks like link management, MDIO etc are still performed by the EMAC LLD. The additional feature in firmware is PTP.

HSR/PRP DAN firmware for PRU-ICSS is a black box product maintained by TI. HSR/PRP driver allows loading and run HSR/PRP firmware and interface with the firmware.

HSR/PRP Driver is provided in full source so that customers can adapt this implementation to own hardware and Operating Systems. This driver provides stack interface for queue management, Rx, Tx, PTP Configuration, management.

Operating System, Switch Driver (ICSS EMAC LLD), TCP/IP Stack (NDK) and associated documentation is available through Processor SDK. See Software section for details

Performance Summary

A 300 MHz CPU speed is sufficient to support a simple IO or sensor application. More complex applications can use higher speed grades of up to 1.5 GHz. The PRU core speed remains 200 MHz for all speed grades.

Memory Summary

This section describes memory usage of the HSR/PRP PRU-ICSS firmware and Cortex-A driver.

Table 1 HSR/PRP PRU-ICSS Firmware Memory Statistics

AM335x/AM437x/AMIC11x

Memory (in bytes)	HSR		PRP		Remarks
	Program memory	Data memory	Program memory	Data memory	
PRU0	7696	8192	7072	8192	Statistics + DBG variables + Host duplicate table
PRU1	7152	7968	6740	7968	Queue context + Statistics + port duplicate table
PRU-ICSS SHARED RAM	NA	11968	NA	11968	Buffer descriptors + PTP + Node Table
L3 OCMC RAM	NA	54272	NA	54272	Receive and Transmit Queues

AM57xx/K2G

Memory (in bytes)	HSR		PRP		Remarks
	Program memory	Data memory	Program memory	Data memory	
PRU0	7552	6536	7552	7576	Statistics + DBG variables + Host duplicate table
PRU1	7188	7968	6768	7968	Queue context + Statistics + port duplicate table
PRU-ICSS SHARED RAM	NA	16128	NA	16128	Buffer descriptors + PTP + Node Table
L3 OCMC RAM	NA	54272	NA	54272	Receive and Transmit Queues

Hardware Requirements

- Sitara Processor with PRU-ICSS IP and HSR/PRP support
- HSR/PRP implementation uses following interrupts mapped to Host Interrupt Controller

Stack/application interrupts		
Firmware interrupt	Host Interrupt	Remarks
Frame Receive	PRU_ICSS_EVTOUT0	Notifies host when firmware has stored a frame in host receive queue
Tx Callback Interrupt	PRU_ICSS_EVTOUT3	Raised when a PTP/1588 frame which requires Tx Timestamping is sent out
Link 0	PRU_ICSS_EVTOUT6	Interrupt is raised when the Link on MII0 port comes up or goes down
Link 1	PRU_ICSS_EVTOUT6	Interrupt is raised when the Link on MII1 port comes up or goes down

- HSR + PTP implementation makes use of one channel of EDMA for PTP implementation

- HW signals required to implement HSR/PRP DAN functionality is shown below, this info needs to be used in conjunction with <http://www.ti.com/tool/PINMUXTOOL>

NOTE: w.r.t prX, X is 1 or 2 (respectively PRU-ICSS1 and PRU-ICSS2 – refer to SOC TRM for availability)

Table 2 PRU-ICSS signals required for HSR/PRP functionality

Signal name		Description
PRU-ICSS MDIO		
prX_mdio_mdclk	Mandatory	MDIO clock
prX_mdio_data	Mandatory	MDIO data
PRU-ICSS MII PORT0 PRU-ICSS MII PORT1		
prX_mii_mt0_clk	Mandatory	MII0 and MII1 transmit clock
prX_mii_mt1_clk		
prX_mii0_txd3	Mandatory	MII0 and MII1 transmit data3
prX_mii1_txd3		
prX_mii0_txd2	Mandatory	MII0 and MII1 transmit data2
prX_mii1_txd2		
prX_mii0_txd1	Mandatory	MII0 and MII1 transmit data1
prX_mii1_txd1		
prX_mii0_txd0	Mandatory	MII0 and MII1 transmit data0
prX_mii1_txd0		
prX_mii0_rxd3	Mandatory	MII0 and MII1 receive data3
prX_mii1_rxd3		
prX_mii0_rxd2	Mandatory	MII0 and MII1 receive data2
prX_mii1_rxd2		
prX_mii0_rxd1	Mandatory	MII0 and MII1 receive data1
prX_mii1_rxd1		
prX_mii0_rxd0	Mandatory	MII0 and MII1 receive data0
prX_mii1_rxd0		
prX_mii0_txen	Mandatory	MII0 and MII1 TX enable
prX_mii1_txen		
prX_mii_mr0_clk	Mandatory	MII0 and MII1 receive clock
prX_mii_mr1_clk		
prX_mii0_rxdv	Mandatory	MII0 and MII1 RX data valid
prX_mii1_rxdv		
prX_mii0_rxer	Mandatory	MII0 and MII1 RXERR
prX_mii1_rxer		
prX_mii0_rxlink	Optional	For fast link loss detection - connect LED_LINK/LED_SPEED from PHY here and enable MLINK mode in MDIO
prX_mii1_rxlink		
PRU-ICSS PTP/1588 Clocks (Network clock synchronization)		
prX_edc_sync0_out	Recommended (for PTP/1588 capable slaves)	SYNC0 out - Time synchronized OUT0

References

1. [High-availability Seamless Redundancy \(HSR\) Ethernet for Substation Automation Reference Design](#)
2. [Parallel Redundancy Protocol \(PRP\) Ethernet Reference Design for Substation Automation](#)

3. [HSR/PRP DAN Developer Guide](#)

Acronyms

Acronym	Description
AL	Application Layer
ASIC	Application Specific Integrated Circuit
DL	Datalink Layer
HSR	H igh- A vailability S eamless R edundancy protocol
PRP	Parallel Redundancy Protocol
DAN	Dual Attached Node
DANH	Dual Attached Node (HSR)
DANP	Dual Attached Node (PRP)
LRE	Link Redundancy Entity
ISR	Interrupt Service Routine
MDIO	Management Data Input Output
MII	Media Independent Interface
OS	Operating Systems
PRUSS	Programmable Real-Time Unit Sub System
PRU-ICSS	Programmable Real-Time Unit - Industrial Communication Sub System - PRUSS with industrial communication support
PTP-1588	Precision Time Protocol (IEEE time synchronization protocol)
RPI	Requested Packet Interval

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