
PRU-ICSS PROFINET IRT Slave Firmware Data Sheet

FEATURES

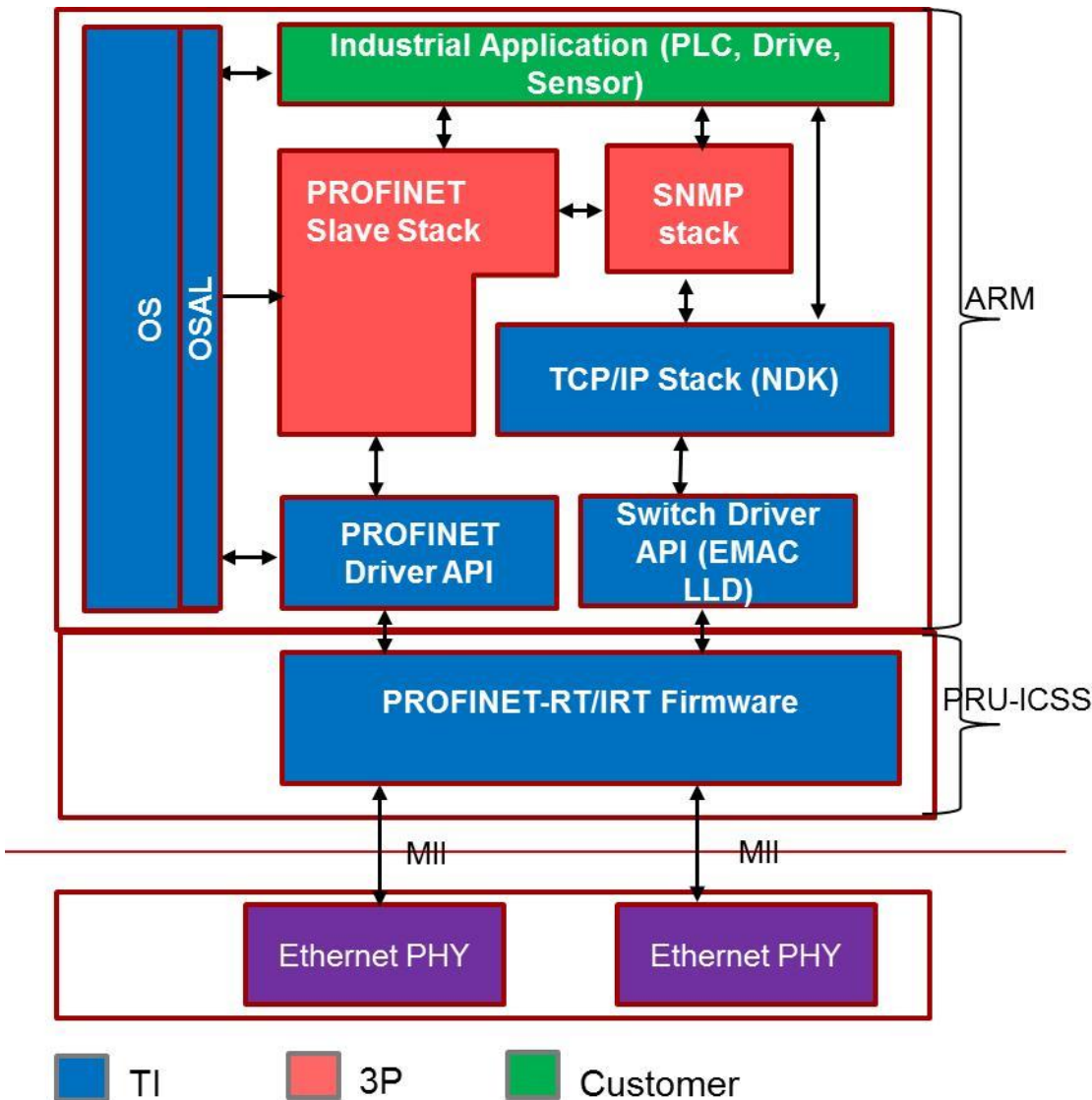
- PROFINET I/O RT/IRT Device(Slave) conforms to PROFINET Conformance classes A,B and C functionality
- Supports minimum cycle time of 250 us
- Integrated two-port cut-through switch, 100 Mb/s Full Duplex
 - Relative forwarder, computes the Forward FSO for RTC3 frames which have to be forwarded
- PROFINET Quality of Service (QoS)
 - Four priority receive queues on host port, each queue 6 KB in size
 - Four priority transmit queues on each physical port, each queue 3 KB in size
- Up to 8 Application Relations (ARs)
- 8 IOCRs
 - 8 Consumer Protocol Machines (CPM)
 - 8 Provider Protocol Machines (PPM)
 - Supports PROFINET IO data size from 40 to 1440 Bytes
- Data Hold Timer
- DCP Identify Filter
 - DCP Identify frame is given to host only if it is meant for it otherwise it is just forwarded.
 - Reduces the DCP Identify frames reaching host at a particular node at network startup
- One Step Time Synchronization (PTCP)
- 1 millisecond buffering per port
- 802.1d learning bridge for received source MAC addresses
- PNIO static routing and custom FDB for multicast addresses
- Interrupt Pacing
- Media Redundancy Protocol (MRP)
 - Bump less transition of PROFINET connection to redundant path on ring break
 - Switch address learned table (FDB) is flushed in 2.4 micro second



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Description

PRU-ICSS PROFINET IRT firmware implements PROFINET IRT slave layer2 functionality and provides PROFINET IRT ASIC like functionality integrated into Sitara Processors with PRU-ICSS. PRU-ICSS PROFINET IRT Software from TI can be used by customers to add PROFINET IRT function on top of Processor SDK to Sitara processors.



PROFINET IRT firmware for PRU-ICSS is a black box product maintained by TI. PROFINET IRT driver allows loading and run PROFINET IRT firmware and interface with the firmware.

PROFINET Driver is provided in full source so that customers can adapt this implementation to own hardware and Operating Systems. This driver provides stack interface for CPM/PPM management, Triple Buffer Management, MRP, DCP Filter, Multicast Filter, Phase management and PTCP modules.

Operating System, Switch Driver (ICSS EMAC LLD), TCP/IP Stack (NDK) and associated documentation is available through Processor SDK. See Software section for details

Performance Summary

A 300 MHz CPU speed is sufficient to support a simple IO or sensor application. More complex applications can use higher speed grades of up to 1.5 GHz. The PRU core speed remains 200 MHz for all speed grades.

Memory Summary

This section describes memory usage of the PROFINET IRT PRU-ICSS firmware and Cortex-A driver.

Table 1 PROFINET IRT PRU-ICSS Firmware Memory Statistics

Memory	Program memory	Data memory	Remarks
PRU0	7.77KB	5.86 KB	
PRU1	7.80KB	5.03 KB	
PRU-ICSS SHARED RAM	NA	12 KB	Buffer descriptors, Filter tables etc
L3 OCMC RAM	NA	64 KB	Switch Buffers, PPM and CPM buffers

Table 2 PROFINET IRT Driver Memory Statistics

Section	Memory
.text (executable code)	21.55 KB
.rodata (constant data)	16.58 KB
.data (initialized non-constant data –writable static)	84 Bytes
.bss (uninitialized data)	10.1 KB

NOTE: Driver object files (iPNDrv.o, iPNoS.o, iRtcDrv.o, iRtcDrv2.o and iPtcpDrv.o) used for this analysis with gcc-arm-none-eabi-4_8-2014q3 toolchain options : -mcpu=cortex-a8 -mtune=cortex-a8 -marm -mfloat-abi=hard -mfpu=neon -O2

Hardware Requirements

- Sitara Processor with PRU-ICSS IP and PROFINET IRT support
- PROFINET IRT implementation uses following interrupts mapped to Host Interrupt Controller

Stack/application interrupts		
Firmware interrupt	Host Interrupt	Remarks
Frame Receive	PRU_ICSS_EVTOUT0	Notifies host when firmware has stored a frame in host receive queue
PPM Frame Receive	PRU_ICSS_EVTOUT1	Raised when firmware has transmitted a PPM frame
CPM Frame Receive	PRU_ICSS_EVTOUT2	On reception of CPM frame firmware raises this interrupt
DHT	PRU_ICSS_EVTOUT3	Firmware notifies DHT event and PPM list toggle event to host through this interrupt
PTCP	PRU_ICSS_EVTOUT4	Firmware notifies reception of RTSync frame
Link 0/1	PRU_ICSS_EVTOUT6	Interrupt is raised when the Link on MII0/1 port comes up or goes down

- PROFINET IRT implementation makes use of one channel of EDMA
- HW signals required to implement PROFINET IRT slave functionality is shown below, this info needs to be used in conjunction with <http://www.ti.com/tool/PINMUXTOOL>

NOTE: w.r.t prX, X is 1 or 2 (respectively PRU-ICSS1 and PRU-ICSS2 – refer to SOC TRM for availability)

Table 3 PRU-ICSS signals required for PROFINET functionality

Signal name		Description
PRU-ICSS MDIO		
prX_mdio_mdclk	Mandatory	MDIO clock
prX_mdio_data	Mandatory	MDIO data
PRU-ICSS MII PORT0 PRU-ICSS MII PORT1		
prX_mii_mt0_clk	Mandatory	MII0 and MII1 transmit clock
prX_mii_mt1_clk		
prX_mii0_txd3	Mandatory	MII0 and MII1 transmit data3
prX_mii1_txd3		
prX_mii0_txd2	Mandatory	MII0 and MII1 transmit data2
prX_mii1_txd2		
prX_mii0_txd1	Mandatory	MII0 and MII1 transmit data1
prX_mii1_txd1		
prX_mii0_txd0	Mandatory	MII0 and MII1 transmit data0
prX_mii1_txd0		
prX_mii0_rxd3	Mandatory	MII0 and MII1 receive data3
prX_mii1_rxd3		
prX_mii0_rxd2	Mandatory	MII0 and MII1 receive data2
prX_mii1_rxd2		
prX_mii0_rxd1	Mandatory	MII0 and MII1 receive data1
prX_mii1_rxd1		
prX_mii0_rxd0	Mandatory	MII0 and MII1 receive data0
prX_mii1_rxd0		
prX_mii0_txen	Mandatory	MII0 and MII1 TX enable
prX_mii1_txen		
prX_mii_mr0_clk	Mandatory	MII0 and MII1 receive clock
prX_mii_mr1_clk		
prX_mii0_rxdv	Mandatory	MII0 and MII1 RX data valid
prX_mii1_rxdv		
prX_mii0_rxer	Mandatory	MII0 and MII1 RXERR
prX_mii1_rxer		
prX_mii0_rxlink	Optional	For fast link loss detection - connect LED_LINK/LED_SPEED from PHY here and enable MLINK mode in MDIO
prX_mii1_rxlink		
PRU-ICSS PTCP Clocks (Network clock synchronization)		
prX_edc_sync0_out	Recommended (for PTCP capable slaves)	SYNC0 out - Time synchronized OUT0

Software

PROFINET IRT slave firmware, driver, examples and associated documentation for Sitara Processors is available from <http://www.ti.com/tool/PRU-ICSS-PROFINET>. PROFINET IRT software runs on top of TI Processor SDK

More details can be found here

http://processors.wiki.ti.com/index.php/Industrial_Protocol_Package_Software_Developer_Guide

http://processors.wiki.ti.com/index.php/Processor_SDK_RTOS_Software_Developer_Guide

http://processors.wiki.ti.com/index.php/Processor_SDK_Linux_Software_Developer's_Guide

Certification Information

Certification was done on [AM335x ICEv2](#) board using PROFINET IRT firmware build (00.0A.0C) and Molex PROFINET IRT stack 5.0.4.0 during June 2015.



Certificate

PROFIBUS Nutzerorganisation e.V. grants to
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the Certificate No: **Z10659** for the PROFINET IO Device:

Model Name: AM3359 Profinet Evaluation Kit
Revision: SW/FW: T 1.0.2; HW: 1
Identnumber: 0x0127; 0x0310
GSD: GSDML-V2.31-MOLEX_TI-AM335xProfinet_SDK-20150609.xml
DAP: DIM 1: Molex-TI sample device, 0x1010 0000

This certificate confirms that the product has successfully passed the certification tests with the following scope:

<input checked="" type="checkbox"/>	PNIO_Version	V2.32
<input checked="" type="checkbox"/>	Conformance Class	C Optional Features: IRT
<input checked="" type="checkbox"/>	Netload Class	III
<input checked="" type="checkbox"/>	PNIO_Tester_Version	V2.3.5
<input checked="" type="checkbox"/>	Tester	SIEMENS AG, Fürth, Germany PN346-1, IRT086-1

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(Official in Charge)

Board of PROFIBUS Nutzerorganisation e. V.



(Karsten Schneider)



(K.-P. Lindner)



References

1. PROFINET on Sitara Processors – s pry252b
2. Industrial Communications Solution Guide - slyy050b
3. [PROFINET IRT Communications Development Platform](#)
4. Certified PROFINET IRT v2.3 Device With 1-GHz ARM Application Processor - tiduak0
5. [Molex PROFINET IRT Stack](#)

Acronyms

Acronym	Description
PRUSS	Programmable RealTime Unit Sub System
PRU-ICSS	Programmable RealTime Unit - Industrial Communication Sub System - PRUSS with industrial communication support
IRT	Isochronous Real Time
PTCP	Precision Transparent Clock Protocol
DL	Datalink Layer
ISR	Interrupt Service Routine
AL	Application Layer
DCP	Discovery and basic Configuration Protocol
IOCR	IO Communication Relation
PNIO	PROFINET Input Output
FDB	Filtering Data Base
ASIC	Application Specific Integrated Circuit
EDMA	Enhanced Direct Memory Access
MDIO	Management Data Input Output
MII	Media Independent Interface
OS	Operating Systems

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