REVISIONS			
Rev	Description	Date	Approved
A	Initial Release	06/10/2011	Jason Green
B	See Revision History Rev B Description	05/04/2012	Jason Green
C	See Revision History Rev C Description	12/21/2012	Michelle Garcia
D	Refer to Revision History in **Table 1**	01/19/2015	Anshul Jain

TI Confidential – NDA Restrictions

.45 WXGA-800 DDR Series 241 DMD Customer Data Sheet

		PROGRAM MANAGER Anshul Jain	DATE 06/10/2011	.45 WXGA-800 DDR Series 241 DMD Customer Data Sheet		
		SYSTEM ELECTRICAL Paulo Pinheiro	DATE 06/10/2011			
		SYSTEM MECHANICAL John McKinley	DATE 06/10/2011			
		SYSTEM OPTICAL Mike Davis	DATE 06/10/2011			
	0314DA	CQRE Paul Konrad	DATE 06/10/2011			
NHA	USED ON	PROD INT Jason Green	DATE 06/10/2011	SIZE A	DRAWING NO 2511628	REV D
APPLICATION		ASIC Larry Dickinson	DATE 06/10/2011	SCALE NONE	Sheet 1 of 31	

Table 1. Revision History

Rev	Date	Section	Summary of Changes
A	06/10/2011	All	Initial Release
B	05/04/2012	Cover Page, Footer	Changed Propriety Information to NDA Restrictions
		Table 8	Update DCLK clock pulse width.
		Table 4 Note 10	Updated the calculation with the max lumens level.
		Table 4 Note 7 Table 5 Note 5	Changed the recommended operating temperature range to 0C-65C and moved the accompanying note.
		Table 4 Notes 6,8,9	Added Notes.
		Table 4 Note 5	Removed dew point specification and reworded statement about reliability regarding temperature and humidity.
		Table 5 Note 5	Add max lumens level
		Figure 3 Note 3	Added note on mirror parking process to go along with the graph.
		Table 11	Updated efficiency value and removed fringe specification
		Table 11 Note 2	Clarified the note.
C	12/21/2012	Footers	updated Copyright from 2011 to 2011–2012
		Sheet 2	updated Important Notice Concerning TI Semi Products.
		Table 3	added VBIAS and VRESET to Note.
		Table 4 Note 2	added VBIAS and VRESET.
		Table 4 Note 8	updated max lumens level from 150 lm to 200 lm
		Table 5 Note 3	added VBIAS and VRESET.
		Table 5	added Operating System Luminance of 200 Lumens maximum
		Table 5 Note 5	updated max lumens level from 150 lm to 200 lm
		Table 8 Note 1	clarified the slew rate effect on setup and hold time.
		Table 12	corrected table header from Table 122 to Table 12.
		Table 13	corrected table header for Package Connector Pins.
		Table 14	corrected table header for Package Test Pads.
		Table 15	changed from duplicate occurrence of Table 13 to Table 15.
D	01/19/2015	Sheet 3	Added section Chipset Component Usage Specification
		All	Update footer with revision and copyright information
		Sheet 31	Legal updates to Important Notice, then moved to last sheet

DLP® Chipset Component Usage Specification

The .45 WXGA-800 DDR Series 241 DMD is a component of one or more DLP® chipsets. Reliable function and operation of the .45 WXGA-800 DDR Series 241 DMD requires that it be used in conjunction with the other components of the applicable DLP chipset, including those components that contain or implement TI DMD control technology. TI DMD control technology is the TI technology and devices for operating or controlling a DLP DMD.

Product Description and Documentation

Table 2. Product Description

DMD Part #	Mechanical ICD	Description
*1191-403BT	2511423	0.45 inch Diagonal Spatial Light Modulator of Aluminum Micro-Mirrors. Display resolution is 1140 Columns by 912 Rows in a Diagonal Pixel Arrangement. Data is clocked into the DMD on both the Rising and Falling Edges of DCLK. This is referred to as Double Data Rate (DDR). Pixel Architecture is VSP with DarkChip3™.

Part Number Description:

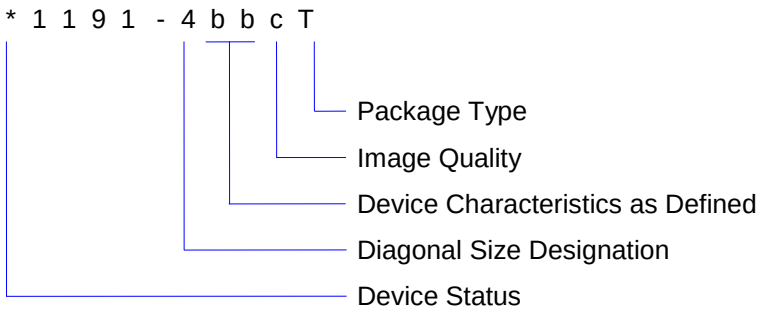

Figure 1. Part Number Description

Device Status:

A lead alpha character of “X” implies the device has been released for restricted sales only. When no lead alpha character (*) is present, the device has been released for unrestricted sales.

Table 3. Package Connector Pin Descriptions		
Pin Name	Description	Type
DATA(23:0)	• Data Bus • Synchronous to Rising Edge and Falling Edge of DCLK • Bond Pads do Not connect to internal Pull Down	LVCMOS Input
DCLK	• Data Clock • Bond Pad does Not connect to internal Pull Down	LVCMOS Input
LOADB	• Parallel Latch Load Enable • Synchronous to Rising Edge and Falling Edge of DCLK • Bond Pad does Not connect to internal Pull Down	LVCMOS Input
TRC	• Toggle Rate Control • Synchronous to Rising Edge and Falling Edge of DCLK • Bond Pad does Not connect to internal Pull Down	LVCMOS Input
SCTRL	• Serial Control (Sync) • Synchronous to Rising Edge and Falling Edge of DCLK • Bond Pad does Not connect to internal Pull Down	LVCMOS Input
DRC_BUS	• Reset Control Serial Bus • Synchronous to Rising Edge of SAC_CLK • Bond Pad does Not connect to internal Pull Down	LVCMOS Input
DRC_OEZ	• Active Low • Output Enable signal for internal Reset Driver circuitry • Bond Pads do Not connect to internal Pull Down	LVCMOS Input
DRC_STROBE	• Rising Edge on DRC_STROBE latches in the Control Signals • Synchronous to Rising Edge of SAC_CLK • Bond Pad does Not connect to internal Pull Down	LVCMOS Input
SAC_BUS	• Stepped Address Control Serial Bus • Synchronous to Rising Edge of SAC_CLK • Bond Pad does Not connect to internal Pull Down	LVCMOS Input
SAC_CLK	• Stepped Address Control Clock • Bond Pad does Not connect to internal Pull Down	LVCMOS Input
VBIAS	• Power supply for Positive Bias level of Mirror Reset signal	Power
VCC	• Power Supply for Low Voltage CMOS logic • Power Supply for Normal High Voltage at Mirror Address Electrodes • Power supply for Offset level of Mirror Reset signal during Power Down	Power
VOFFSET	• Power Supply for High Voltage CMOS logic • Power Supply for Stepped High Voltage at Mirror Address Electrodes • Power supply for Offset level of Mirror Reset signal	Power
VREF	• Power Supply for Low Voltage CMOS DDR Interface	Power
VRESET	• Power supply for Negative Reset level of Mirror Reset signal	Power
VSS	• Common Return for all Power	Power

Note: VOFFSET, VCC, VREF, VBIAS, VRESET, and VSS power supplies are required for all DMD operating modes.

Table 4. Absolute Maximum Ratings Note 1				
Parameters		Min	Max	Units
LVCMOS Logic Supply voltage: VREF	Note 2	– 0.5	4	VDC
LVCMOS Logic Supply voltage: VCC	Note 2	– 0.5	4	VDC
Mirror Electrode and HVCMOS voltage: VOFFSET	Note 2	– 0.5	8.75	VDC
Mirror Electrode Voltage: VBIAS		– 0.5	17	VDC
Supply Voltage Delta |VBIAS – VOFFSET|	Note 3		8.75	VDC
Mirror Electrode Voltage: VRESET		– 11	0.5	VDC
Input voltage: other inputs	Note 2	– 0.5	VREF + 0.5	VDC
Clock Frequency: DCLK	Note 4	80	120	MHz
Operating Temperature: • Reference Location Test Point 1 and the active array in Figure 2	Note 5,6,7,8	– 20	75	°C
Storage Temperature (non-operating): Reference Location Test Point 1 in Figure 2	Note 5, 9	– 40	85	°C
Operating Relative Humidity (non-condensing)	Note 5	0	95	%
Non-operating and Storage Relative Humidity (non-condensing)	Note 5, 9	0	95	%

Note 1: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the DMD. This is a stress rating only and functional operation of the DMD at these or any other conditions beyond those indicated in the “Recommended Operating Conditions” section of this product spec are not implied. Exposure to absolute maximum rated conditions for extend periods may affect device reliability.

Note 2: All voltage values are with respect to GND (VSS). VOFFSET, VCC, VREF, VBIAS, VRESET, and VSS power supplies are required for all DMD operating modes

Note 3: To prevent excess current, the supply voltage delta |VBIAS – VOFFSET| must be less than 8.75V

Note 4: BSA to Reset Timing specifications are synchronous and guaranteed for DCLK between 80MHz and 120MHz

Note 5: Extended exposure to high Temperature and high Relative Humidity will reduce DMD reliability.

Note 6: Exposure of the DMD simultaneously to the maximum operating conditions for Temperature and Illumination UV will reduce device lifetime.

Note 7: Operating between -20°C to 0°C, or between 65°C to 75°C, will reduce DMD lifetime; operation in these temperature ranges should be limited to <500 cumulative hours over the life of the DMD.

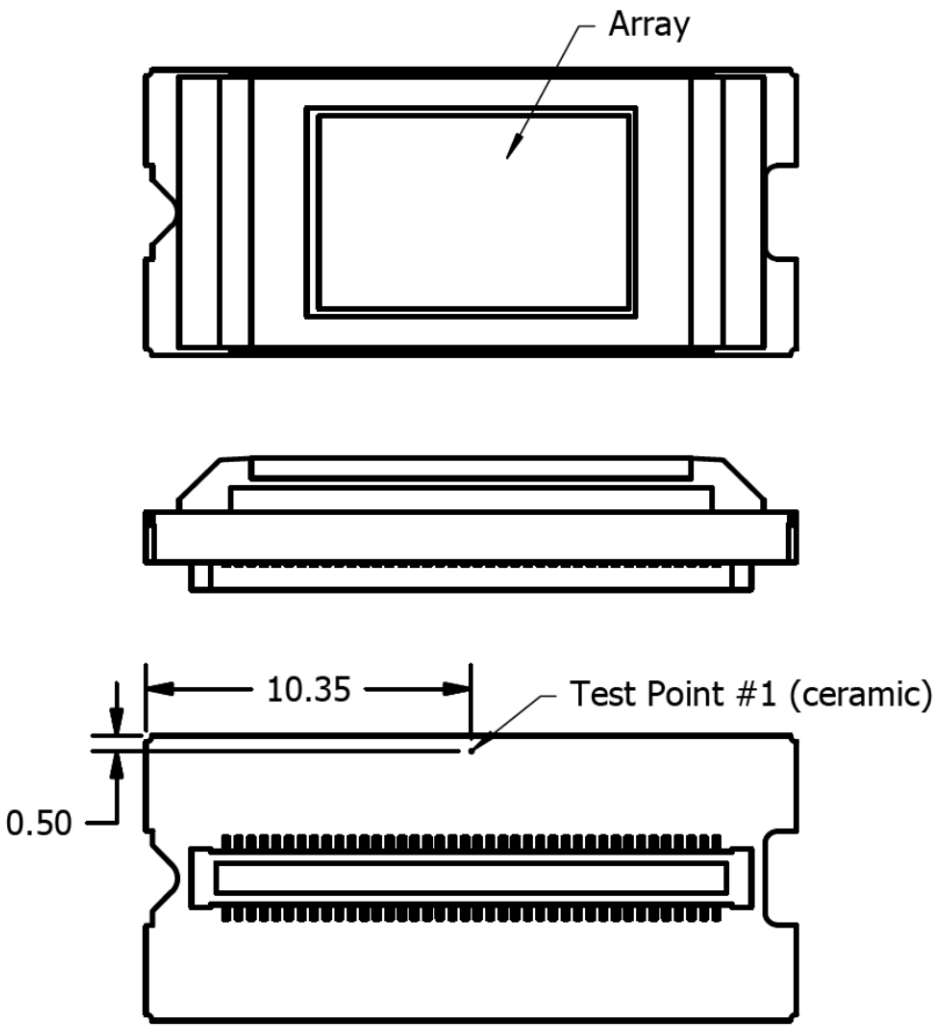

Figure 2. Thermocouple Location

Note 8:
Active Array Temperature cannot be measured directly. Therefore it must be computed analytically from measurement points on the outside of the Series 241 package, the package thermal resistance, the electrical power, and the illumination heat load. The relationship between array temperature and the reference ceramic temperature, Thermocouple Location (Test Point #1) in Figure 2, is provided by the following equations.

$T_{Array} = T_{Ceramic} + (Q_{Array} \bullet R_{Array\text{-}To\text{-}Ceramic})$

$Q_{Array} = (0.00293 \bullet SL) + (\text{Nominal Electrical Power})$

Where:

T_{Array} = computed array temperature (°C)

$T_{Ceramic}$ = measured ceramic temperature (°C) (Test Point # 1 location)

Q_{Array} = Total DMD array power (electrical + absorbed) (Watts)

$R_{Array\text{-}To\text{-}Ceramic}$ = DMD package thermal resistance from array to outside ceramic (°C/Watt) – see Table 10

SL = measured screen lumens (lumens)

The electrical power dissipation of the DMD is variable and depends on the voltages, data rates and operating frequencies. A nominal electrical power dissipation to use when calculating array temperature is 0.25 Watts. The absorbed power from the illumination source is variable and depends on the operating state of the mirrors and the intensity of the light source. The equations shown above are valid for a 1-Chip DMD system with a total projection efficiency from DMD to the screen of 87%. The constant 0.00293 is based on array characteristics. It assumes a spectral efficiency of 300 lumens/Watt for the projected light and illumination distribution of 83.7% on the active array, and 16.3% on the array border and window aperture.

Sample Calculation:

DCLK = 120MHz, VCC = 2.5V, VREF = 1.8V, VOFFSET = 8.5V, VBIAS = 16V, VRESET = –10V

Screen lumens = 200 lumens

$T_{Ceramic}$ = 55 °C

$Q_{Array} = (0.00293 \bullet 200) + 0.25 = 0.836$ Watts

T_{Array} = 55 °C + (0.836 Watts • 2.0 °C/Watt) = 56.672 °C

Note 9:
As a best practice TI recommends storing the DMD in a temperature and humidity controlled environment

Table 5. Recommended Operating Conditions						
Parameters			Min	Nom	Max	Units
VREF	LVCMOS Interface Power Supply Voltage	Note 3	1.6	1.8	2.0	V
VCC	LVCMOS Logic power supply voltage	Note 3	2.375	2.5	2.625	V
VOFFSET	Mirror Electrode and HVCMOS voltage	Note 3	8.25	8.5	8.75	V
VBIAS	Mirror Electrode Voltage		15.5	16	16.5	V
	Supply Voltage Delta |VBIAS – VOFFSET|	Note 2			8.75	V
VRESET	Mirror Electrode Voltage		– 9.5	– 10	– 10.5	V
Test Point 1, Tarray	Operating Case Temperature	Note 1,4	0		65	^{o}C
ILLuv	Illumination, wavelength < 395nm	Note 4		0.68	2.00	mW/cm^2
ILLir	Illumination, wavelength > 800nm				10	mW/cm^2
	Operating System Luminance	Note 5			200	lm
Vp	Positive Going Threshold Voltage		0.4*VREF		0.7*VREF	V
Vn	Negative Going Threshold Voltage		0.3*VREF		0.6*VREF	V
Vh	Hysteresis Voltage (Vp – Vn)		0.1*VREF		0.4*VREF	V
Vih(DC)	DC High level input voltage		0.7*VREF		VREF + 0.5	V
Vil(DC)	DC Low level input voltage		-0.3		0.3 * VREF	V
Vih(AC)	AC High level input current		0.8*VREF		VREF + 0.5	V
Vil(AC)	AC Low level input current		-0.3		0.2 * VREF	V

Note 1:
Operating case temperature limits apply to the Array and Thermocouple Location Test Point # 1, referenced in Figure 2 Extended exposure to high Temperature and high Relative Humidity will reduce DMD reliability.

Note 2:
To prevent excess current, the supply voltage delta |VBIAS – VOFFSET| must be Less than 8.75v

Note 3:
VOFFSET, VCC, VREF, VBIAS, VRESET, and VSS power supplies are required for all DMD operating modes.

Note 4:
Exposure of the DMD simultaneously to the maximum operating conditions for Temperature and Illumination UV will reduce device lifetime.

Note 5: The DMD can be used in projectors up to and including 200 lumens. It shall not be used in projectors exceeding 200 screen lumens.

Requirements for Power Up and Power Down

The DMD requires VCC, VREF, VOFFSET, VBIAS, and VRESET power supplies to the DMD. Previous DMDs using external reset waveform drivers have required VCC, VREF, and VOFFSET (sometimes referred to as VCC2) power supplies. Because the DMD generates its own reset waveforms, the additional power supplies VBIAS and VRESET must be supplied to the DMD.

These five power supplies have to be coordinated during power up/down operations. Failure to meet any of the below requirements will result in a significant reduction in the DMD's reliability / lifetime. Refer to Figure 3.

• During Power up, VCC and VREF must always start and settle before VOFFSET, VBIAS and VRESET, voltages are applied to the DMD.

• Power-Down sequence is the reverse order of the previous Power-Up sequence. VCC and VREF must be supplied until after VBIAS, VRESET and VOFFSET are discharged to within 4 V of ground.

• During Power Up, VBIAS does not have to start after VOFFSET. However, it is a Strict Requirement that the delta between VBIAS and VOFFSET must be within ± 8.75v (Note 1).

• During Power Down it is not mandatory to stop driving VBIAS prior to VOFFSET, but it is a strict requirement that the delta between VBIAS and VOFFSET must be within ± 8.75v (Note 1).

• During power-up and power-down, there is No Requirement for the relative timing of VRESET with respect to VOFFSET and VBIAS

• During power up, the DMD's LVCMOS input pins shall not be driven high until after VCC and VREF have settled at operating voltage. During power down, the DMD's LVCMOS input pins must be less than VREF + 0.3 v.

• Slew Rates for power-up and power-down are flexible, as long as the transient voltage Levels follow the requirements listed above.

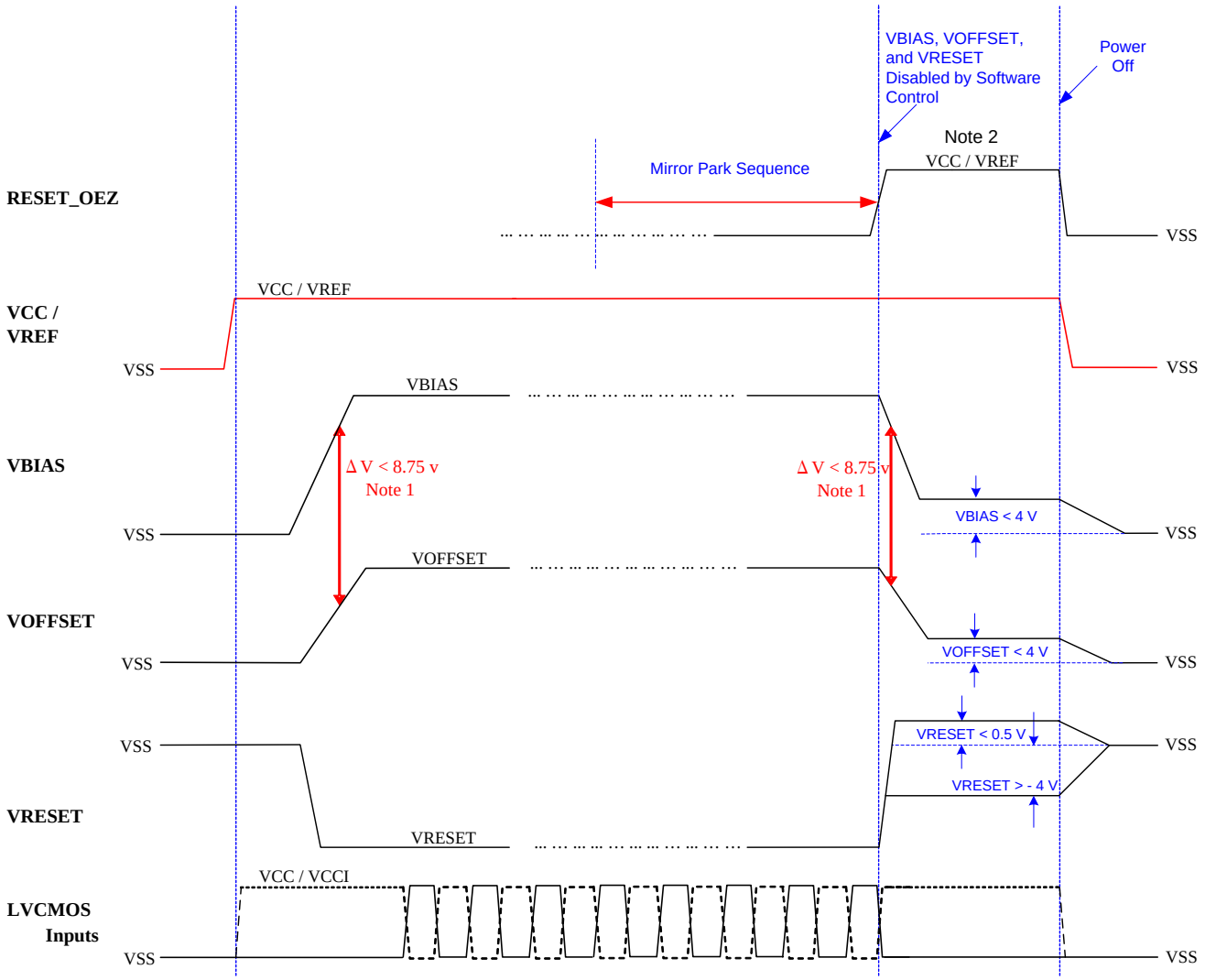

Figure 3. Power Up/Down Requirements

Note 1:
± 8.75V delta, ΔV, shall be considered the max operating delta between VBIAS and VOFFSET. It is critical to meet this requirement and that VBIAS not reach full power level until after VOFFSET is at almost full power level. OEMs may find that the most reliable way to ensure this is to delay powering VBIAS until after VOFFSET is fully powered on during power up (and to remove VBIAS prior to VOFFSET during power down). In this case, if VOFFSET is being run at its maximum allowable voltage level (8.75V), it is acceptable that the delta between VOFFSET and VBIAS may temporarily overshoot 8.75V, with the ABSOULUTE MAXIMUM delta allowed being 9V.

Note 2:
When system power is interrupted, the ASIC driver initiates a hardware power down that disables VBIAS, VRESET and VOFFSET after the mirror park sequence. Software power down disables VBIAS, VRESET and VOFFSET after the mirror park sequence through software control.

Note 3:
During the mirror parking process, VBIAS, VRESET, VOFFSET, VCC, and VSS power supplies are all required to be within spec. Once the mirrors are parked, VBIAS, VRESET, and VOFFSET may be turned off. Then, VCC and VSS power supplies may remain enabled or be turned off.

DMD Marking Location

Device Marking will include the Human-Readable character string GHJJJJK 1191-4bbcT

GHJJJJK is the Lot Trace Code

1191-4bbcT is the device part number

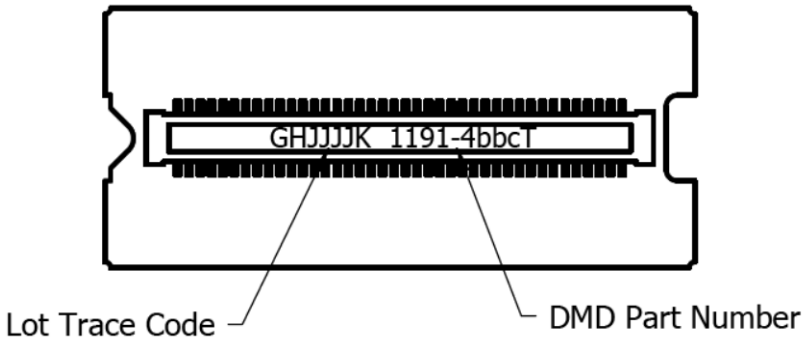

Figure 4. DMD Marking Location

Table 6. Electrical Characteristics For Recommended Operating Conditions							
Parameters		Notes	Test Conditions	Min	Nom	Max	Units
Voh	High level output voltage		VCC = 2.50 V Ioh = -21 mA	1.70			V
Vol	Low level output voltage		VCC = 2.50 V Iol = 15mA			0.40	V
Iil	Low level input current	Note 1 Note 2	VREF = 2.00 V Vi = 0.00 V	-50			nA
Iih	High level input current	Note 1 Note 2	VREF = 2.00 V Vi = VREF			50	nA
Supply Current							
Iref	Current at VREF = 2.0v		DCLK Frequency=120MHz		2.15	2.75	mA
Icc	Current at VCC = 2.75v		DCLK Frequency=120MHz		125	160	mA
Ioffset	Current at VOFFSET = 8.75v	Note 3			3	3.3	mA
Ibias	Current at VBIAS = 16.5v	Note 3 Note 4	3 Global Resets within Time Period = 200us		2.55	3.55	mA
Ireset	Current at VRESET = – 10.5v		3 Global Resets within Time Period = 200us		2.45	3.1	mA
Supply Power							
Pref	Power at VREF = 2.0v		DCLK Frequency=120MHz		3.87	5.5	mW
Pcc	Power at VCC = 2.75v		DCLK Frequency=120MHz		312.5	440	mW
Poffset	Power at VOFFSET = 8.75v				25.5	28.9	mW
Pbias	Power at VBIAS = 16.5v		3 Global Resets within Time Period = 200us		40.8	58.6	mW
Preset	Power at VRESET = – 10.5v		3 Global Resets within Time Period = 200us		24.5	32.6	mW

Note 1 :
includes LVCMOS pins only

Note 2:
LVCMOS input pins do Not have Pull-up or Pull-down configurations

Note 3:
To prevent excess current, the supply voltage delta |VBIAS – VOFFSET| must be less than 8.75v

Note 4:
When DRC_OEZ = High, the internal Reset Drivers are Tri-Stated and Ibias standby current is 6.5mA

Table 7. Capacitance at Recommended Operating Conditions					
Parameters		Test Condition	Min	Max	Units
C_I	Input Capacitance	f = 1 MHz		10	pf
C_O	Output Capacitance	f = 1 MHz		10	pf

TEXAS INSTRUMENTS
POST OFFICE BOX 655474 DALLAS, TEXAS 75265

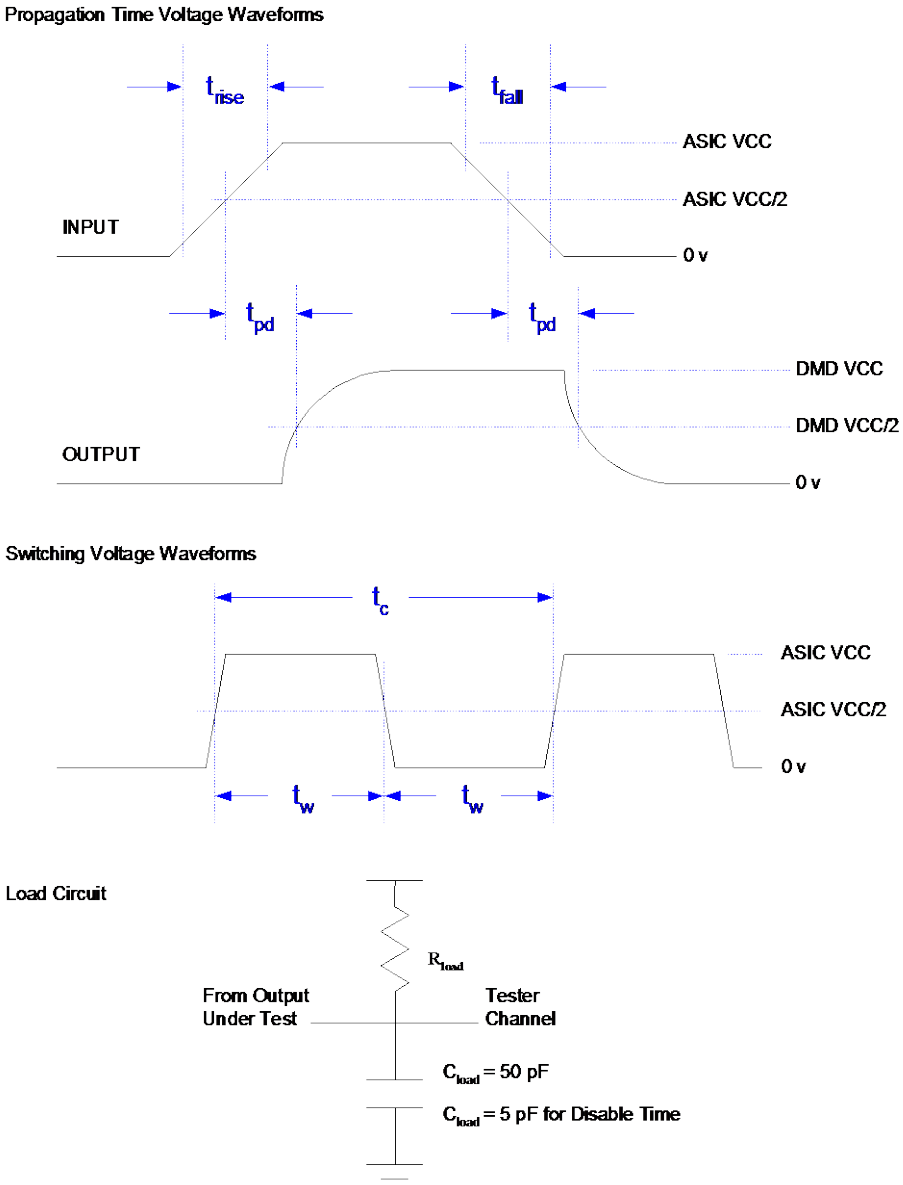

Figure 5. Measurement Conditions

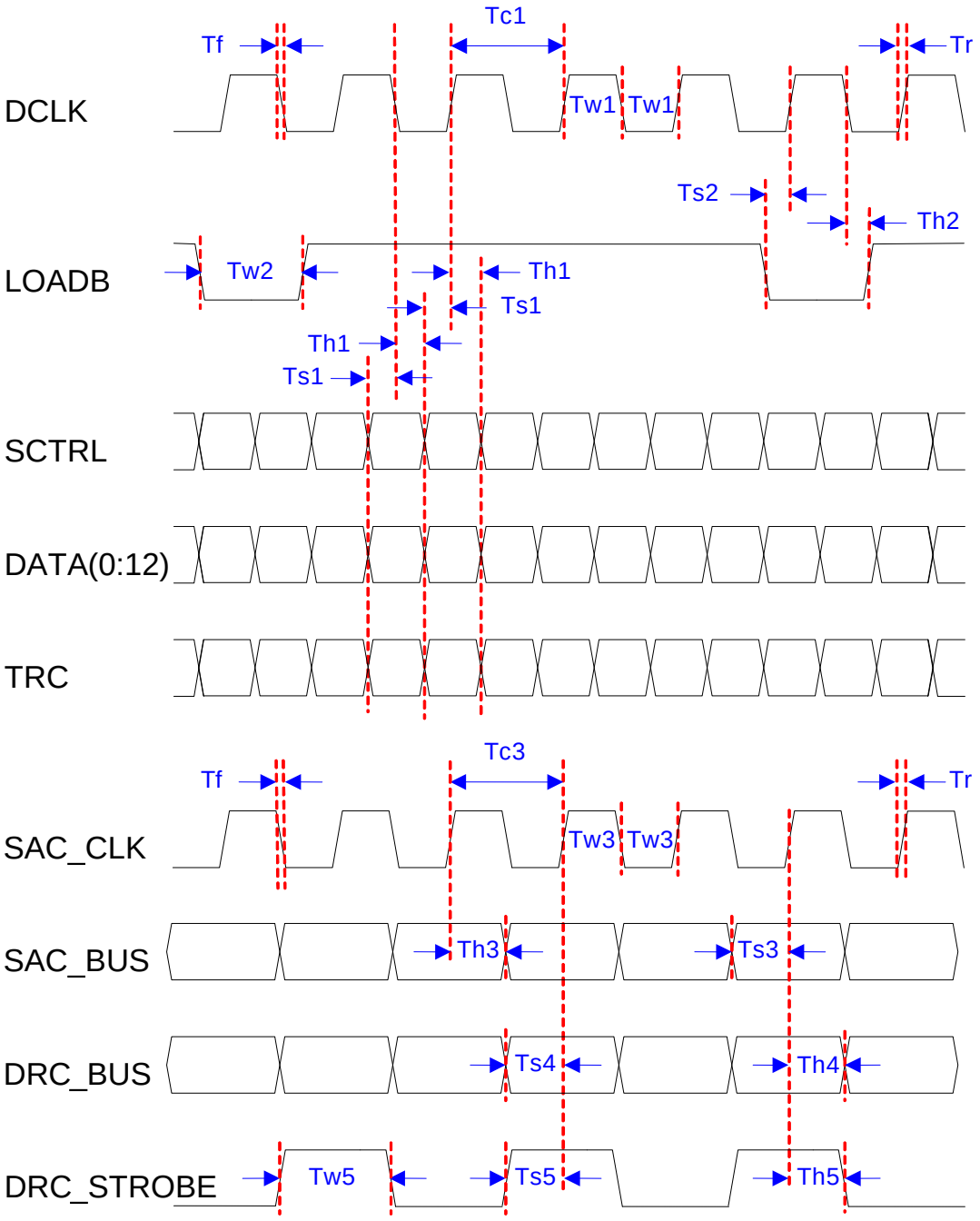

Figure 6. Critical Timing Waveforms

Table 8. Critical Timing						
Parameter		Notes	Min	Typ	Max	Units
Ts1	Setup time: DATA before rising or falling edge of DCLK	Note 1	0.7			ns
Ts1	Setup time: TRC before rising or falling edge of DCLK	Note 1	0.7			ns
Ts1	Setup time: SCTRL before rising or falling edge of DCLK	Note 1	0.7			ns
Ts2	Setup time: LOADB low before rising edge of DCLK	Note 1	0.7			ns
Ts3	Setup time: SAC_BUS low before rising edge of SAC_CLK	Note 1	1.0			ns
Ts4	Setup time: DRC_BUS high before rising edge of SAC_CLK	Note 1	1.0			ns
Ts5	Setup time: DRC_STROBE high before rising edge of SAC_CLK	Note 1	1.0			ns
Th1	Hold time: DATA after rising or falling edge of DCLK	Note 1	0.7			ns
Th1	Hold time: TRC after rising or falling edge of DCLK	Note 1	0.7			ns
Th1	Hold time: SCTRL after rising or falling edge of DCLK	Note 1	0.7			ns
Th2	Hold time: LOADB low after falling edge of DCLK	Note 1	0.7			ns
Th3	Hold time: SAC_BUS low after rising edge of SAC_CLK	Note 1	1.0			ns
Th4	Hold time: DRC_BUS after rising edge of SAC_CLK	Note 1	1.0			ns
Th5	Hold time: DRC_STROBE after rising edge of SAC_CLK	Note 1	1.0			ns
Tc1	Clock Cycle: DCLK		8.33	10.0	12.5	ns
Tc3	Clock Cycle: SAC_CLK		12.5	13.33	14.3	ns
Tw1	Pulse Width high or low: DCLK		3.33			ns
Tw2	Pulse Width low: LOADB		4.73			ns
Tw3	Pulse Width high or low: SAC_CLK		5			ns
Tw5	Pulse Width high: DRC_STROBE		7			ns
	Fast Input slew rate	Note 2	1.0			V/ns
	Slow Input slew rate	Note 2	0.5		1.0	V/ns
tr	Rise time (20% – 80%): DCLK / SAC_CLK	Note 3			1.08	ns
tr	Rise time (20% – 80%): DATA / TRC / SCTRL / LOADB	Note 3			1.08	ns
tf	Fall time (20% – 80%): DCLK / SAC_CLK	Note 3			1.08	ns
tf	Fall time (20% – 80%): DATA / TRC / SCTRL / LOADB				1.08	ns

Note 1:
Assumes fast input slew rate > 1.0 V/ns. For slower slew rates (0.5 V/ns < slew rate < 1.0 V/ns) the setup and hold times will be longer. 150 picoseconds should be added on setup and hold for every 0.10 V/ns decrease in slew rate (from 1.0 V/ns). The numbers are assuming all the slew rates for all the inputs and the clock are the same.

Note 2: Fast/slow slew rates affect setup and hold times. See note 1.

Note 3: Assumes VREF = 1.8 V

Table 9. Physical Parameters					
Parameter		Min	Nom	Max	Units
Number of Columns	Figure 7		1140		
Number of Rows	Figure 7		912		
Mirror (Pixel) Pitch Diagonal Horizontal and Vertical	Figure 8		 7.637 10.8		um
Total Height of Active Mirror Array • 1140 pixels			 6.1614		mm
Total Width of Active Mirror Array • 912 pixels			 9.855		mm
Active Array Border	Note 1		POM		
Active Array Border Size			10		mirrors/side

Note 1:
The structure and qualities of the border around the active array includes a band of partially functional mirrors called the “pond of mirrors” (POM). These mirrors are structurally and/or electrically prevented from tilting toward the bright or “on” state but still require an electrical bias to tilt toward “off.”

Out of the 10 POM Rows on the Top and Bottom, only the 1 POM Row closest to the Active Array is Electrically attached to that Reset group. The other 9 POM Rows are attached to a dedicated POM Internal Reset Driver circuit.

Table 10. Thermal Parameters					
Parameter		Min	Nom	Max	Unit
Thermal Resistance • Active area to case	Note 1			 2.0	 °C/W

Note 1:
The total heat load on the DMD is largely driven by the incident light absorbed by the active area; although other contributions include light energy absorbed by the window aperture and electrical power dissipation of the array.

Optical systems should be designed to minimize the light energy falling outside the window clear aperture since any additional thermal load in this area can significantly degrade the reliability of the device.

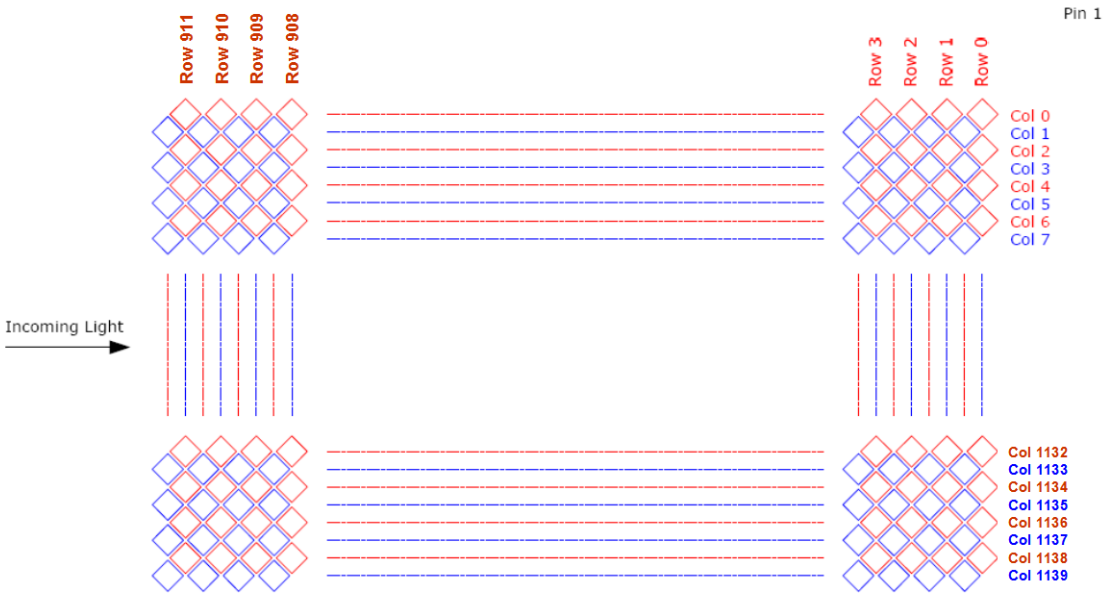

Figure 7. Diagonal Pixel Arrangement

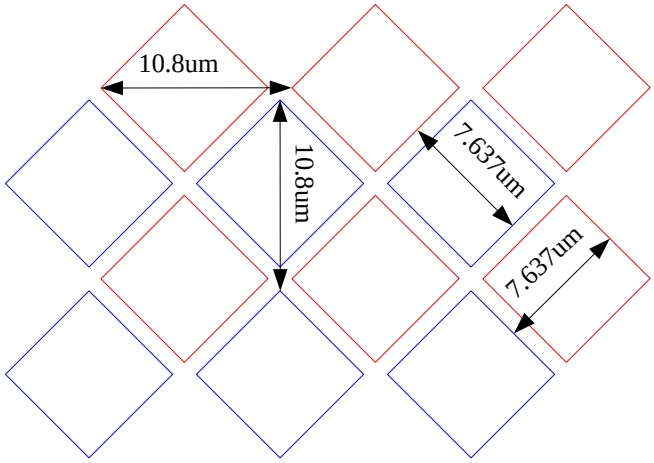

Figure 8. Pixel Pitch Dimensions

Table 11. Optical Parameters					
Parameter		Min	Nom	Max	Unit
Mirror Tilt – half angle • Variation device to device	Note 1	11	12	13	Degrees
Axis of Rotation with respect to System Datums • Variation device to device	Figure 9	89	90	91	Degrees
Mirror Metal Specular Reflectivity (420 nm – 700 nm)			89.4		%
DMD Efficiency (420 nm – 700 nm)	Note 2		66		%
Window Material Designation			Corning Eagle XG		
Window Refractive Index at wavelength 546.1 nm			1.5119		
Window Transmittance, minimum within the wavelength range 420-680 nm. Applies to all angles 0-30° AOI.	Note 3	97	99		%
Window Transmittance, average over the wavelength range 420-680 nm. Applies to all angles 30-45° AOI.	Note 3	97			%

Note 1: Mirror Tilt
Limits on variability of mirror tilt half angle are critical in the design of the accompanying optical system. Variations in tilt angle within a device may result in apparent non-uniformities, such as line pairing and image mottling, across the projected image. Variations in the average tilt angle between devices may result in colorimetry, brightness, and system contrast variations. The specified limits represent the tolerances of the tilt angles within a device.

Note 2: DMD Efficiency
Efficiency numbers assume 24-degree illumination angle, F/2.4 illumination and collection cones, uniform source spectrum, and uniform pupil illumination. Efficiency numbers assume 100% electronic mirror duty cycle and do not include optical overfill loss. The efficiency is a photopically-weighted number corresponding to 12 dgree tilt angle. Note that this number is specified under conditions described above and deviations from the specified conditions could result in decreased efficiency.

Note 3: Window Transmittance
Single-pass through both surfaces and glass.

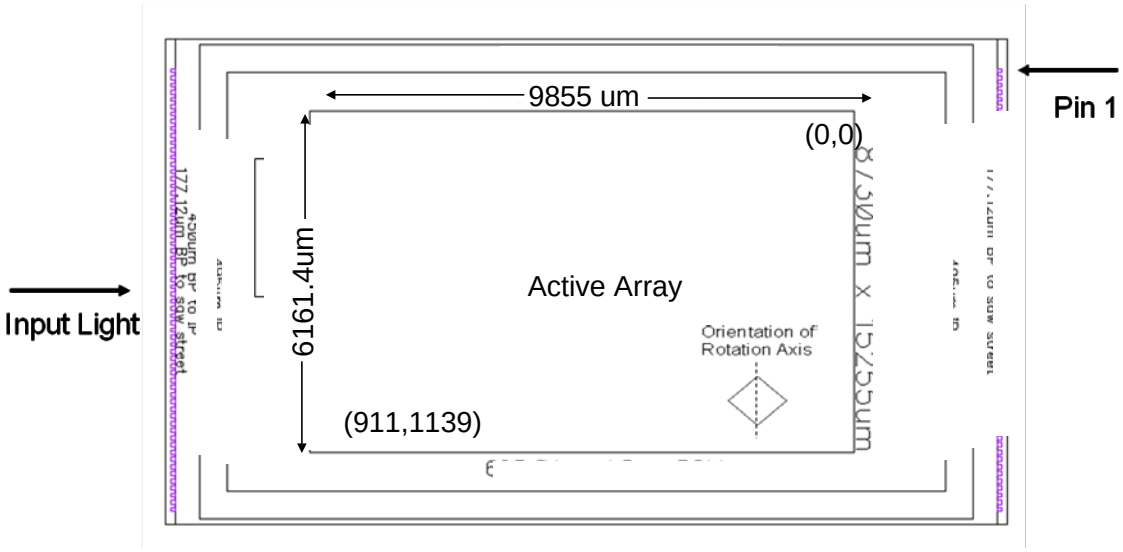

Figure 9. Array Dimensions and Mirror Tilt Axis Orientation

Note 1:
Optimizing system optical performance and image quality strongly relates to optical system design parameter trades. Although it is not possible to anticipate every conceivable application, projector image quality and optical performance is contingent on compliance to the optical system operating conditions described in a) through c) below:

a) Numerical Aperture and Stray Light Control.
The angle defined by the numerical aperture of the illumination and projection optics at the DMD optical area should be the same. This angle should not exceed the nominal device mirror tilt angle unless appropriate apertures are added in the illumination and/or projection pupils to block out flat-state and stray light from the projection lens. The mirror tilt angle defines DMD capability to separate the "ON" optical path from any other light path, including undesirable flat-state specular reflections from the DMD window, DMD border structures, or other system surfaces near the DMD such as prism or lens surfaces. If the numerical aperture exceeds the mirror tilt angle, or if the projection numerical aperture angle is more than two degrees larger than the illumination numerical aperture angle, objectionable artifacts in the display's border and/or active area could occur.

b) Pupil Match.
TI's optical and image quality specifications assume that the exit pupil of the illumination optics is nominally centered within two degrees of the entrance pupil of the projection optics. Misalignment of pupils can create objectionable artifacts in the display's border and/or active area, which may require additional system apertures to control, especially if the numerical aperture of the system exceeds the pixel tilt angle.

c) Illumination Overfill.
The active area of the device is surrounded by an aperture on the inside DMD window surface that masks structures of the DMD chip assembly from normal view, and is sized to anticipate several optical operating conditions. Overfill light illuminating the area outside the active array can create artifacts from the mechanical features that surround the active array and other surface anomalies that may be visible on the screen. The illumination optical system should be designed to limit light flux incident anywhere outside the active array more than 20 pixels from the edge of the active array on all sides. Depending on the particular system's optical architecture and assembly tolerances, this amount of overfill light on the outside of the active array may still cause artifacts to still be visible.

TI ASSUMES NO RESPONSIBILITY FOR IMAGE QUALITY ARTIFACTS OR DMD FAILURES CAUSED BY OPTICAL SYSTEM OPERATING CONDITIONS EXCEEDING LIMITS DESCRIBED ABOVE.

Mechanical dimensions and tolerances are shown in the Mechanical ICD drawing referenced in Table 2. Mechanical loads applied to the array side of the DMD should be evenly distributed to the 3 Datum 'A' areas and the Datum 'E' area.

Table 12. System Interface Parameters					
Parameter		Min	Nom	Max	Unit
Maximum Load to be Applied to the • Connector Area • DMD Mounting Area (combined load uniformly applied to 4 areas)	Figure 10			110 110	Newtons Newtons

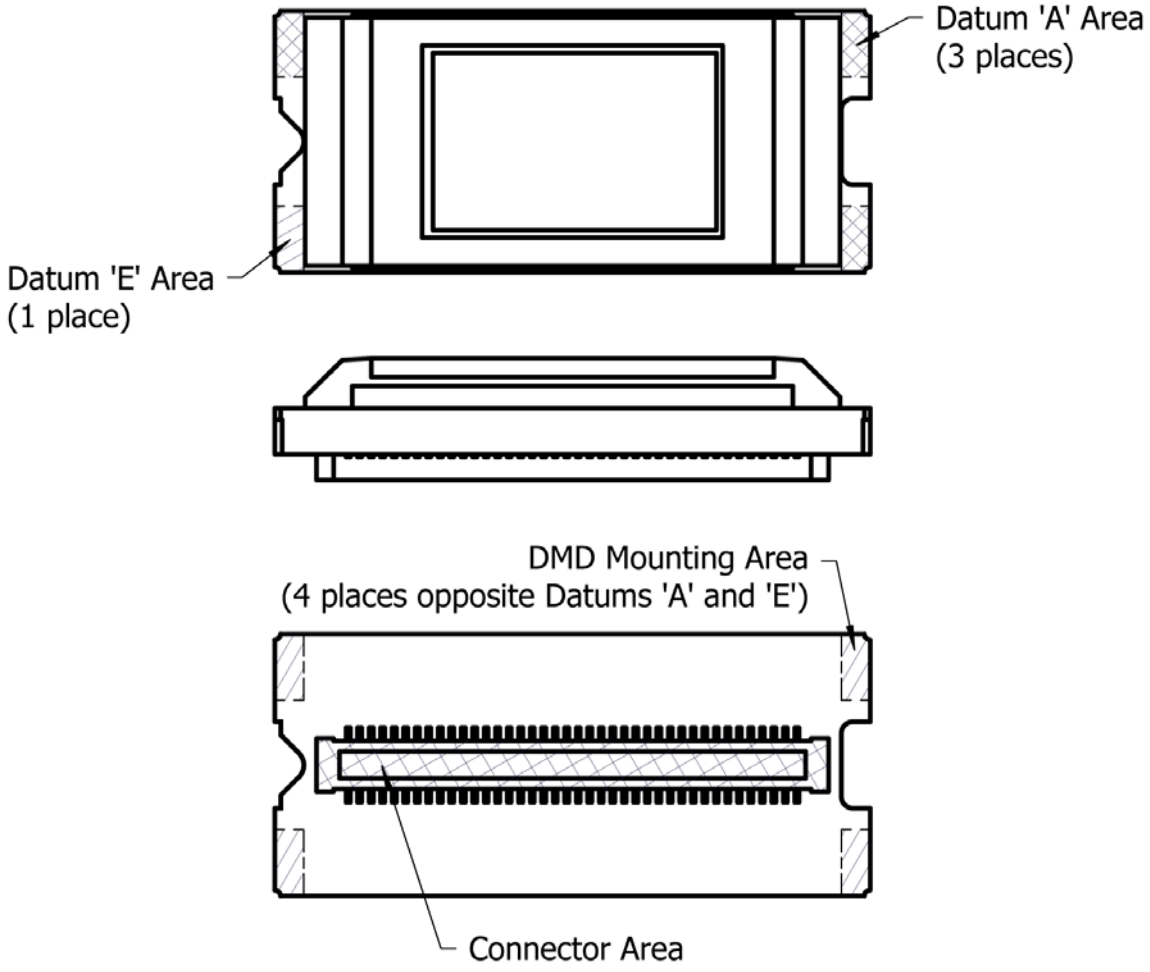

Figure 10 System Interface Loads

Table 13. Package Connector Pins	
Connector Pin	Pin Name
C1	VCC
C2	VCC
C3	D<6>
C4	D<4>
C5	VSS
C6	D<5>
C7	D<3>
C8	VSS
C9	D<2>
C10	D<1>
C11	VSS
C12	D<0>
C13	D<7>
C14	VSS
C15	D<8>
C16	D<9>
C17	VSS
C18	D<10>
C19	D<11>
C20	VSS
C21	D<12>
C22	D<13>
C23	VSS
C24	VSS
C25	VREF
C26	VREF
C27	VSS
C28	VSS
C29	DRC_BUS
C30	VSS
C31	VBIAS
C32	VBIAS
C33	DRC _OEZ
C34	VCC
C35	VCC
C36	DRC _STROBE
C37	VCC
C38	VCC
C39	VCC
C40	VCC
D1	VCC
D2	VCC
D3	TRC
D4	D<17>
D5	VSS

Table 13. Package Connector Pins	
Connector Pin	Pin Name
D6	D<20>
D7	D<22>
D8	VSS
D9	D<18>
D10	D<19>
D11	VSS
D12	LOADB
D13	DCLK
D14	VSS
D15	D<23>
D16	D<21>
D17	VSS
D18	SCTRL
D19	D<16>
D20	VSS
D21	D<15>
D22	D<14>
D23	VSS
D24	VSS
D25	VOFFSET
D26	VOFFSET
D27	VSS
D28	VSS
D29	SAC_CLK
D30	VSS
D31	VRESET
D32	VRESET
D33	SAC_BUS
D34	VCC
D35	VCC
D36	SCAN_TEST
D37	VCC
D38	VCC
D39	VCC
D40	VCC

Table 14. Package Test Pads	
Electrical Test Pad	DLP® System Board
A1	Do Not Connect
A2	Do Not Connect
A3	Do Not Connect
A4	Do Not Connect
A5	Do Not Connect
A6	Do Not Connect
A7	Do Not Connect
A8	Do Not Connect
A9	Do Not Connect
A10	Do Not Connect
A11	Do Not Connect
A12	Do Not Connect
A13	Do Not Connect
A14	Do Not Connect
A15	Do Not Connect
A16	Do Not Connect
A17	Do Not Connect
A18	Do Not Connect
A19	Do Not Connect
A20	Do Not Connect
A21	Do Not Connect
A22	Do Not Connect
A23	Do Not Connect
A24	Do Not Connect
A25	Do Not Connect
B1	Do Not Connect
B2	Do Not Connect
B3	Do Not Connect
B4	Do Not Connect
B5	Do Not Connect
B6	Do Not Connect
B7	Do Not Connect
B8	Do Not Connect
B9	Do Not Connect
B10	Do Not Connect
B11	Do Not Connect
B12	Do Not Connect
B13	Do Not Connect
B14	Do Not Connect
B15	Do Not Connect
B16	Do Not Connect

Table 14. Package Test Pads	
Electrical Test Pad	DLP® System Board
B17	Do Not Connect
B18	Do Not Connect
B19	Do Not Connect
B20	Do Not Connect
B21	Do Not Connect
B22	Do Not Connect
B23	Do Not Connect
B24	Do Not Connect
B25	Do Not Connect
E1	Do Not Connect
E2	Do Not Connect
E3	Do Not Connect
E4	Do Not Connect
E5	Do Not Connect
E6	Do Not Connect
E7	Do Not Connect
E8	Do Not Connect
E9	Do Not Connect
E10	Do Not Connect
E11	Do Not Connect
E12	Do Not Connect
E13	Do Not Connect
E14	Do Not Connect
E15	Do Not Connect
E16	Do Not Connect
E17	Do Not Connect
E18	Do Not Connect
E19	Do Not Connect
E20	Do Not Connect
E21	Do Not Connect
E22	Do Not Connect
E23	Do Not Connect
E24	Do Not Connect
E25	Do Not Connect
F1	Do Not Connect
F2	Do Not Connect
F3	Do Not Connect
F4	Do Not Connect
F5	Do Not Connect
F6	Do Not Connect
F7	Do Not Connect
F8	Do Not Connect

Table 14. Package Test Pads	
Electrical Test Pad	DLP® System Board
F9	Do Not Connect
F10	Do Not Connect
F11	Do Not Connect
F12	Do Not Connect
F13	Do Not Connect
F14	Do Not Connect
F15	Do Not Connect
F16	Do Not Connect
F17	Do Not Connect
F18	Do Not Connect
F19	Do Not Connect
F20	Do Not Connect
F21	Do Not Connect
F22	Do Not Connect
F23	Do Not Connect
F24	Do Not Connect
F25	Do Not Connect

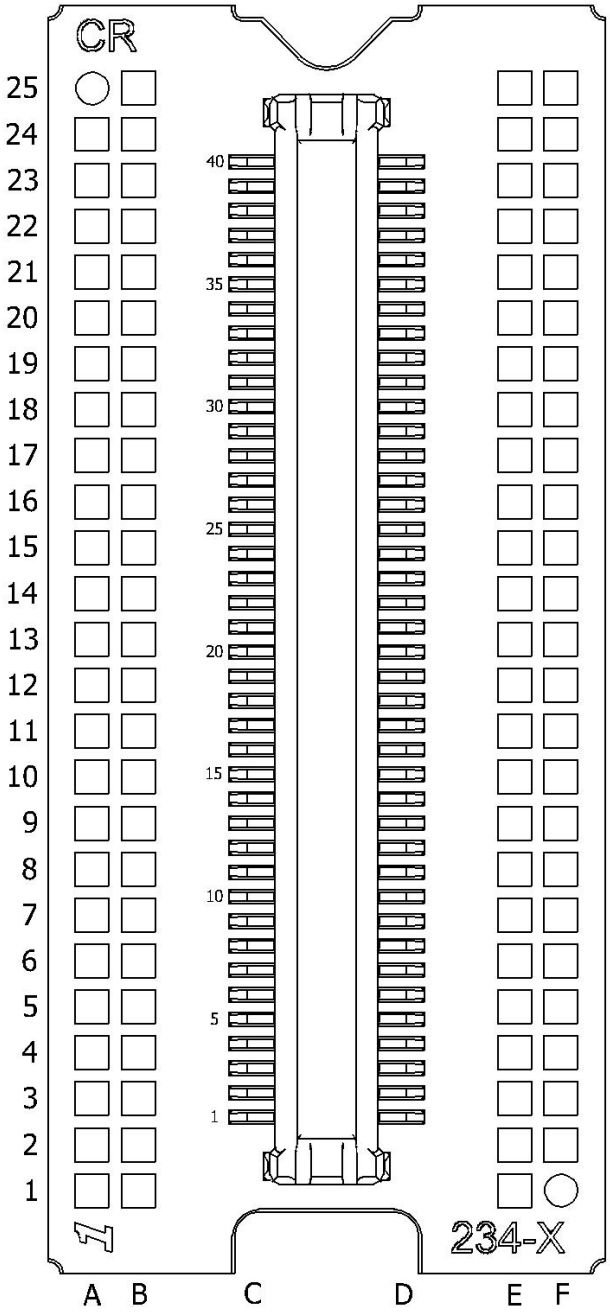

Figure 11. Package Connector Pins & LGA Test Pads - Bottom View

Electrostatic Discharge Immunity

All external signals on the DMD are protected from damage by electrostatic discharge, and are tested in accordance with JESD22-A114-B Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM).

Table 15. DMD ESD Protection Limits

Package Pin Type	Voltage (maximum)	Units
Input	2000	V
Output	2000	V
Power	2000	V

Notes on Handling:

All CMOS devices require proper Electrostatic Discharge (ESD) handling procedures.

Refer to drawing 2509743 DMD Handling Specification for Series 2xx, for precautions to protect the DMD from ESD and to protect the DMD's glass and electrical contacts.

Refer to drawing 2504640 DMD Glass Cleaning Procedure for correct and consistent methods for cleaning the glass of the DMD, in such a way that the anti reflective coatings on the glass surface are not damaged.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265