TEXAS INSTRUMENTS

Modeling the ADS6XXX family of LVDS buffer through IBIS

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Method of modeling the LVDS buffer through IBIS

Since the LVDS buffer has differential inputs and differential outputs, some additional considerations are involved while modeling it through IBIS.

ADS6XXX LVDS buffer architecture

The structure of the LVDS buffer in ADS6XXX is shown in Figure 1. HI and LO refer to the differential input to the buffer. Voltage levels of 0 Volts and 1.8 Volts correspond to logic levels of '0' and '1' at HI and LO. LOUTP and LOUTM are the differential output of the buffer. The buffer consists of two current sources (one NMOS and one PMOS) and a set of four switches to change the direction of the current flowing into the external load.

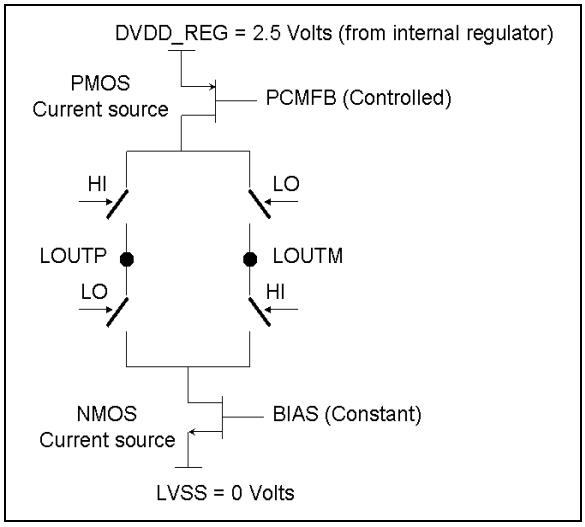

Figure 1. LVDS buffer architecture

While the NMOS current source is a constant current source (its value set by one of the eight current mode settings), the PMOS current source is controlled through a feedback loop as shown in Figure 2.

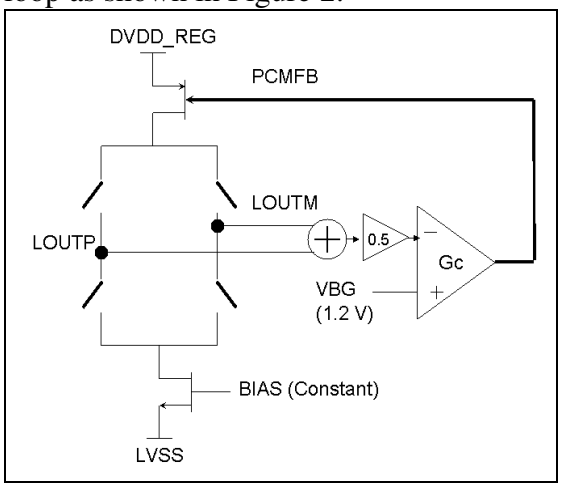

Figure 2. Controlling the PMOS current source

The PMOS current source is controlled so as to maintain the output common mode voltage of the buffer equal to a reference voltage of 1.2 Volts.

Pulldown and Pullup V-I tables

Since the LVDS buffer does not have a tristate, the power and ground clamp data are merged into the pullup and pulldown tables. The switches are controlled using HI and LO and the voltage at LOUTP is swept from –VDD to 2*VDD. The setup for the pulldown data is as shown in Figure 3. A 50 Ohm resistor connects LOUTM to the common mode voltage of VBG=1.2 Volts.

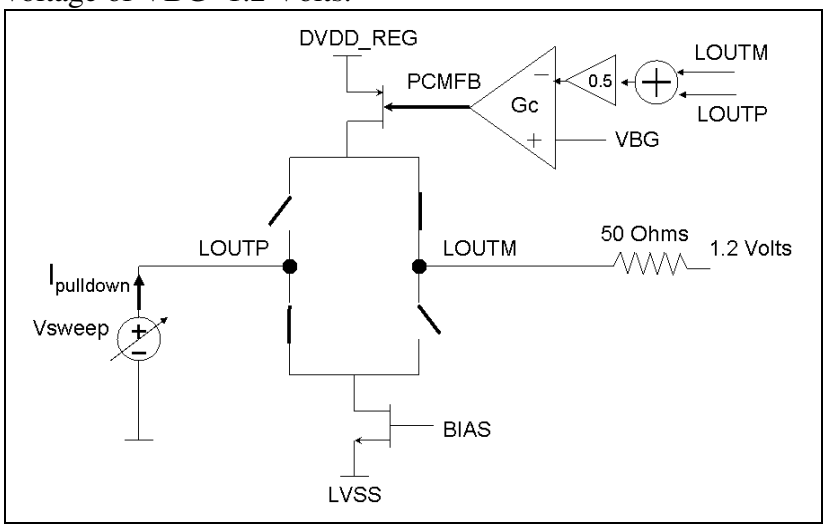

Figure 3. Voltage sweep for Pulldown table

Since the NMOS current source is a constant current source, the pulldown current is fairly a constant for an output voltage between 0.5 V to 1.9 V.

The pullup data is generated by the method shown in Figure 4. In this case however, because of the P-side current source being a controlled current source, the pullup current source varies *even* around an output voltage of 1.2 Volts.

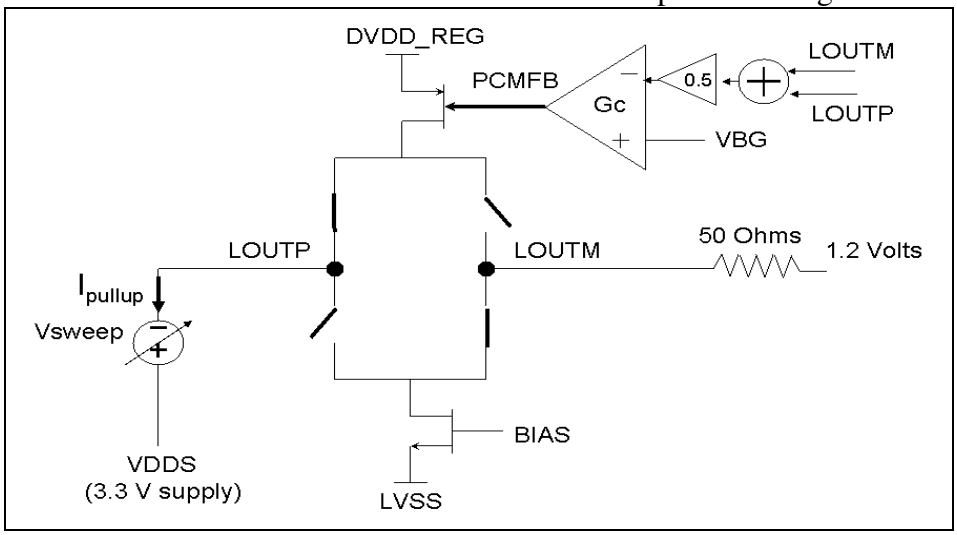

Figure 4. Voltage sweep for Pullup table

Generating the V-t table

The V-t tables are generated using the setup shown in Figure 5.

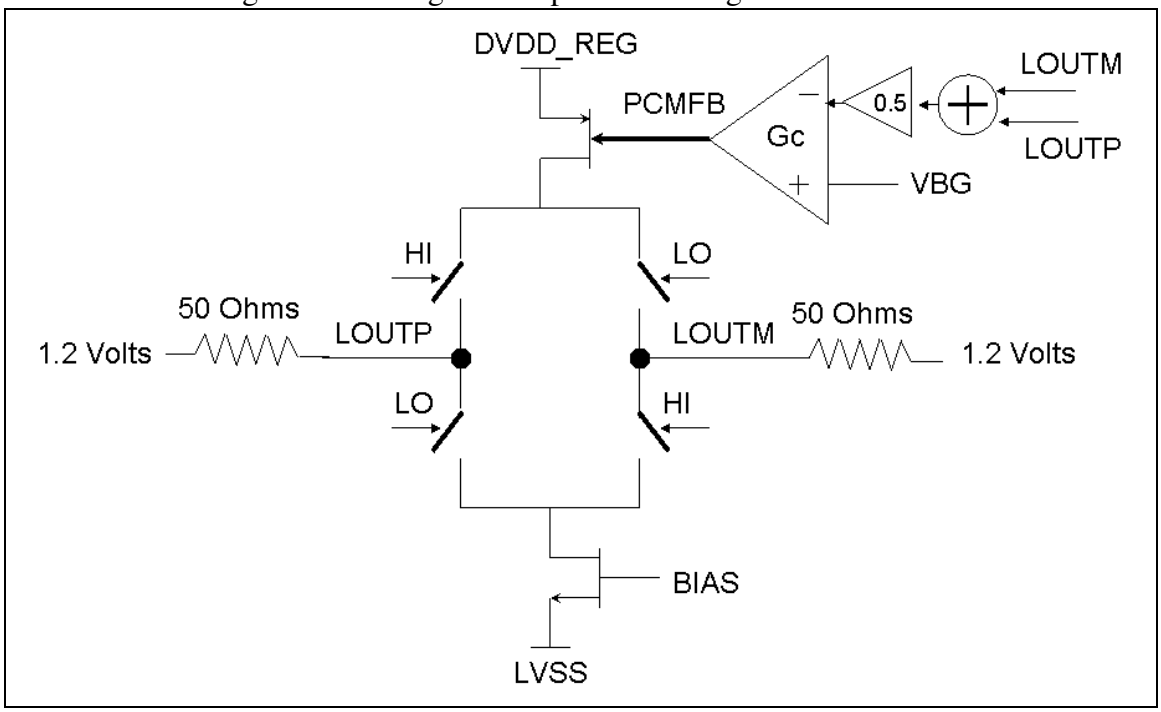

Figure 5. Generation of V-t table

Comparison of IBIS model with the actual circuit

The IBIS models were generated and compared with the actual circuit through SPICE simulations. Figure 6 shows the simulation environment for the actual LVDS buffer, while Figure 7 shows the identical environment used for the IBIS model.

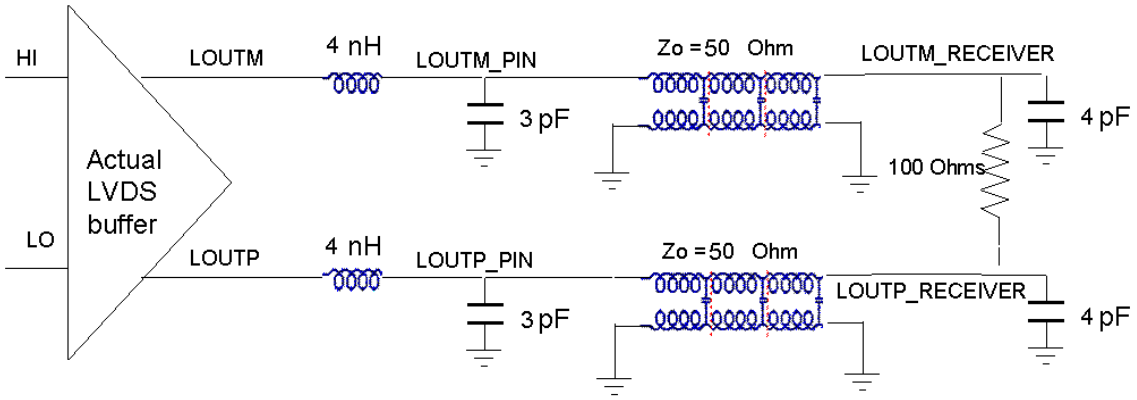

Figure 6. Simulation environment for the actual LVDS buffer

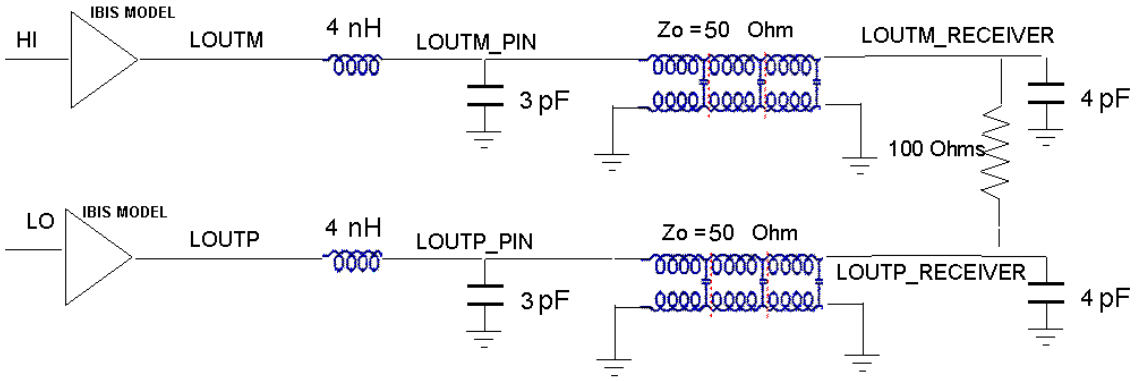

Figure 7. Simulation environment for the IBIS model of the LVDS buffer

Simulations were done with different values of the delay for the transmission line.

Figure 8 shows a comparison of the SPICE simulation results obtained from the IBIS model with those from the actual circuit. The delay of the transmission line was set to 1.50ns. No load termination was used. There are 3 sets of waveforms

1. LOUTP and LOUTM : waveforms at the buffer output
2. LOUTP_RX and LOUTM_RX : Waveform at the receiver end.
3. LOUTP_RX - LOUTM_RX : Differential voltage at the reciever end

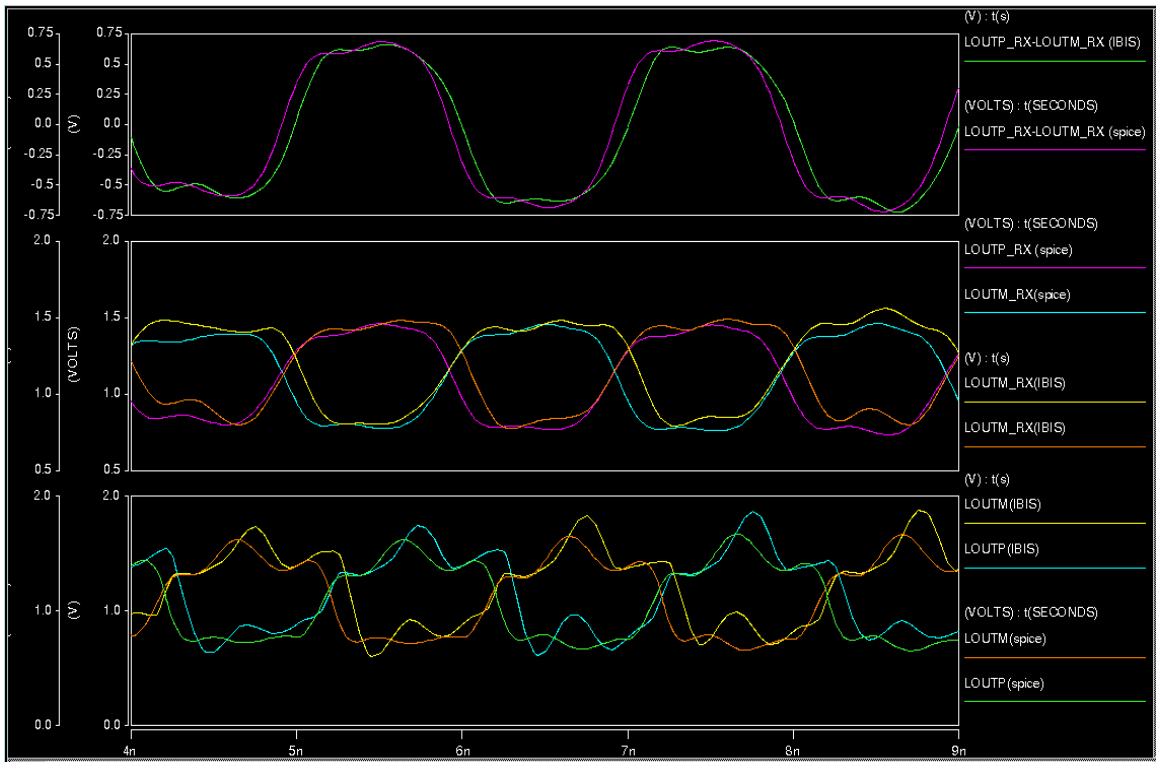

Figure 8. Comparison of results between full-transistor spice simulation and simulation using IBIS model for buffer.

Waveforms are plotted at the nodes :
LOUTP , LOUTM : Output pins of the buffer
LOUTP_RX , LOUTM_RX : The nodes at the receiver end of transmission line across which 100Ω load is connected

As can be observed, there is a close match between the actual circuit and its IBIS model.

MODEL SUMMARY

Component name - ADS6XXX
Model type - Output buffer
Filename - ads6xxx.ibs

Modeling conditions:

Condition	typ/ min/ max
AVDD	3.3 V/ 3.0 V/ 3.6 V
VBG (Common mode reference)	1.2 V/ 1.1 V/ 1.3 V
Junction temperature (Tj)	25/ 125/ -40 (degree C)
Process setting	nominal/ weak/ strong

Package Characteristics:

Characteristics	typ/ min/ max
R_pkg:	0.61Ω/0.53Ω/0.78Ω
L_pkg	2.1nH/1.78 nH /2.77 nH
C_pkg	0.18pF / 0.12 pF /0.27 pF

Please Note: Models for the buffer have been generated at various differential load terminations like 100, 75 and 50 ohms. Please refer to [Notes] keyword in the model file for details of the termination used for creating the model.

Quality Verification:

The created IBIS models are verified as follows:

1. Visual check of each characteristics using the s2iplt tool
2. Syntax check by IBISCHK4
3. Behavior of IBIS models and actual circuit compared using SPICE

Simulation using IBIS models for the buffer and load termination

For each of the 8 different current modes there are different models of the buffer.

MODEL NAME	CURRENT MODE
OLVDS_IBIS_MODE010	2.5mA
OLVDS_IBIS_MODE011	3.0mA
OLVDS_IBIS_MODE000	3.5mA
OLVDS_IBIS_MODE001	4.0mA
OLVDS_IBIS_MODE110	5.0mA
OLVDS_IBIS_MODE111	6.0mA
OLVDS_IBIS_MODE100	7.0mA
OLVDS_IBIS_MODE101	8.0mA

There are 5 internal load termination resistances which can be turned on or off. To model their effect the [series Current] keyword is used in the IBIS model them. There are 5 models by names RES_166, RES_200, RES_250, RES_333, RES_500.

Depending on the current mode and load terminations used in simulation model names for the buffer and termination resistances have to be specified against the parameter “MODEL” in the buffer statement in the netlist.

Sample instantiation of the IBIS models for the buffer in HSPICE:

```
BOUTPUTP PU 0 LOUTP INP
+FILE = 'ads6xxx.ibs' MODEL = 'OLVDS_IBIS_MODE111'
+TYP = MIN POWER=OFF
+BUFFER = OUTPUT
+RAMP_RWF = 1
+RAMP_FWF = 1
+INTERPOL = 1

BOUTPUTM PU 0 LOUTM INM
+FILE = 'ads6xxx.ibs' MODEL = 'OLVDS_IBIS_MODE111'
+TYP = MIN POWER=OFF
+BUFFER = OUTPUT
+RAMP_RWF = 1
+RAMP_FWF = 1
+INTERPOL = 1
```

Sample instantiation of the load termination of 200ohm in HSPICE

```
BSERIES200 LOUTP LOUTM
+FILE = 'ads6xxx.ibs' MODEL = 'RES_200'
+TYP = MIN
+BUFFER = SERIES_SWITCH
+SS_STATE = ON
```

```
+INTERPOL = 1
```

Sample SPICE deck for simulation of buffer with internal load termination

The following SPICE deck consists of 2 instances: BOUTPUTP BOUTPUTM of the buffer model 'OLVDS_IBIS_MODE111' to represent the LVDS buffer with 6.0mA current drive and 2 instances name BSERIES200 and BSERIES275 to represent 2 internal terminations turned on. The deck works with HSPICE version 2005.03 . If your HSPICE version doesn't support [series Current] keyword in IBIS model an alternative is to modify the deck by replacing the elements having name BSERIES200 and BSERIES275, with resistors of corresponding value.

```
.TEMP 125
* INPUT TO THE BUFFER
VINM INM 0 PULSE (0 1.65 0N 0.2N 0.2N .8N 2N)
VINP INP 0 PULSE (1.65 0 0N 0.2N 0.2N .8N 2N)
************************************************
*     2 instances of Buffer model to represent lvds buffer        *
************************************************
BOUTPUTP PU 0 LOUTP INP
+FILE = 'ads6xxx.ibs' MODEL = 'OLVDS_IBIS_MODE111'
+TYP = MIN POWER=ON
+BUFFER = OUTPUT
+RAMP_RWF = 1
+RAMP_FWF = 1
+INTERPOL = 1
BOUTPUTM PU 0 LOUTM INM
+FILE = 'ads6xxx.ibs' MODEL = 'OLVDS_IBIS_MODE111'
+TYP = MIN POWER=ON
+BUFFER = OUTPUT
+RAMP_RWF = 1
+RAMP_FWF = 1
+INTERPOL = 1
********************************************************
*INTERNAL LOAD TERMINATION OF 200 OHM and 250 OHM *
********************************************************
BSERIES200 LOUTP LOUTM
+FILE = 'ads6xxx.ibs' MODEL = 'RES_200'
+TYP = MIN
+BUFFER = SERIES_SWITCH
+SS_STATE = ON
+INTERPOL = 1

BSERIES250 LOUTP LOUTM
+FILE = 'ads6xxx.ibs' MODEL = 'RES_250'
```

```
+TYP = MIN
+BUFFER = SERIES_SWITCH
+SS_STATE = ON
+INTERPOL = 1

* PIN INDUCTANCE
LOUTP LOUTP_EXT LOUTP 4N
LOUTM LOUTM_EXT LOUTM 4N
* PIN CAPACITANCE
COUTP LOUTP_EXT 0 3PF
COUTM LOUTM_EXT 0 3PF

* TRANSMISSION LINE LOAD
TDATALINKP LOUTP_EXT 0 LOUTP_RX 0 Z0=50 TD=1.5N
TDATALINKM LOUTM_EXT 0 LOUTM_RX 0 Z0=50 TD=1.5N

* LVDS TERMINATION AT RECEIVER END
RLOAD LOUTP_RX LOUTM_RX 100

* CAPACITANCE AT RECEIVER END
COUTP_RX LOUTP_RX 0 4PF
COUTM_RX LOUTM_RX 0 4PF

ROUTP_RX LOUTP_RX VBG 1E8
ROUTM_RX LOUTM_RX VBG 1E8
VVBG VBG 0 1.1

.OPTION POST
.TRAN 10PS 20NS
.PLOT TRAN V(LOUTP) V(LOUTM) V(LOUTP_RX) V(LOUTM_RX)
+ V(LOUTP_RX,LOUTM_RX)
.END
```

As mentioned earlier (fig 2) there exists a feedback loop to control the PMOS current source. So when simulating the buffer along with internal load terminations or with external loads different from 100ohm the results may have a small DC shift (around 0.1V to 0.2V). This is because IBIS cannot model buffers with feedback (which changes the buffer characteristics with load).