NOTES, UNLESS OTHERWISE SPECIFIED:

1. The netname "P12V" represents connection to the +12V power plane.
2. The netname "P3V3" represents connection to the +3.3V power plane.
3. The netname "P1V8" represents connection to the +1.8V power plane.
4. The netname "P1V5" represents connection to the +1.5V power plane.
5. The netname "P1V2" represents connection to the +1.2V power plane.
6. The netname "P1V0_CORE" represents connection to the +1V power plane for the FPGA Core supply.
7. The netname "P1V0_MGT" represents connection to the filtered +1V power plane for the FPGA TX RX MGT.
8. The netname "V_OFFSET" represents connection to the +10V power plane.
9. The netname "V_RESET" represents connection to the -14V power plane.
10. The netname "V_BIAS" represents connection to the +18V power plane.

COMPUTER GENERATED DRAWING - DO NOT REVISE MANUALLY

REVISIONS

REV	DESCRIPTION	DATE	APPROVED
E.1	ECO 2175907: Initial Release	7/31/2018	DH

Contents

Page 2: FMC Connector 1
Page 3: FMC Connector 2
Page 4: Power
Page 5: FPGA Config
Page 6: I2C and Clocks
Page 7: FPGA Video data
Page 8: Unused FPGA Banks
Page 9: DMD Flex Cable Connectors
Page 10: FPGA Power and Ground

Revision E.2

Page 3, 4:
J1, J2 PN change from ASP-134488-01 to taller SEAM-40-11.0-S-10-2-A-K-TR for additional clearance when plugging in to VC707 board

Page 5:
U8, Pins 5, 9, 24 removed from same net. These pins now NC
U9, Pins 5, 9, 24 removed from same net. These pins now NC

Page 6:
D6, D7 pins 3 and 4 swap. Pin 3 is Green Cathode, Pin 4 is Red Cathode

Revision E.3

Page 7:
Added C514 to enable Cypress USB-I2C Circuitry

Revision E.4

Page 7:
U29 changed from CY7C65215A to CY7C65215. The 215A was holding I2C lines low before USB initialization
X3 changed from ASDMB-25.000MHZ-LY-T to DSC6111JE1A-PROGRAMMABLE programmed to 28.125 MHz to support 3.6 Gbps DMD operation
R13, R21, R22, R23 corrected to DNI in BOM

Page 10:
I2C going to DMD board is now 3.3V

Revision E.5

Page 3:
Added R238, R239, R240, R241, R242, R243, R244, R245, R246, R247, R248, R249, R250

Changed net FMC_GPIO_7 name to DMDLOAD_REQ

Revision E.6

Page 6:
Added R251 (install) and R252 (DNI)

DLP®
TEXAS INSTRUMENTS

TI INFORMATION
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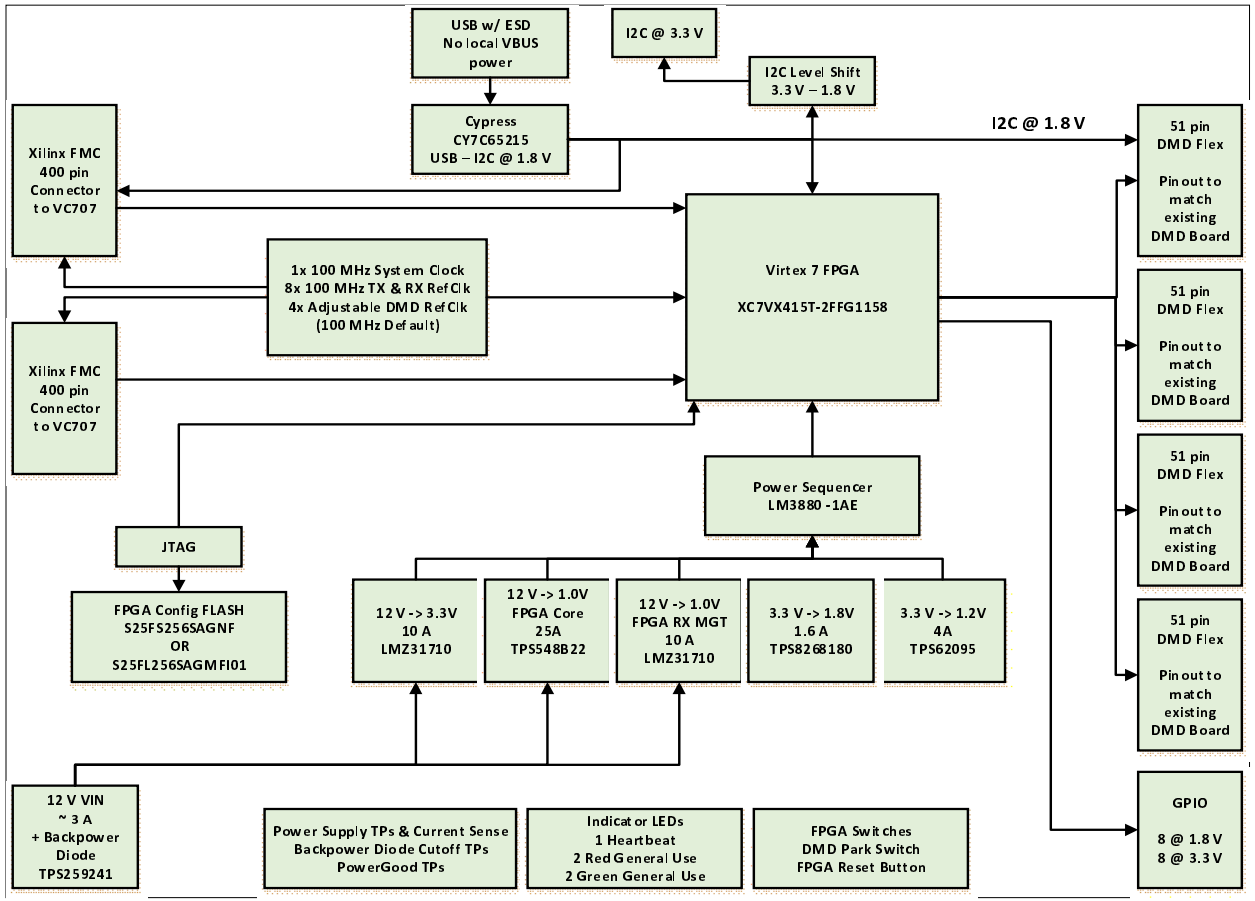
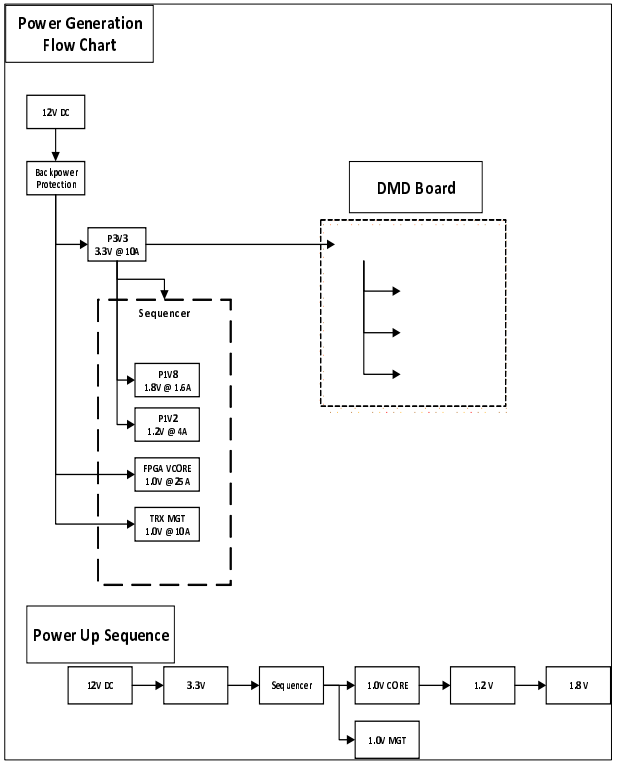
		DWN Ben Uhing DATE 3/11/2019	TEXAS INSTRUMENTS
		ENGR	(C) COPYRIGHT 2018 TEXAS INSTRUMENTS ALL RIGHTS RESERVED
		SYST Tim Ryan	TITLE: ESD, DLPC980 Controller Board EVM
		PRJ Mike McCormick	
		QA	
NEXT ASSY	USED ON		C / DRAWING NO 2516376 / REV E.6
APPLICATION		SW Cadence Capture V.17.2	SCALE / SHEET 1 of 12



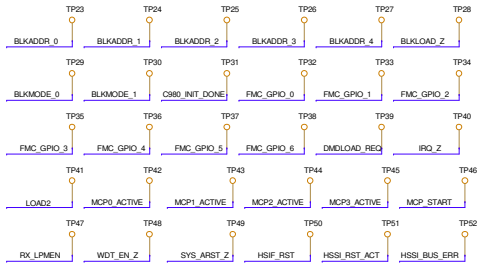


TEXAS INSTRUMENTS

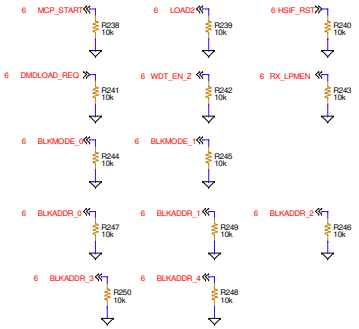
DWN	DATE	D	DRAWING NO	REV
Ben Uhing				E.6
ISSUE DATE		SCALE	SHEET 2 OF 12	

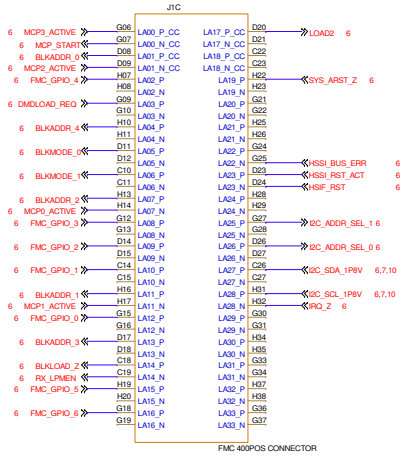
NOTE:

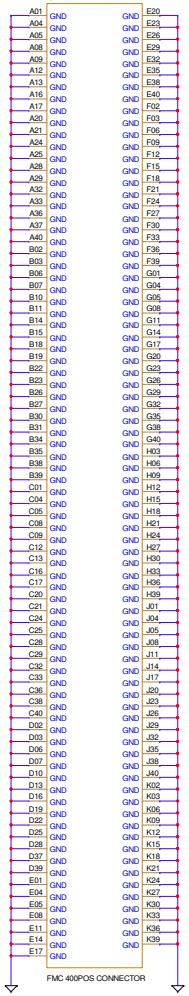
J1 on DLPC980 EVM connects to J35 on VC707 EVM

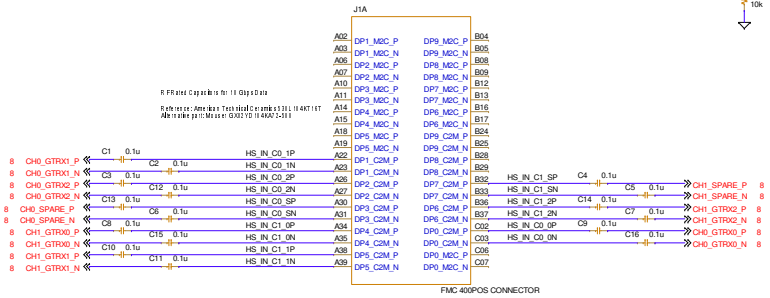


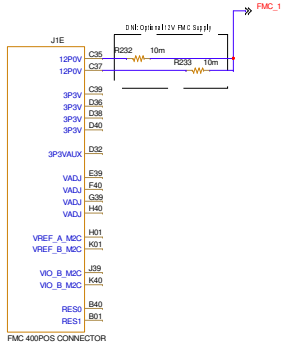
Pull-downs added for stand-alone controller

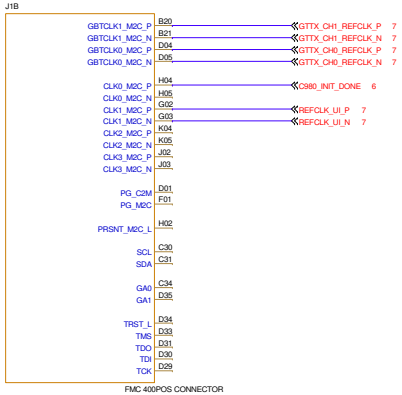


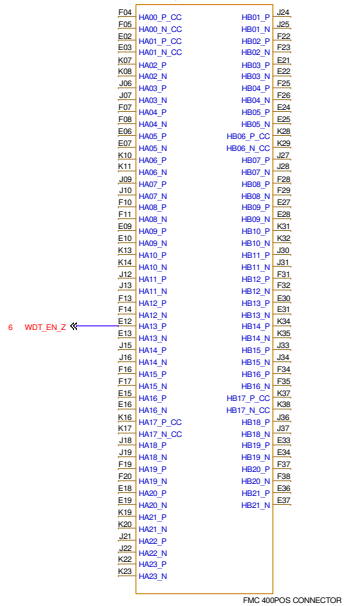








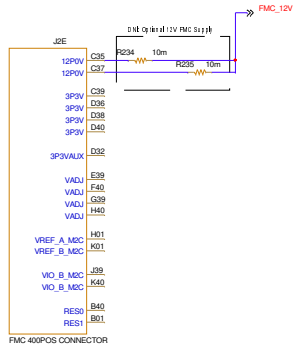


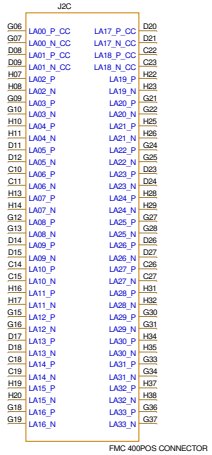


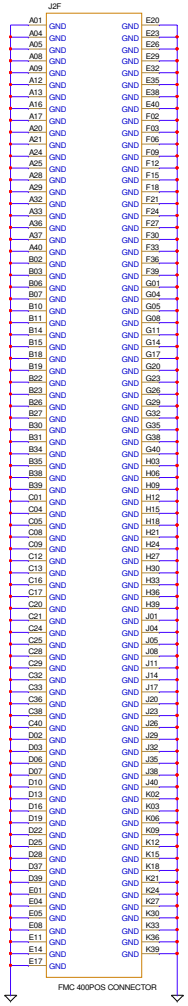
TEXAS INSTRUMENTS	DWN Ben Lihing	DATE	D	DRAWING NO
	ISSUE DATE		SCALE	SHEET 3 OF 12
				REV E.6

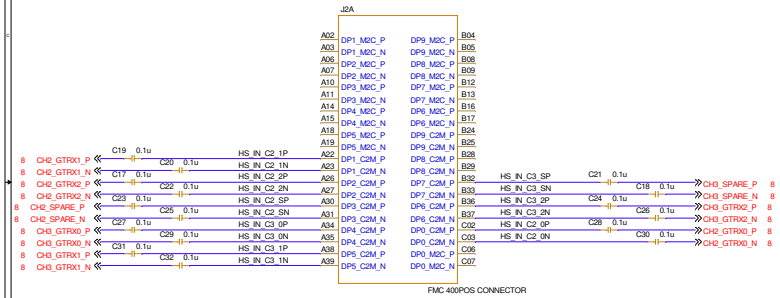
NOTE:

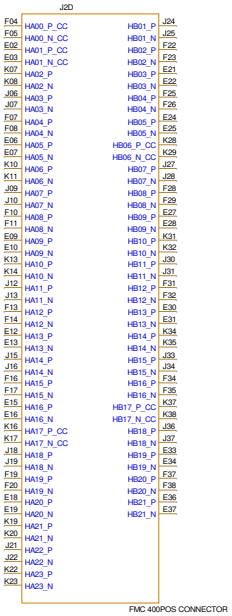
J2 on DLPC980 EVM connects to J37 on VC707 EVM

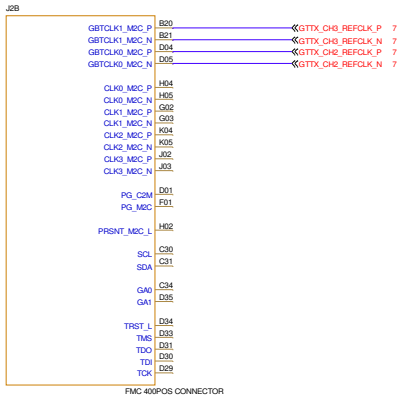












TEXAS INSTRUMENTS	DWN Ben Uhing	DATE	D	DRAWING NO
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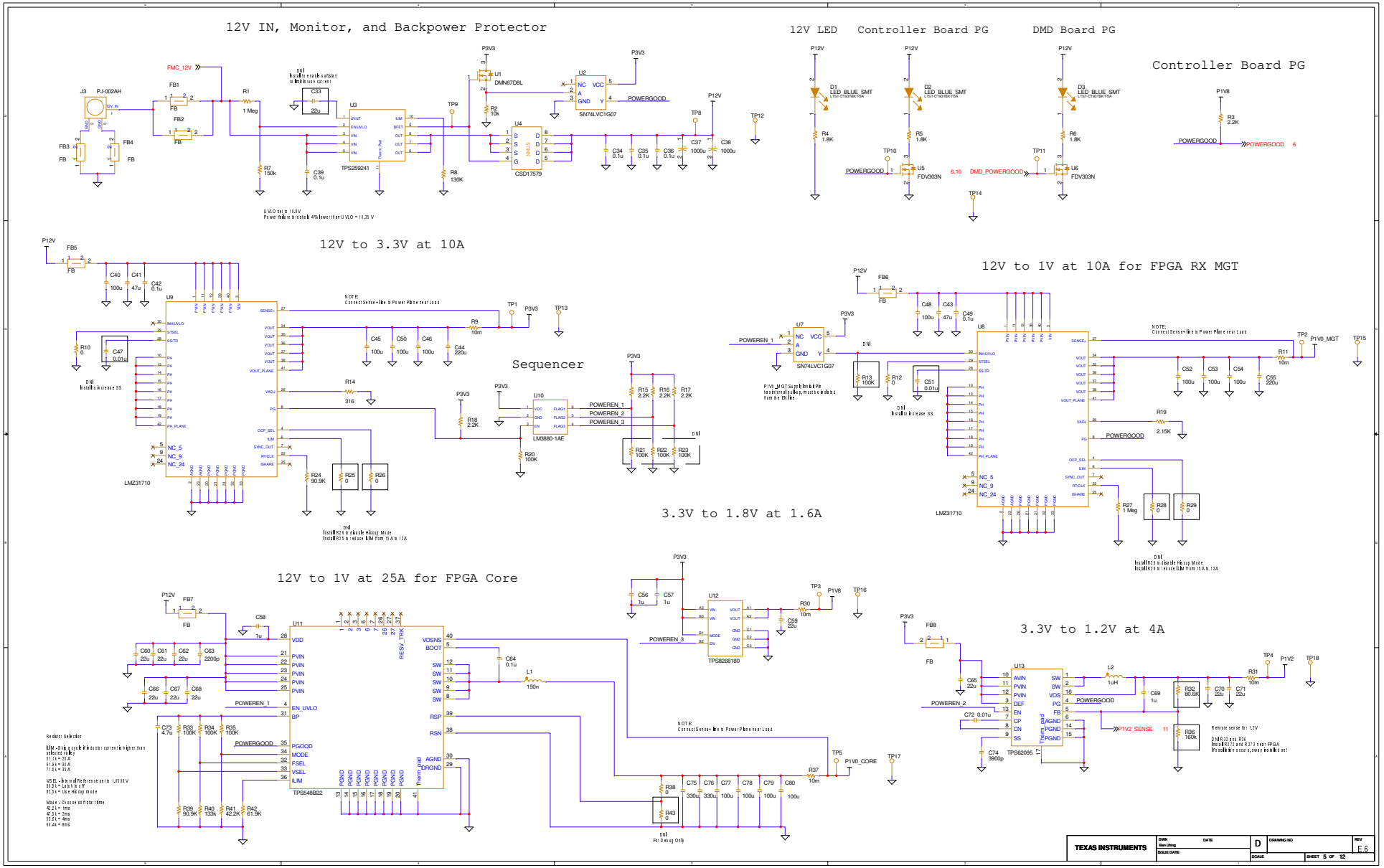
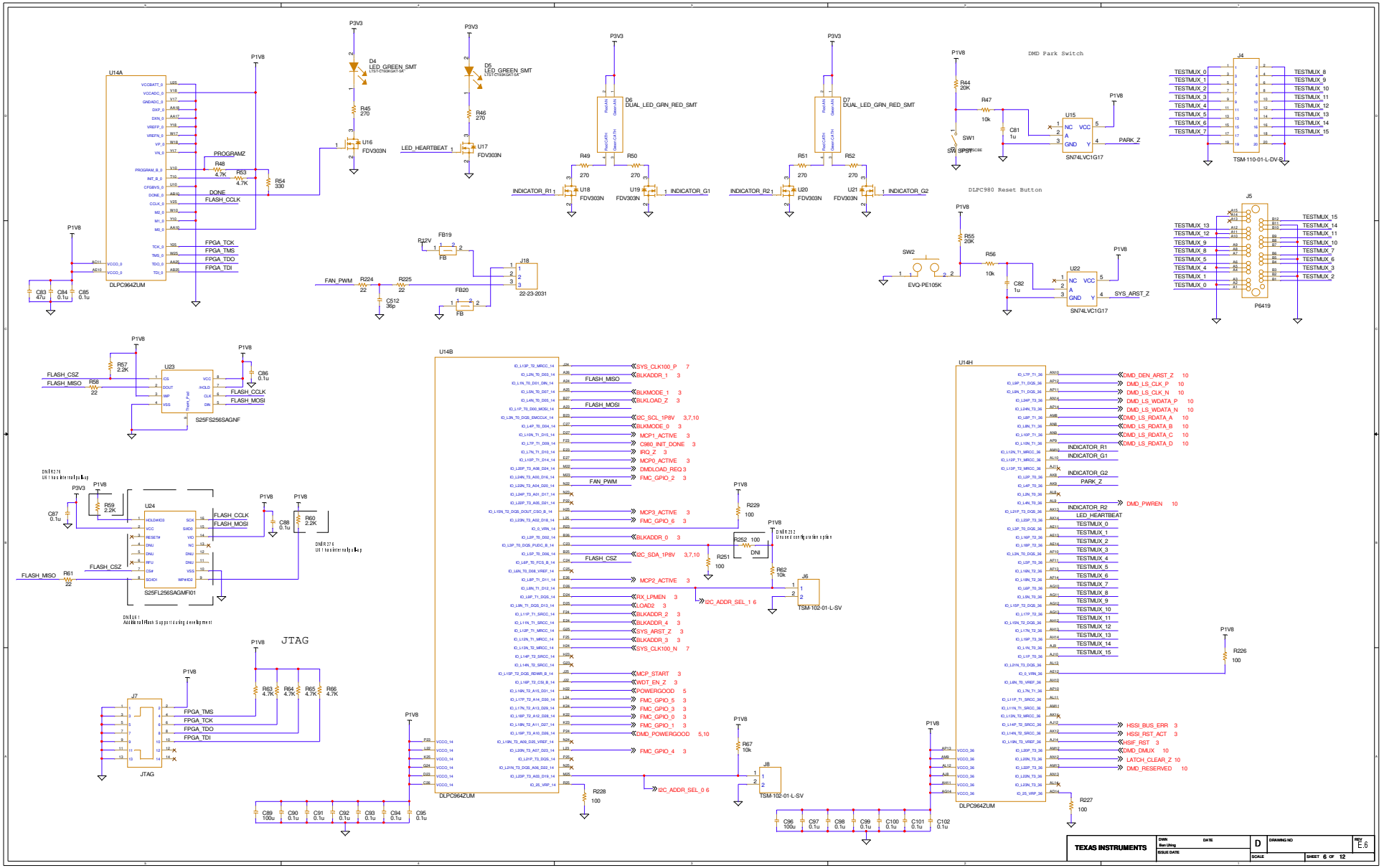
	SCALE		SHEET 4 OF 12	


12V IN, Monitor, and Backpower Protector
12V LED Controller Board PG
DMD Board PG
Controller Board PG
12V to 3.3V at 10A
12V to 1V at 10A for FPGA RX MGT
Sequencer
3.3V to 1.8V at 1.6A
12V to 1V at 25A for FPGA Core
3.3V to 1.2V at 4A
TEXAS INSTRUMENTS



U14A
DLPC964ZUM
P1V8
P3V3
D4
LED_GREEN_SMT
D5
LED_GREEN_SMT
R45
270
R46
270
U16
FDV303N
U17
FDV303N
LED_HEARTBEAT
PROGRAMZ
R48
4.7K
R53
4.7K
R54
330
DONE
FLASH_CCLK
FPGA_TCK
FPGA_TMS
FPGA_TDO
FPGA_TDI
C83
47u
C84
0.1u
C85
0.1u
D6
DUAL_LED_GRN_RED_SMT
D7
DUAL_LED_GRN_RED_SMT
R49
270
R50
270
R51
270
R52
270
INDICATOR_R1
INDICATOR_G1
INDICATOR_R2
INDICATOR_G2
U18
FDV303N
U19
FDV303N
U20
FDV303N
U21
FDV303N
DMD Park Switch
R44
20K
R47
10k
C81
1u
SW1
SW_SPST
U15
SN74LVC1G17
PARK_Z
J4
TSM-110-01-L-DV-P
DLPC980 Reset Button
R55
20K
R56
10k
C82
1u
SW2
EVQ-PE105K
U22
SN74LVC1G17
SYS_ARST_Z
J5
P6419
FB19
FB
FB20
FB
R12V
J18
22-23-2031
FAN_PWM
R224
22
R225
22
C512
36p
U23
S25FS256SAGNF
R57
2.2K
R58
22
C86
0.1u
FLASH_CSZ
FLASH_MISO
FLASH_CCLK
FLASH_MOSI
U24
S25FL256SAGMFI01
C87
0.1u
R59
2.2K
C88
0.1u
R60
2.2K
R61
22
DNI R276
U61 has internal pulls up
DNI R276
U61 has internal pulls up
DNI U61
Additional Flash Supporting development
JTAG
J7
JTAG
R63
4.7K
R64
4.7K
R65
4.7K
R66
4.7K
FPGA_TMS
FPGA_TCK
FPGA_TDO
FPGA_TDI
U14B
DLPC964ZUM
SYS_CLK100_P 7
BLKADDR_1 3
BLKMODE_1 3
BLKLOAD_Z 3
I2C_SCL_1P8V 3,7,10
BLKMODE_0 3
MCP1_ACTIVE 3
C980_INIT_DONE 3
IRQ_Z 3
MCP0_ACTIVE 3
DMDLOAD_REQ 3
FMC_GPIO_2 3
MCP3_ACTIVE 3
FMC_GPIO_6 3
BLKADDR_0 3
I2C_SDA_1P8V 3,7,10
MCP2_ACTIVE 3
RX_LPMEN 3
LOAD2 3
BLKADDR_2 3
BLKADDR_4 3
SYS_ARST_Z 3
BLKADDR_3 3
SYS_CLK100_N 7
MCP_START 3
WDT_EN_Z 3
POWERGOOD 5
FMC_GPIO_5 3
FMC_GPIO_3 3
FMC_GPIO_0 3
FMC_GPIO_1 3
DMD_POWERGOOD 5,10
FMC_GPIO_4 3
I2C_ADDR_SEL_0 6
I2C_ADDR_SEL_1 6
R229
100
R252
100
DNI
R251
100
R62
10k
J6
TSM-102-01-L-SV
R67
10k
J8
TSM-102-01-L-SV
R228
100
U14H
DLPC964ZUM
DMD_DEN_ARST_Z 10
DMD_LS_CLK_P 10
DMD_LS_CLK_N 10
DMD_LS_WDATA_P 10
DMD_LS_WDATA_N 10
DMD_LS_RDATA_A 10
DMD_LS_RDATA_B 10
DMD_LS_RDATA_C 10
DMD_LS_RDATA_D 10
INDICATOR_R1
INDICATOR_G1
INDICATOR_G2
PARK_Z
DMD_PWREN 10
INDICATOR_R2
LED_HEARTBEAT
TESTMUX_0
TESTMUX_1
TESTMUX_2
TESTMUX_3
TESTMUX_4
TESTMUX_5
TESTMUX_6
TESTMUX_7
TESTMUX_8
TESTMUX_9
TESTMUX_10
TESTMUX_11
TESTMUX_12
TESTMUX_13
TESTMUX_14
TESTMUX_15
R226
100
HSSI_BUS_ERR 3
HSSI_RST_ACT 3
HSIF_RST 3
DMD_DMUX 10
LATCH_CLEAR_Z 10
DMD_RESERVED 10
R227
100
C89
100u
C90
0.1u
C91
0.1u
C92
0.1u
C93
0.1u
C94
0.1u
C95
0.1u
C96
100u
C97
0.1u
C98
0.1u
C99
0.1u
C100
0.1u
C101
0.1u
C102
0.1u
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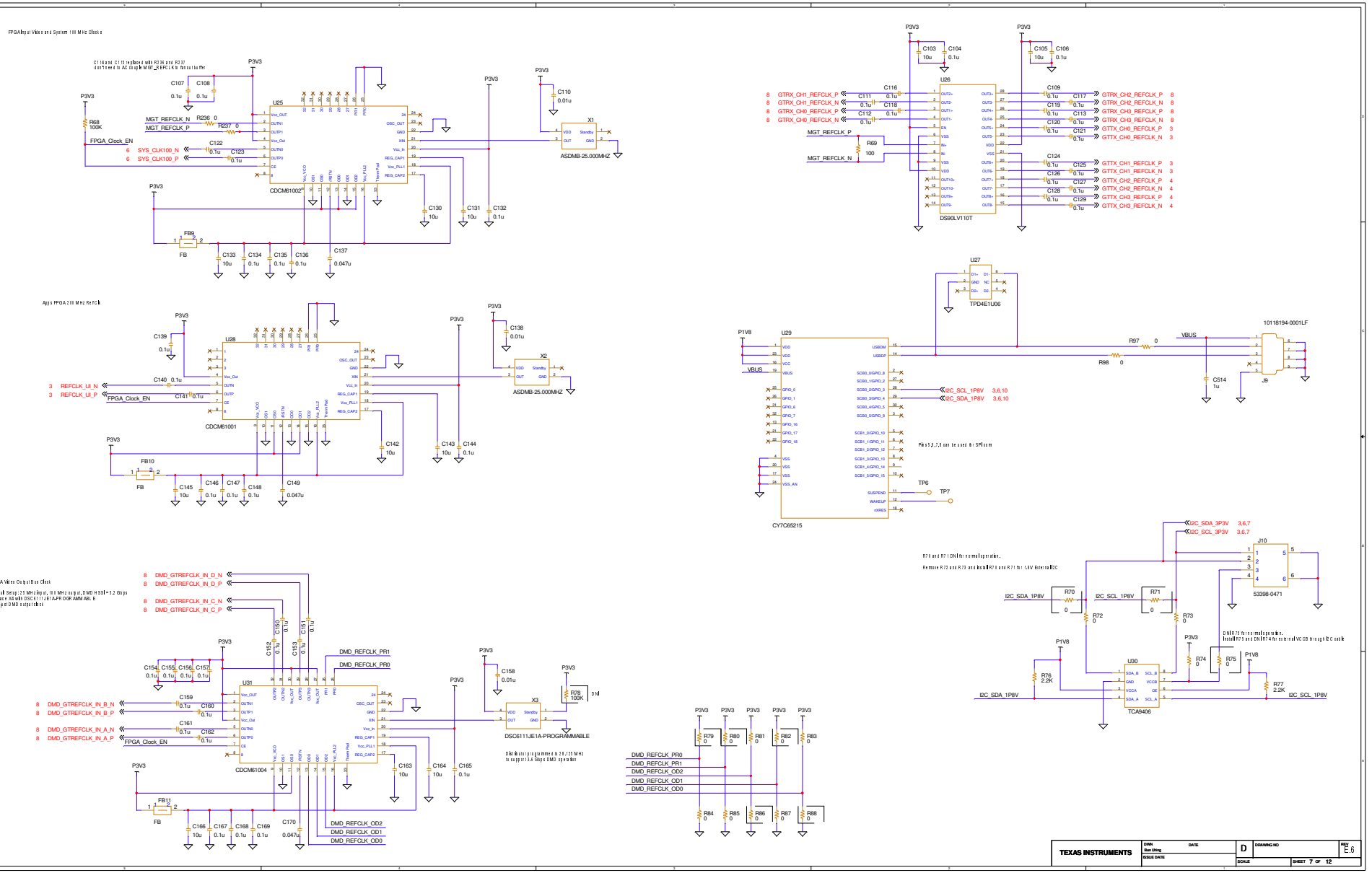
SHEET 6 OF 12


FPGA Input Video and System 100 MHz Clocks
C114 and C115 replaced with R236 and R237
don't need to AC couple MGT_REFCLK to fanout buffer
U25
CDCM61002
MGT_REFCLK_N
MGT_REFCLK_P
FPGA_Clock_EN
SYS_CLK100_N
SYS_CLK100_P
X1
ASDMB-25.000MHZ
FB9
FB
Apps FPGA 200 MHz Ref Clk
U28
CDCM61001
REFCLK_UI_N
REFCLK_UI_P
X2
ASDMB-25.000MHZ
FB10
FB
FPGA Video Output Bus Clock
Default Setup: 25 MHz input, 100 MHz output, DMD HSSI=3.2 Gbps
Replace X4 with DSC6111JE1A-PROGRAMMABLE
to adjust DMD output clock
DMD_GTREFCLK_IN_D_N
DMD_GTREFCLK_IN_D_P
DMD_GTREFCLK_IN_C_N
DMD_GTREFCLK_IN_C_P
DMD_GTREFCLK_IN_B_N
DMD_GTREFCLK_IN_B_P
DMD_GTREFCLK_IN_A_N
DMD_GTREFCLK_IN_A_P
U31
CDCM61004
DMD_REFCLK_PR1
DMD_REFCLK_PR0
DMD_REFCLK_OD2
DMD_REFCLK_OD1
DMD_REFCLK_OD0
X3
DSC6111JE1A-PROGRAMMABLE
Distributor programmed to 20.125 MHz
to support 13.6 Gbps DMD operation
U26
DS90LV110T
GTRX_CH1_REFCLK_P
GTRX_CH1_REFCLK_N
GTRX_CH0_REFCLK_P
GTRX_CH0_REFCLK_N
GTRX_CH2_REFCLK_P
GTRX_CH2_REFCLK_N
GTRX_CH3_REFCLK_P
GTRX_CH3_REFCLK_N
GTTX_CH0_REFCLK_P
GTTX_CH0_REFCLK_N
GTTX_CH1_REFCLK_P
GTTX_CH1_REFCLK_N
GTTX_CH2_REFCLK_P
GTTX_CH2_REFCLK_N
GTTX_CH3_REFCLK_P
GTTX_CH3_REFCLK_N
U27
TPD4E1U06
U29
CY7C65215
I2C_SCL_1P8V
I2C_SDA_1P8V
VBUS
10118194-0001LF
J9
TP6
TP7
R70 and R71 DNI for normal operation.
Remove R72 and R73 and install R76 and R77 for 1.8V External I2C
J10
53398-0471
I2C_SDA_3P3V
I2C_SCL_3P3V
U30
TCA9406
DNI R75 for normal operation.
Install R75 and DNI R74 for external VCCB through I2C cable
DMD_REFCLK_PR0
DMD_REFCLK_PR1
DMD_REFCLK_OD2
DMD_REFCLK_OD1
DMD_REFCLK_OD0
TEXAS INSTRUMENTS
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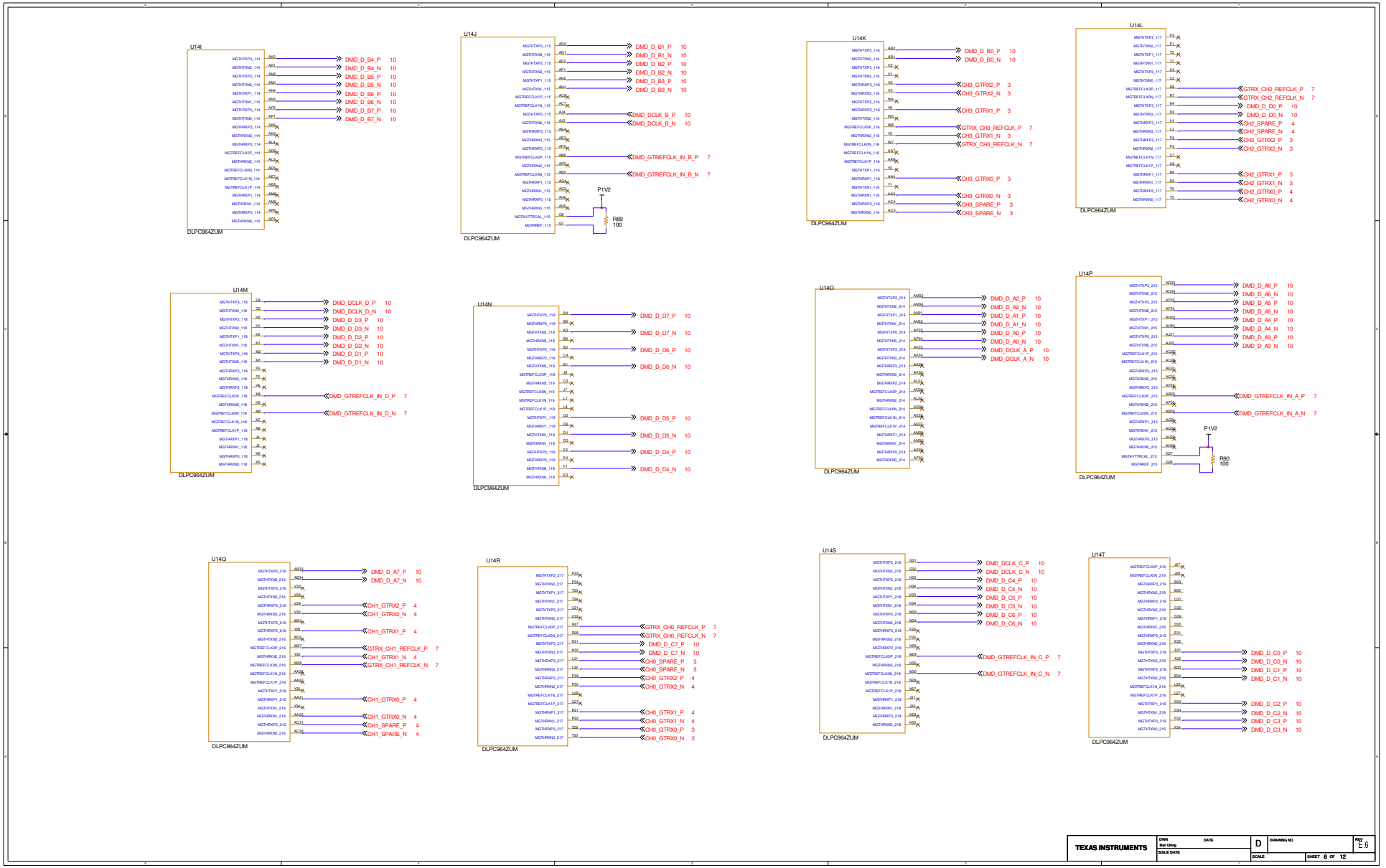
Ben Uhing
DATE
ISSUE DATE
D
DRAWING NO
REV
E.6
SCALE
SHEET 7 OF 12


U14I
DLPC964ZUM
DMD_D_B4_P 10
DMD_D_B4_N 10
DMD_D_B5_P 10
DMD_D_B5_N 10
DMD_D_B6_P 10
DMD_D_B6_N 10
DMD_D_B7_P 10
DMD_D_B7_N 10
U14J
DLPC964ZUM
DMD_D_B1_P 10
DMD_D_B1_N 10
DMD_D_B2_P 10
DMD_D_B2_N 10
DMD_D_B3_P 10
DMD_D_B3_N 10
DMD_DCLK_B_P 10
DMD_DCLK_B_N 10
DMD_GTREFCLK_IN_B_P 7
DMD_GTREFCLK_IN_B_N 7
P1V2
R89
100
U14K
DLPC964ZUM
DMD_D_B0_P 10
DMD_D_B0_N 10
CH3_GTRX2_P 3
CH3_GTRX2_N 3
CH3_GTRX1_P 3
GTRX_CH3_REFCLK_P 7
CH3_GTRX1_N 3
GTRX_CH3_REFCLK_N 7
CH3_GTRX0_P 3
CH3_GTRX0_N 3
CH3_SPARE_P 3
CH3_SPARE_N 3
U14L
DLPC964ZUM
GTRX_CH2_REFCLK_P 7
GTRX_CH2_REFCLK_N 7
DMD_D_D0_P 10
DMD_D_D0_N 10
CH2_SPARE_P 4
CH2_SPARE_N 4
CH2_GTRX2_P 3
CH2_GTRX2_N 3
CH2_GTRX1_P 3
CH2_GTRX1_N 3
CH2_GTRX0_P 4
CH2_GTRX0_N 4
U14M
DLPC964ZUM
DMD_DCLK_D_P 10
DMD_DCLK_D_N 10
DMD_D_D3_P 10
DMD_D_D3_N 10
DMD_D_D2_P 10
DMD_D_D2_N 10
DMD_D_D1_P 10
DMD_D_D1_N 10
DMD_GTREFCLK_IN_D_P 7
DMD_GTREFCLK_IN_D_N 7
U14N
DLPC964ZUM
DMD_D_D7_P 10
DMD_D_D7_N 10
DMD_D_D6_P 10
DMD_D_D6_N 10
DMD_D_D5_P 10
DMD_D_D5_N 10
DMD_D_D4_P 10
DMD_D_D4_N 10
U14O
DLPC964ZUM
DMD_D_A2_P 10
DMD_D_A2_N 10
DMD_D_A1_P 10
DMD_D_A1_N 10
DMD_D_A0_P 10
DMD_D_A0_N 10
DMD_DCLK_A_P 10
DMD_DCLK_A_N 10
U14P
DLPC964ZUM
DMD_D_A6_P 10
DMD_D_A6_N 10
DMD_D_A5_P 10
DMD_D_A5_N 10
DMD_D_A4_P 10
DMD_D_A4_N 10
DMD_D_A3_P 10
DMD_D_A3_N 10
DMD_GTREFCLK_IN_A_P 7
DMD_GTREFCLK_IN_A_N 7
P1V2
R90
100
U14Q
DLPC964ZUM
DMD_D_A7_P 10
DMD_D_A7_N 10
CH1_GTRX2_P 4
CH1_GTRX2_N 4
CH1_GTRX1_P 4
GTRX_CH1_REFCLK_P 7
CH1_GTRX1_N 4
GTRX_CH1_REFCLK_N 7
CH1_GTRX0_P 4
CH1_GTRX0_N 4
CH1_SPARE_P 4
CH1_SPARE_N 4
U14R
DLPC964ZUM
GTRX_CH0_REFCLK_P 7
GTRX_CH0_REFCLK_N 7
DMD_D_C7_P 10
DMD_D_C7_N 10
CH0_SPARE_P 3
CH0_SPARE_N 3
CH0_GTRX2_P 4
CH0_GTRX2_N 4
CH0_GTRX1_P 4
CH0_GTRX1_N 4
CH0_GTRX0_P 3
CH0_GTRX0_N 3
U14S
DLPC964ZUM
DMD_DCLK_C_P 10
DMD_DCLK_C_N 10
DMD_D_C4_P 10
DMD_D_C4_N 10
DMD_D_C5_P 10
DMD_D_C5_N 10
DMD_D_C6_P 10
DMD_D_C6_N 10
DMD_GTREFCLK_IN_C_P 7
DMD_GTREFCLK_IN_C_N 7
U14T
DLPC964ZUM
DMD_D_C0_P 10
DMD_D_C0_N 10
DMD_D_C1_P 10
DMD_D_C1_N 10
DMD_D_C2_P 10
DMD_D_C2_N 10
DMD_D_C3_P 10
DMD_D_C3_N 10
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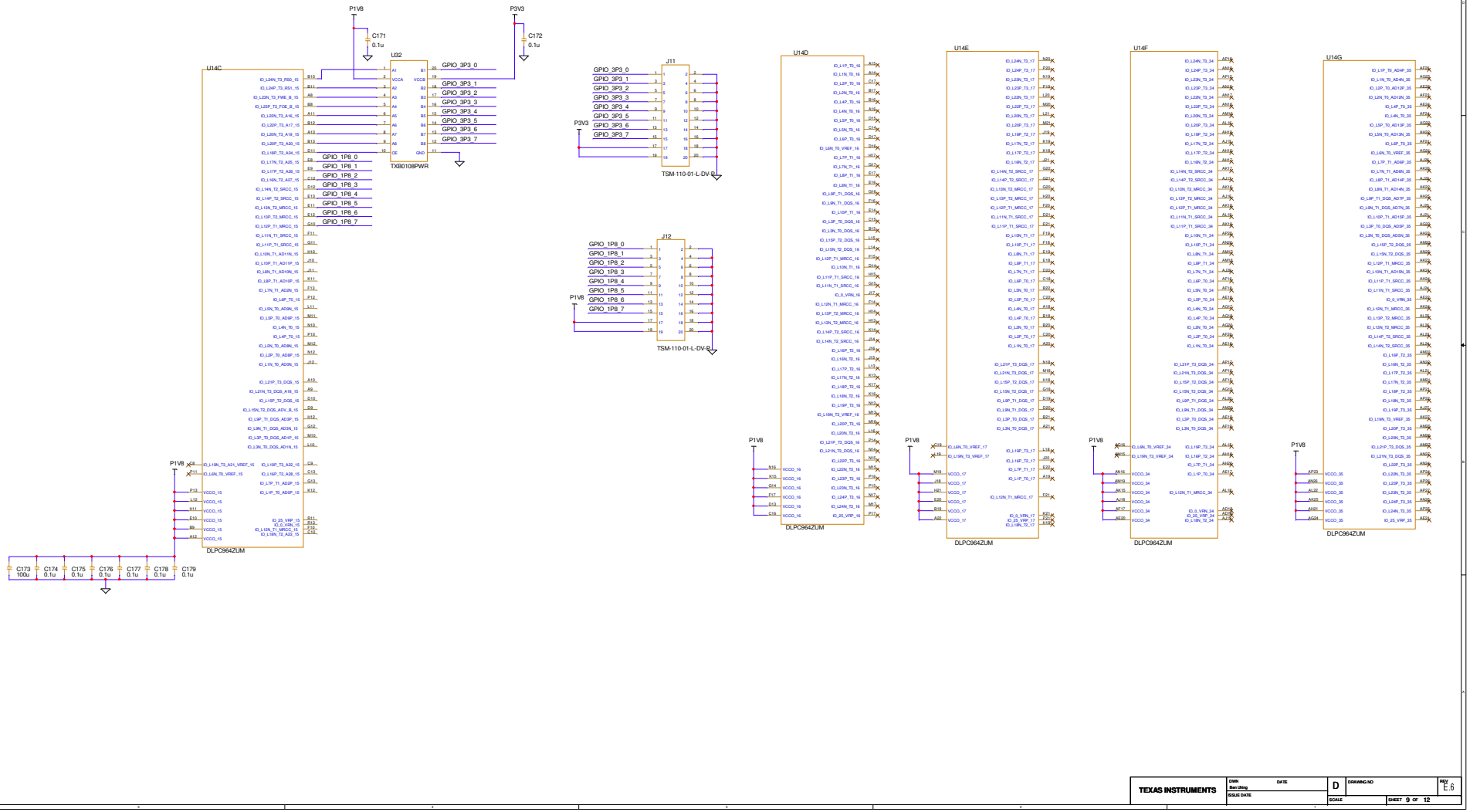
SHEET 8 OF 12


P1V8
C171
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P3V3
C172
0.1u
U32
TXB0108PWRPW
GPIO_3P3_0
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GPIO_3P3_2
GPIO_3P3_3
GPIO_3P3_4
GPIO_3P3_5
GPIO_3P3_6
GPIO_3P3_7
GPIO_1P8_0
GPIO_1P8_1
GPIO_1P8_2
GPIO_1P8_3
GPIO_1P8_4
GPIO_1P8_5
GPIO_1P8_6
GPIO_1P8_7
U14C
DLPC964ZUM
J11
TSM-110-01-L-DV-P
J12
TSM-110-01-L-DV-P
U14D
DLPC964ZUM
U14E
DLPC964ZUM
U14F
DLPC964ZUM
U14G
DLPC964ZUM
C173
100u
C174
0.1u
C175
0.1u
C176
0.1u
C177
0.1u
C178
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C179
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DRAWING NO
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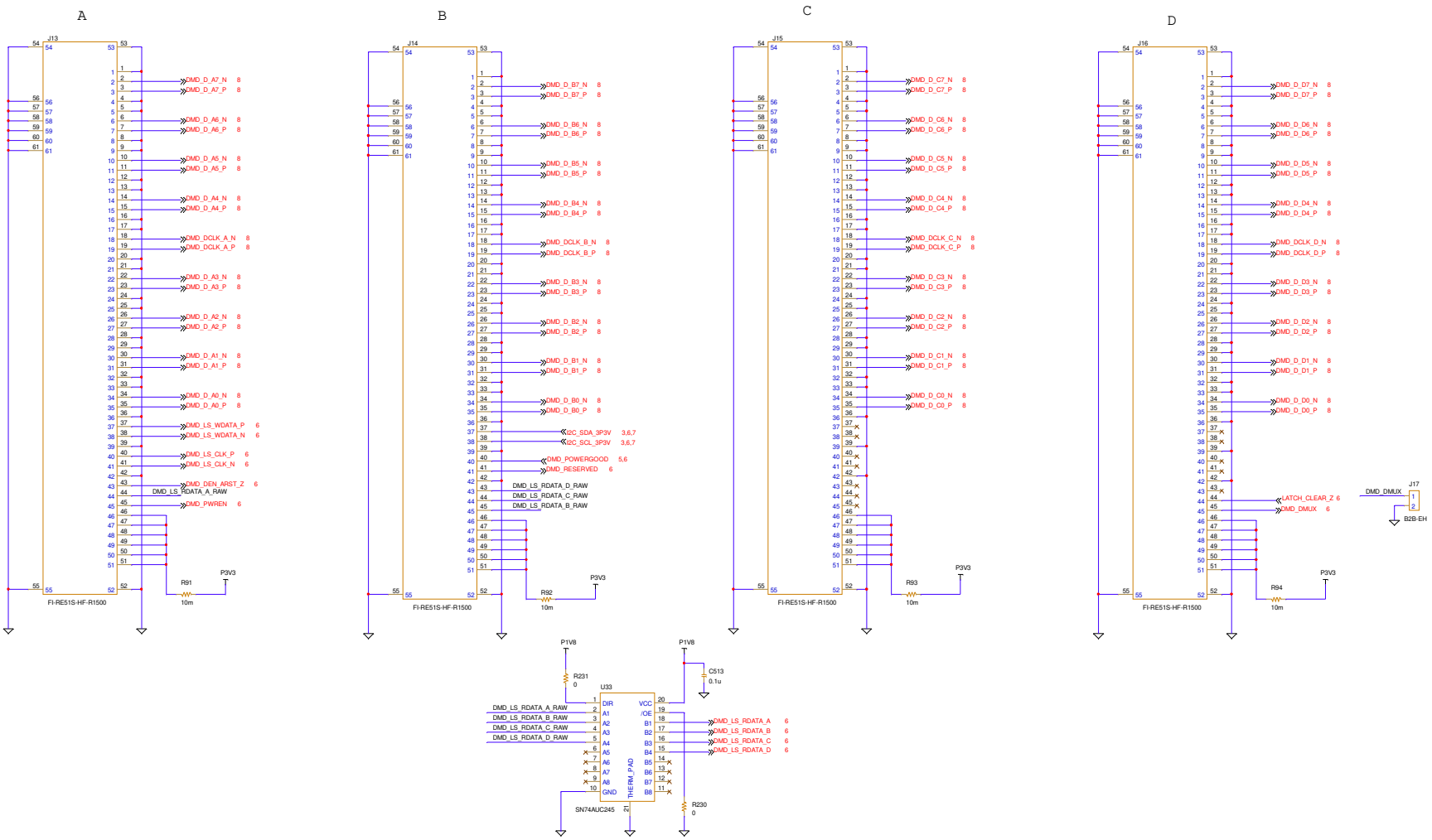
E.6
SCALE
SHEET 9 OF 12

Flex Cable 51-pin Connectors to DMD Board



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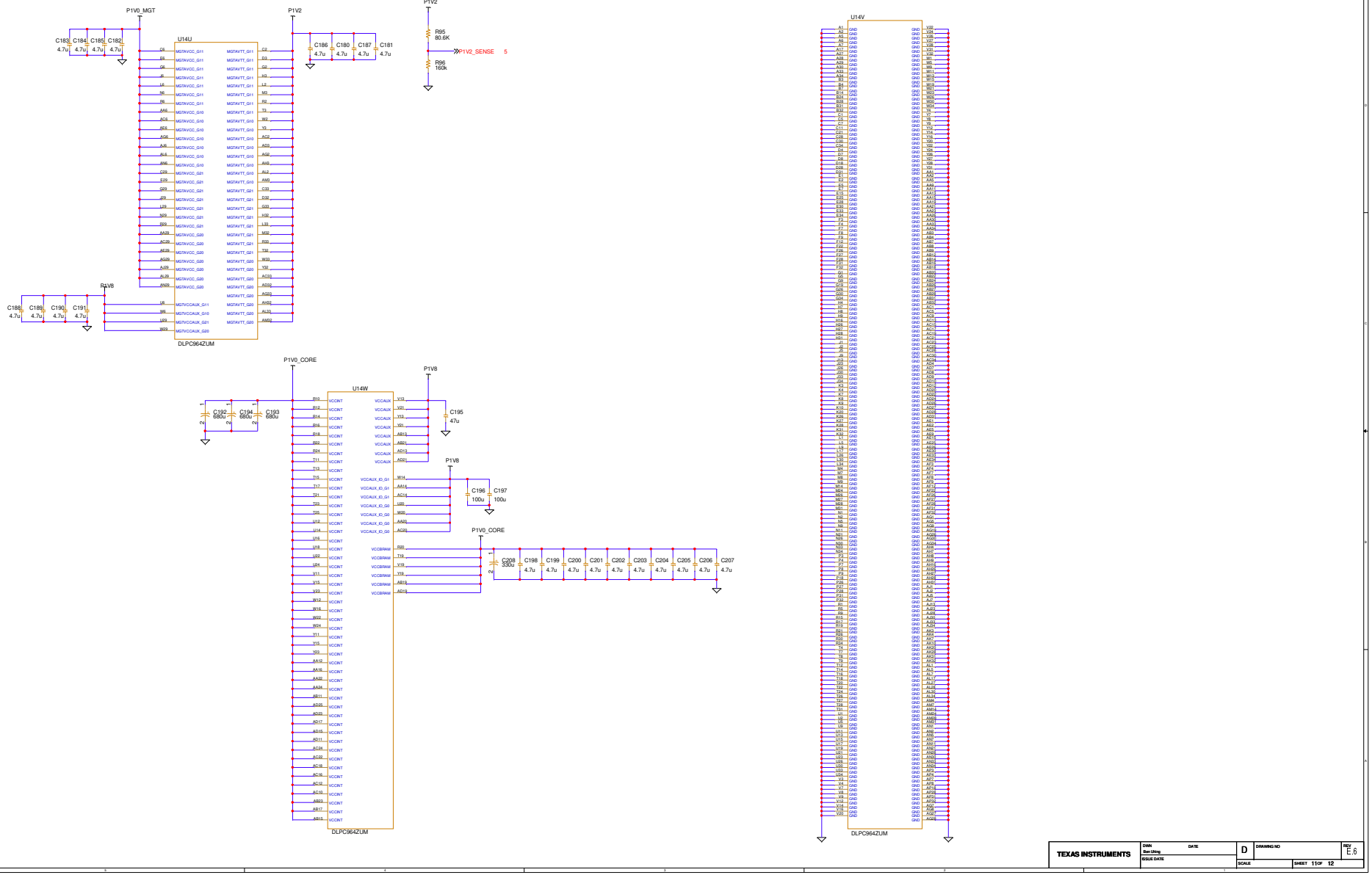
P1V0_MGT
P1V2
U14U
C183 4.7u
C184 4.7u
C185 4.7u
C182 4.7u
C186 4.7u
C180 4.7u
C187 4.7u
C181 4.7u
R95 80.6K
R96 160k
P1V2_SENSE 5
R1V8
C188 4.7u
C189 4.7u
C190 4.7u
C191 4.7u
DLPC964ZUM
P1V0_CORE
U14W
P1V8
C192 680u
C194 680u
C193 680u
C195 47u
C196 100u
C197 100u
C208 330u
C198 4.7u
C199 4.7u
C200 4.7u
C201 4.7u
C202 4.7u
C203 4.7u
C204 4.7u
C205 4.7u
C206 4.7u
C207 4.7u
DLPC964ZUM
U14V
DLPC964ZUM
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SHEET 11 OF 12

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