COMPUTER GENERATED DRAWING - DO NOT REVISE MANUALLY

REVISIONS

REV	DESCRIPTION	DATE	APPROVED
A	Initial Release		
B	Pre-EVM Release Update	3/3/2021	
C	Pre-EVM Release Update	5/15/2023	

		DWN	Mike McCormick	DATE 2/17/2023
		ENGR	Tim Ryan	9/9/2022
		SYST	Mike McCormick	9/9/2022
PWB: 2518421		PRJ	John O'Connor	7/27/2020
CCA: 2518422		QA	Mark Dorak	7/27/2020
NEXT ASSY	USED ON			
APPLICATION		SW	Cadence Capture V.17.2	

TEXAS INSTRUMENTS

TITLE

ESD, DLP082C - DLPLCRC910EVM Schematic

C	DRAWING NO 2518420	REV C
SCALE	SHEET 1 of 19	

PMBUS ADDRESSES

TPS65400
1101 001_

DMD 3.3V CURRENT SENSE
1000 000_

3.3V CURRENT SENSE
1000 001_

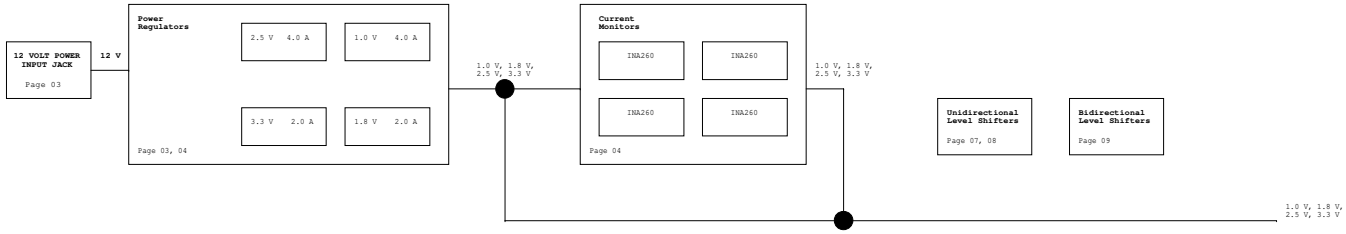
2.5V CURRENT SENSE
1001 100_

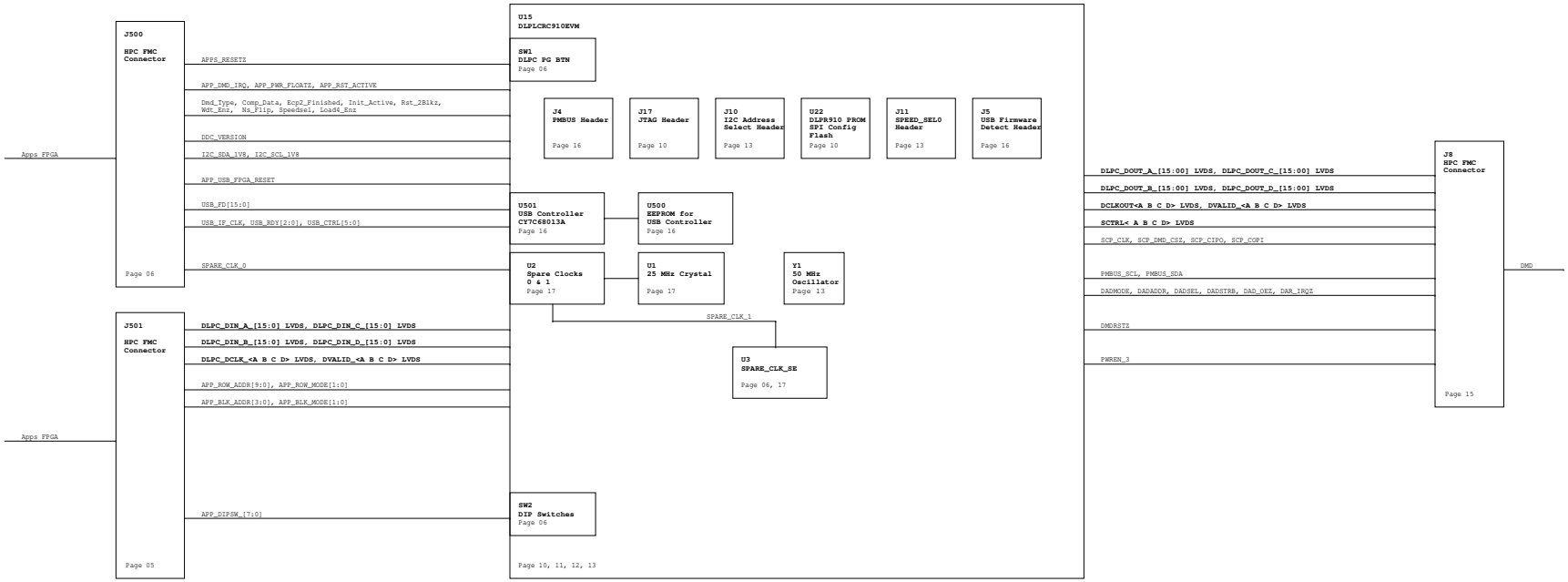
1.8V CURRENT SENSE
1000 011_

1.0V CURRENT SENSE
1000 010_

I2C BUS ADDRESSES

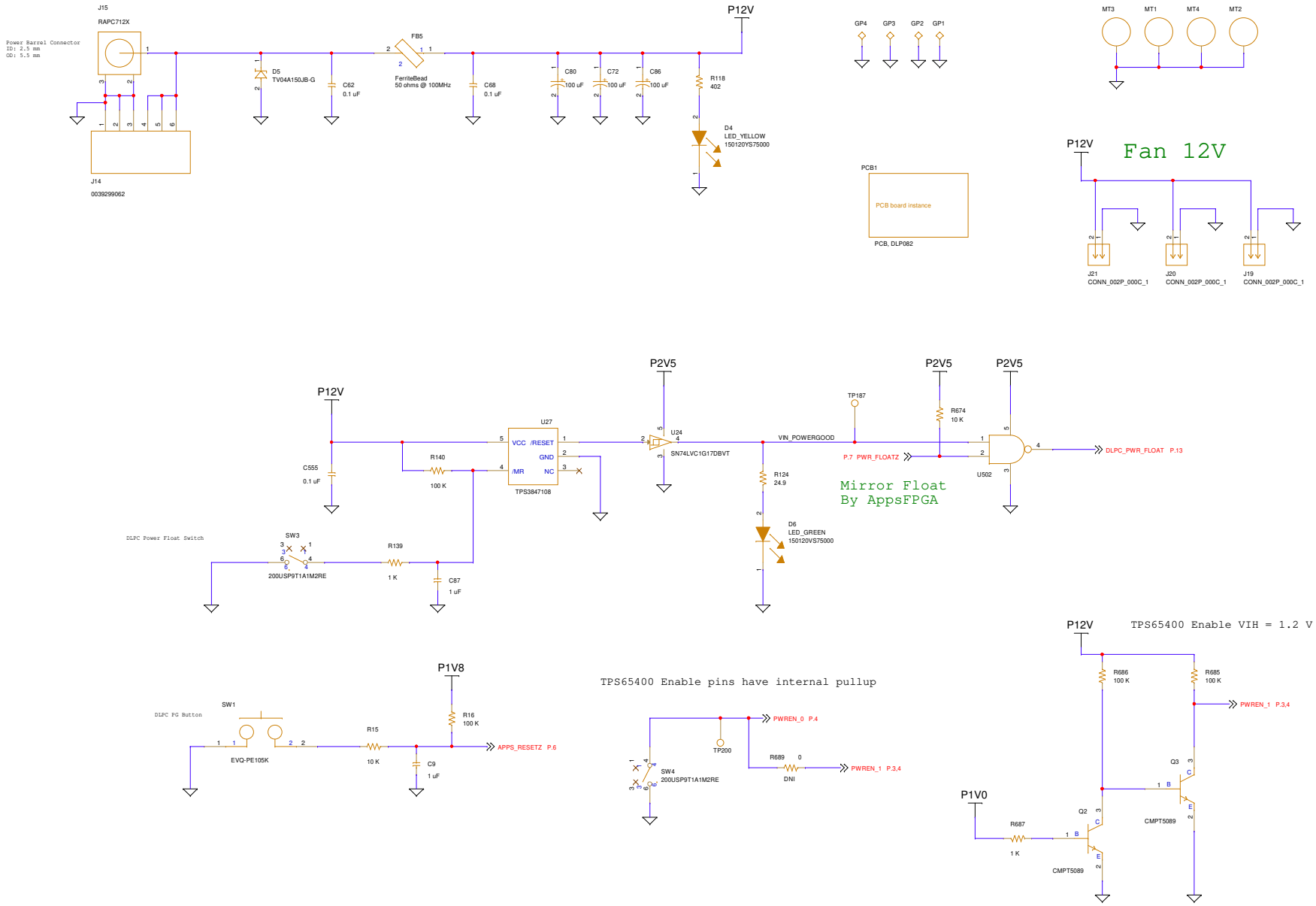
DLPC910
0110 100_ OR 0110 110_





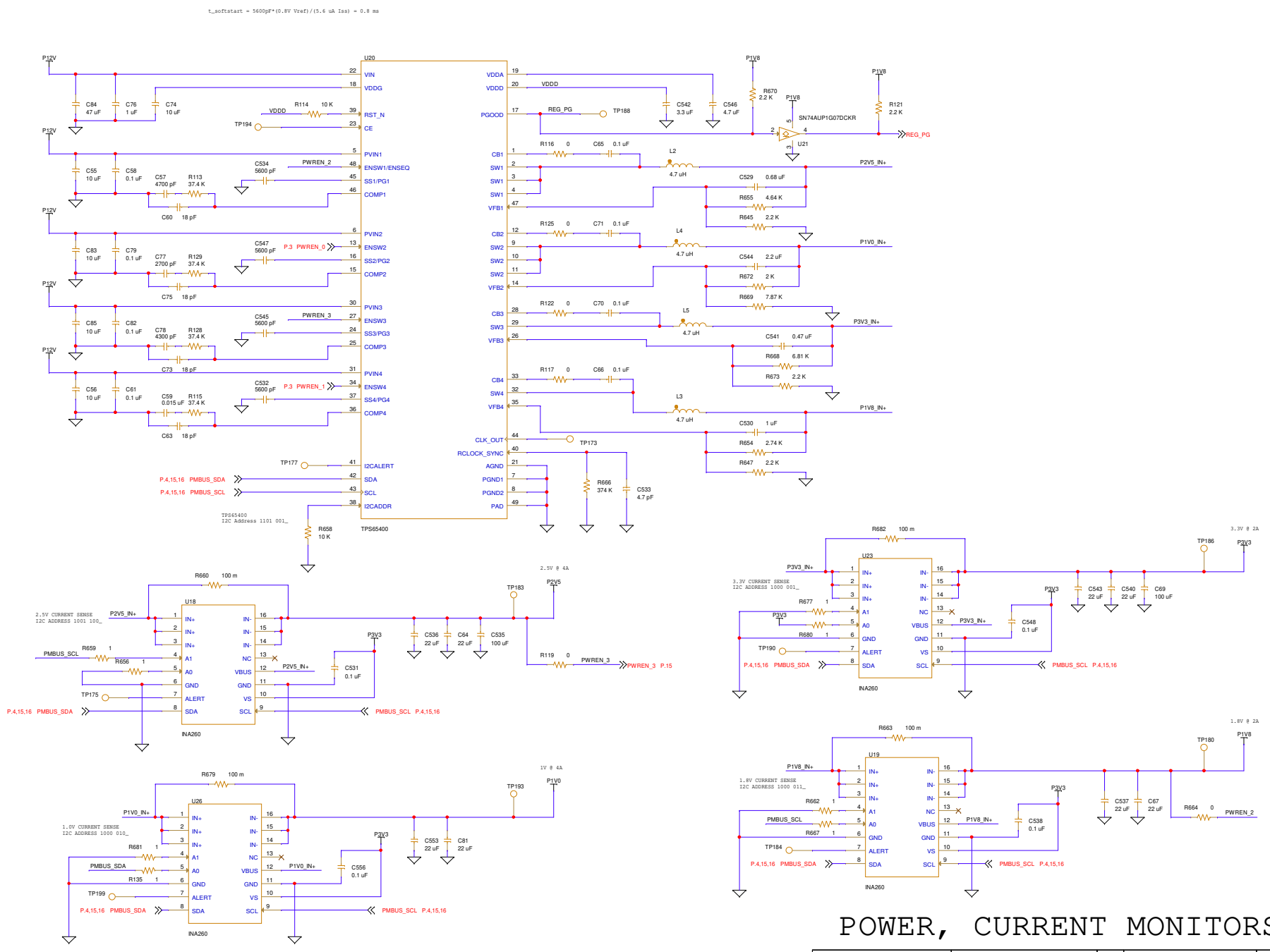
BLOCK DIAGRAM

TEXAS INSTRUMENTS	DWN Mike McCormick	DATE 2/17/2023	C	DRAWING NO 2518420 REV C
	ISSUE DATE //		SCALE	SHEET 2 OF 19



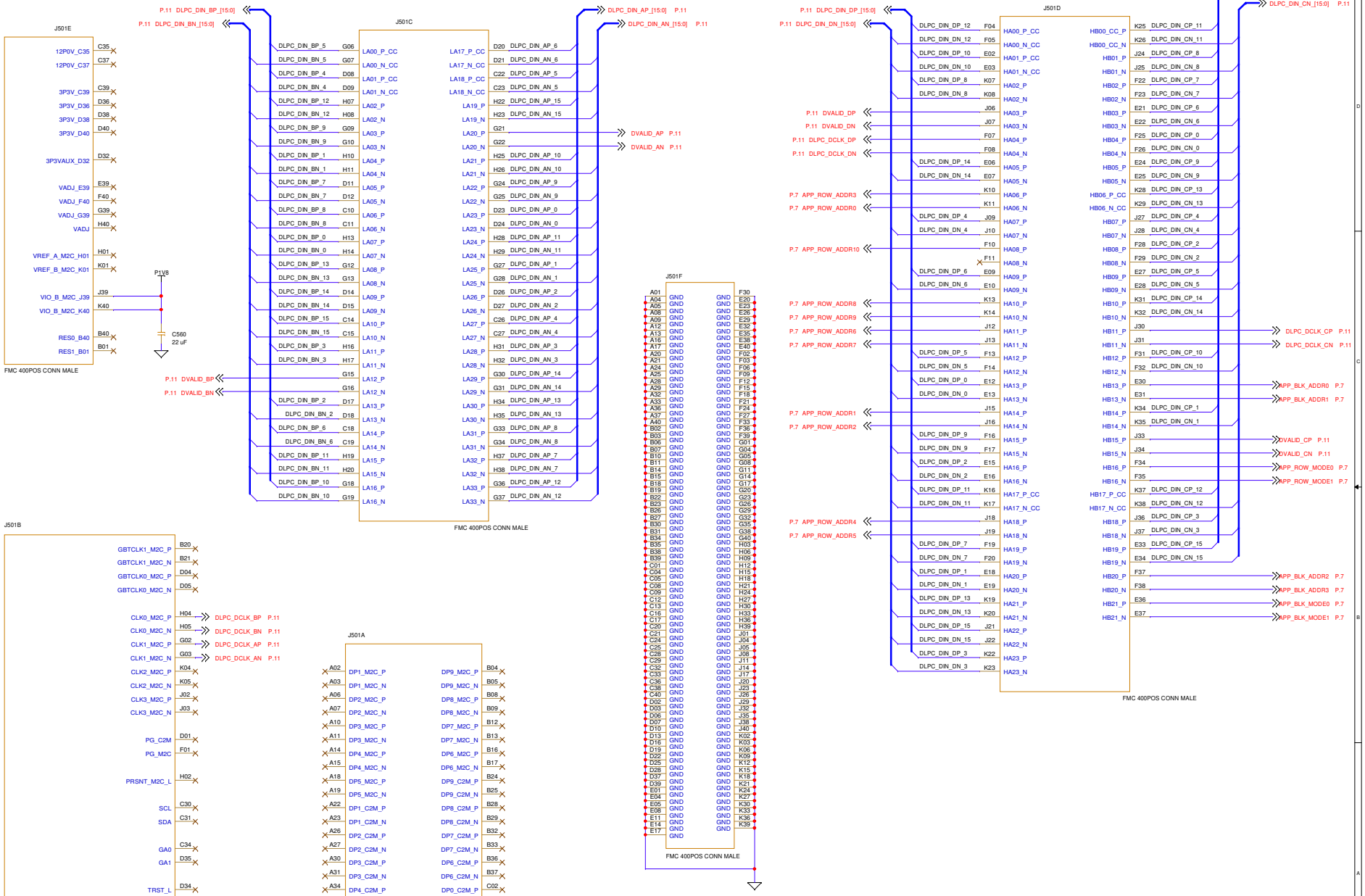
POWER IN, MONITORING

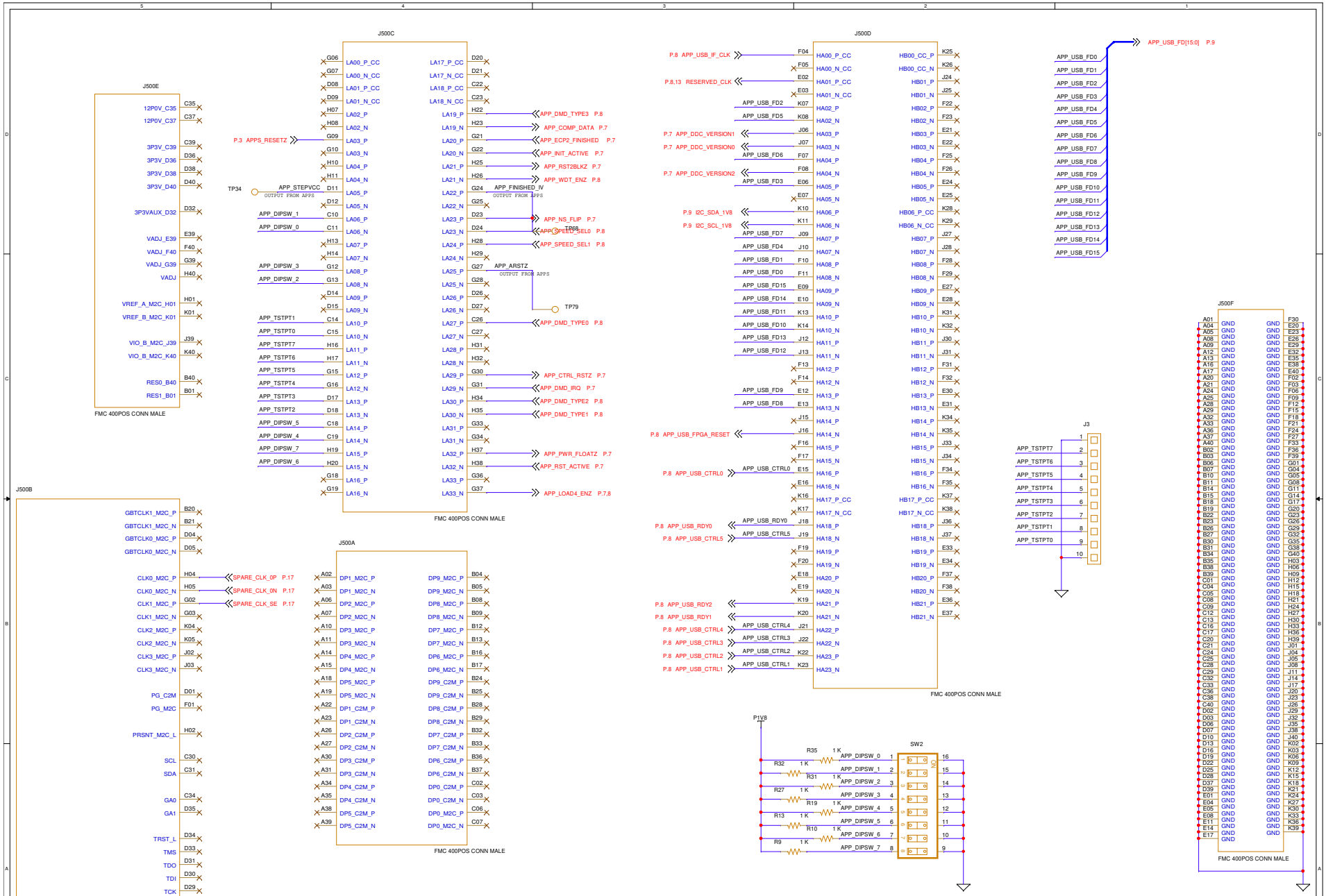
TEXAS INSTRUMENTS	DWN Mike McCormick	DATE 2/17/2023	C	DRAWING NO 2518420	REV C
	ISSUE DATE //			SCALE	SHEET 3 OF 19

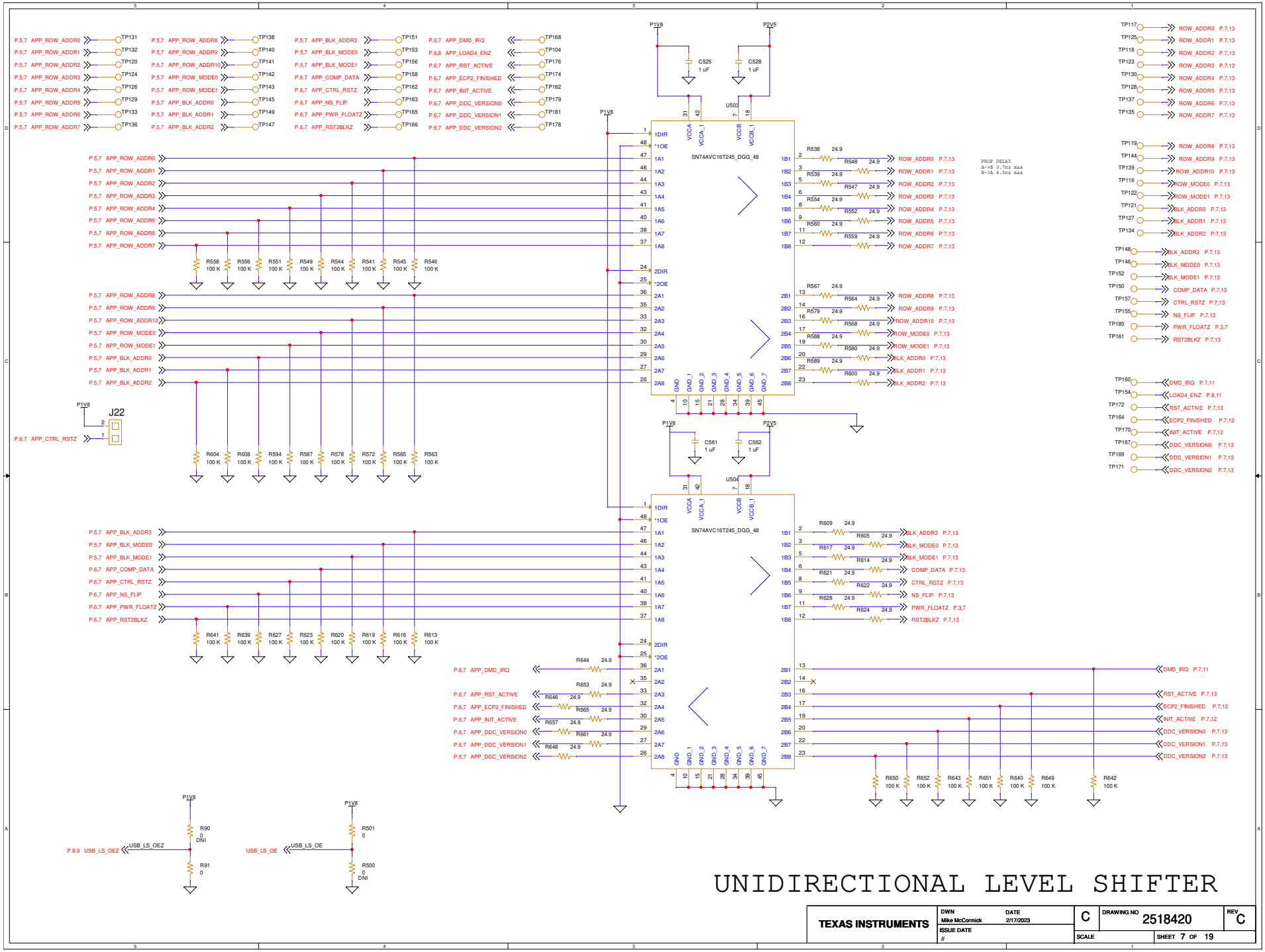


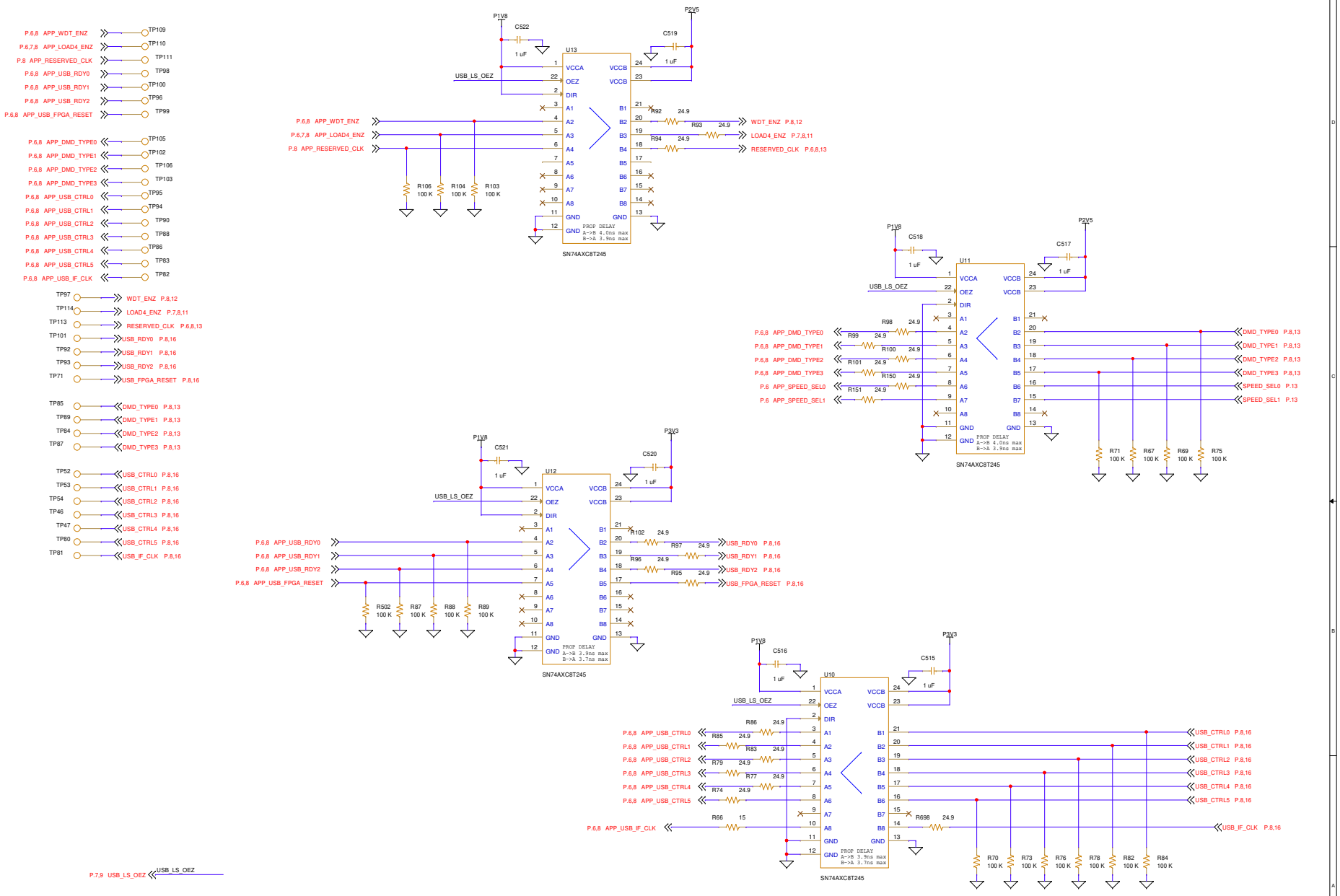
POWER, CURRENT MONITORS

TEXAS INSTRUMENTS	DWN Mike McCormick	DATE 2/17/2023	C	DRAWING NO 2518420	REV C
	ISSUE DATE //		SCALE	SHEET 4 OF 19	


J501E
FMC 400POS CONN MALE
J501C
FMC 400POS CONN MALE
J501F
FMC 400POS CONN MALE
J501D
FMC 400POS CONN MALE
J501B
FMC 400POS CONN MALE
J501A
FMC 400POS CONN MALE
P1V8
C560
22 uF
FMC1 TO VC707 APPLICATIONS FPGA
TEXAS INSTRUMENTS
DWN
Mike McCormick
DATE
2/17/2023
ISSUE DATE
//
C
DRAWING NO
2518420
REV
C
SCALE
SHEET 5 OF 19

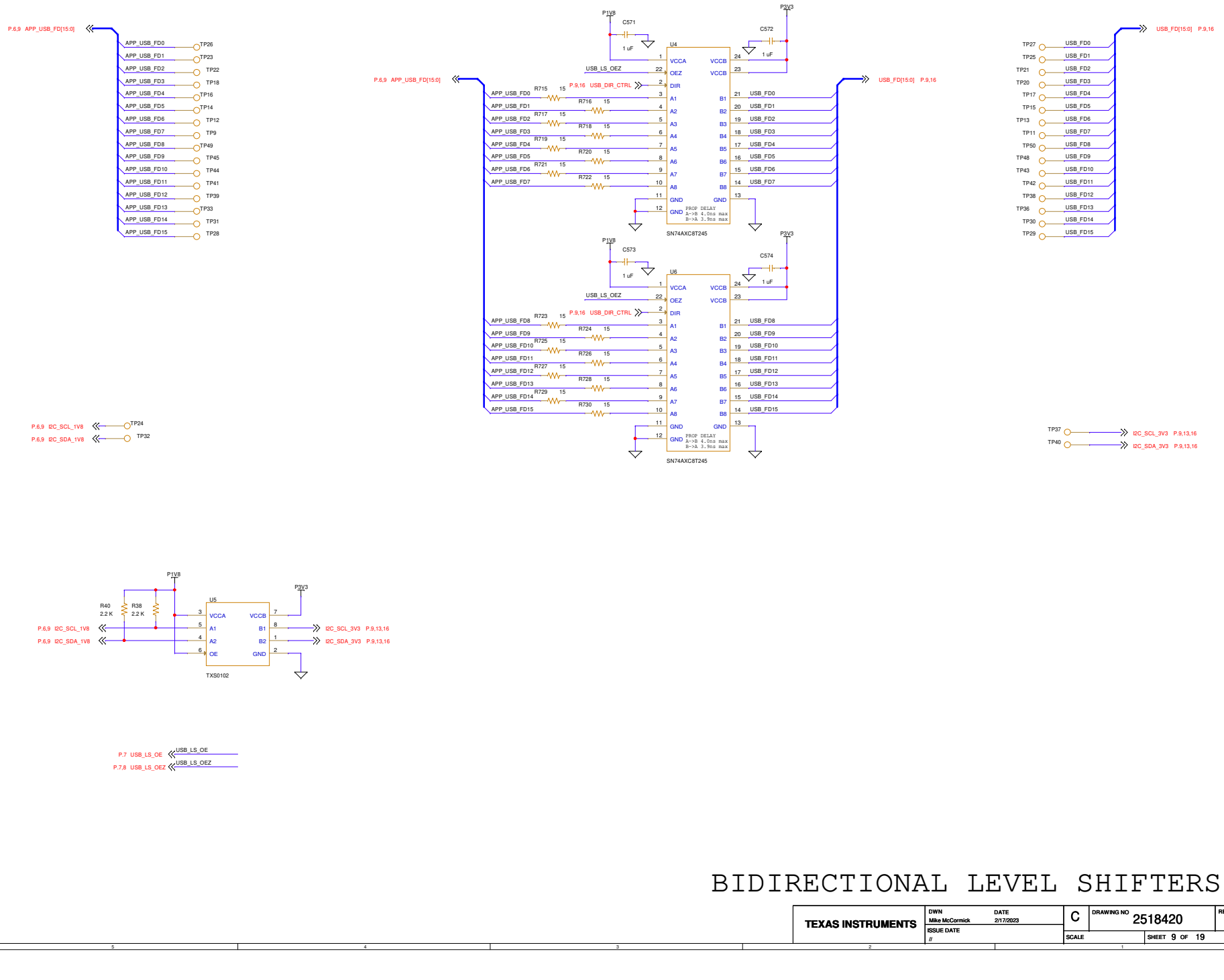

J500C
J500E
J500B
J500A
J500D
J500F
J3
FMC 400POS CONN MALE
P1V8
SW2
TP34
TP79
TP88
APP_STEPVCC
APP_FINISHED_IV
APP_ARSTZ
OUTPUT FROM APPS
APP_USB_FD[15:0] P.9
FMC2 TO VC707 APPLICATIONS FPGA
TEXAS INSTRUMENTS
DWN Mike McCormick
DATE 2/17/2023
ISSUE DATE //
C
DRAWING NO 2518420
REV C
SCALE
SHEET 6 OF 19


P1V8
P2V5
C525 1 uF
C528 1 uF
U503
SN74AVC16T245_DGG_48
1DIR
*1OE
1A1
1A2
1A3
1A4
1A5
1A6
1A7
1A8
2DIR
*2OE
2A1
2A2
2A3
2A4
2A5
2A6
2A7
2A8
VCCA
VCCA_1
VCCB
VCCB_1
GND
GND_1
GND_2
GND_3
GND_4
GND_5
GND_6
GND_7
PROP DELAY
A->B 3.7ns max
B->A 4.5ns max
C561 1 uF
C562 1 uF
U504
J22
P.6,7 APP_CTRL_RSTZ
P.8,9 USB_LS_OEZ
USB_LS_OEZ
USB_LS_OE
R90 0 DNI
R91 0
R501 0
R500 0 DNI
UNIDIRECTIONAL LEVEL SHIFTER
TEXAS INSTRUMENTS
DWN Mike McCormick
DATE 2/17/2023
ISSUE DATE //
C
DRAWING NO 2518420
REV C
SCALE
SHEET 7 OF 19



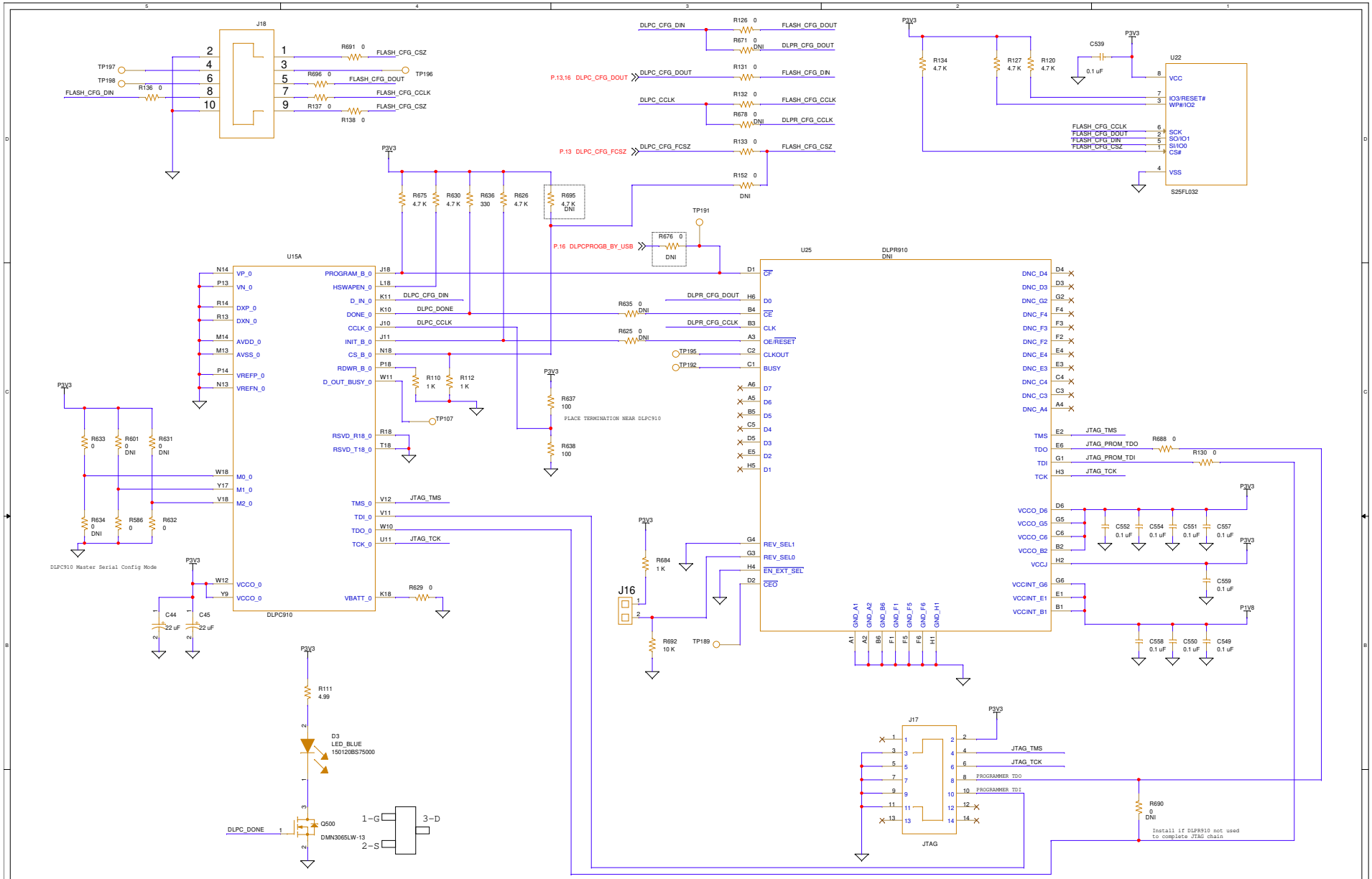
UNIDIRECTIONAL LEVEL SHIFTERS

TEXAS INSTRUMENTS	DWN Mike McCormick	DATE 2/17/2023	C	DRAWING NO 2518420	REV C
	ISSUE DATE //		SCALE	SHEET 8 OF 19	



BIDIRECTIONAL LEVEL SHIFTERS

TEXAS INSTRUMENTS	DWN Mike McCormick	DATE 2/17/2023	C	DRAWING NO 2518420	REV C
	ISSUE DATE //		SCALE	SHEET 9 OF 19	



To Configure DLPC910 Controller with SPI PROM:
- Remove R634 and install R633 to put the DLPC910 Controller into SPI Configuration Mode (M0=1, M1=0, M2=0)
- Install 0 ohm resistors into R126, R131, R132, R133.
- Install R134 with a 4.7K ohm resistor.
- Remove R671, R678, R635, R625.

DLPC910 CONFIG

TEXAS INSTRUMENTS	DWN Mike McCormick	DATE 2/17/2023	C	DRAWING NO 2518420 REV C
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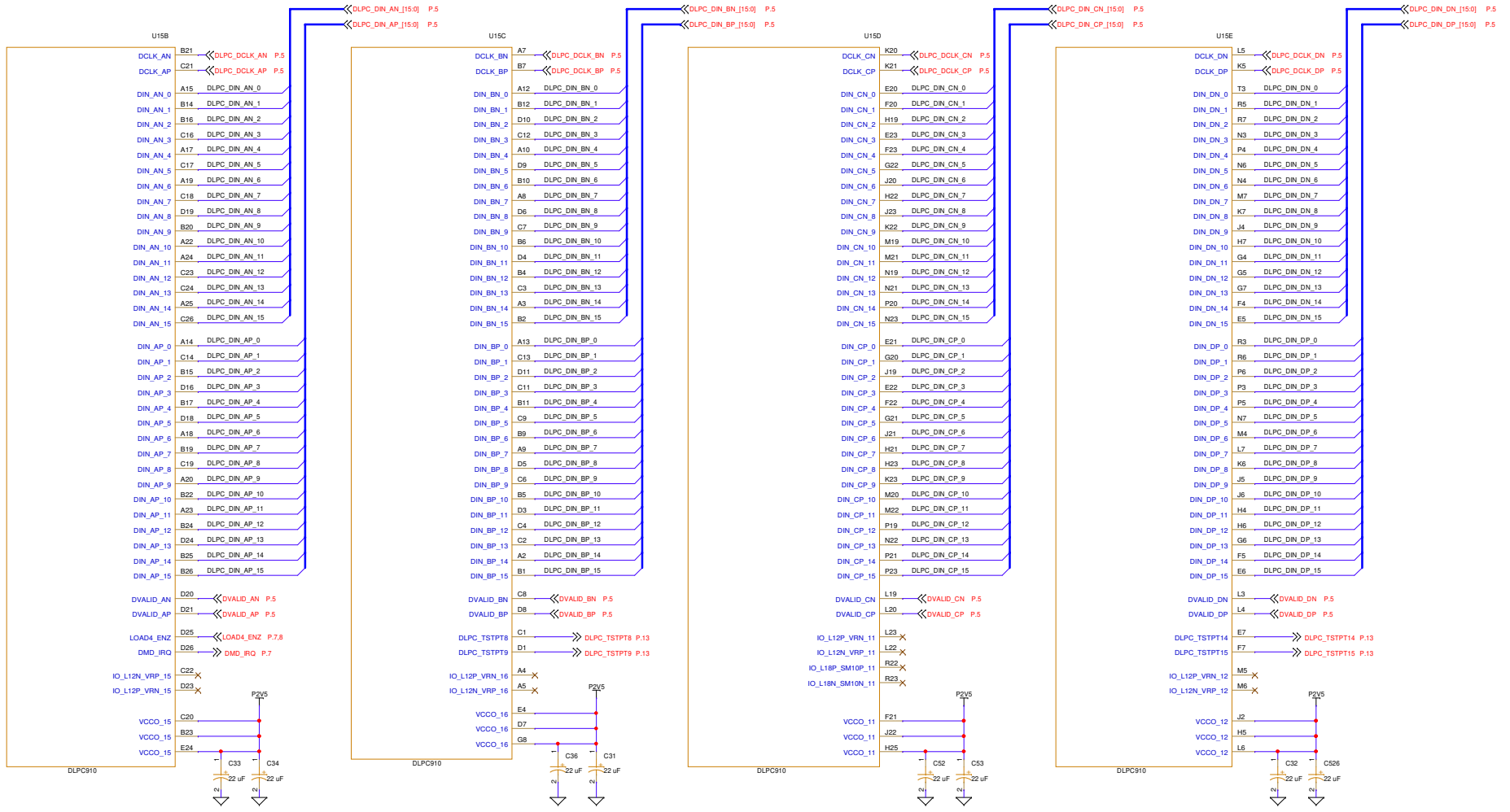
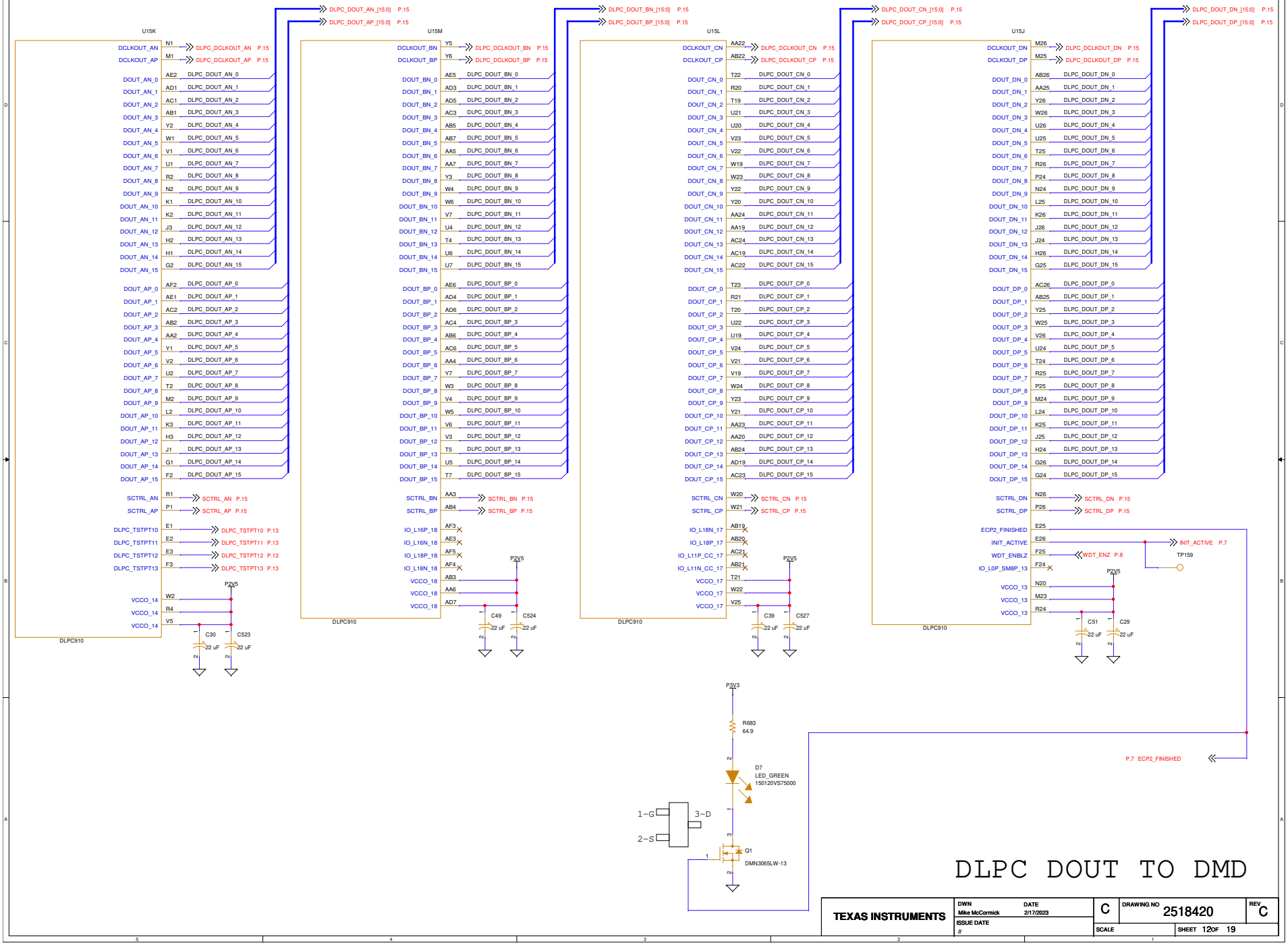


DLPC910 LVDS INPUTS NOT INTERNALLY TERMINATED
PLACE TERMINATION RESISTORS CLOSE TO DLPC910

DLPC DIN FROM APPS FPGA

TEXAS INSTRUMENTS	DWN Mike McCormick	DATE 2/17/2023	C	DRAWING NO 2518420	REV C
	ISSUE DATE //			SCALE	SHEET 11 OF 19


U15K
U15M
U15L
U15J
DLPC910
DLPC_DOUT_AN_[15:0] P.15
DLPC_DOUT_AP_[15:0] P.15
DLPC_DOUT_BN_[15:0] P.15
DLPC_DOUT_BP_[15:0] P.15
DLPC_DOUT_CN_[15:0] P.15
DLPC_DOUT_CP_[15:0] P.15
DLPC_DOUT_DN_[15:0] P.15
DLPC_DOUT_DP_[15:0] P.15
P2V5
P3V3
C30 22 uF
C523 22 uF
C49 22 uF
C524 22 uF
C39 22 uF
C527 22 uF
C51 22 uF
C29 22 uF
R683 64.9
D7 LED_GREEN 150120VS75000
Q1 DMN3065LW-13
TP159
INIT_ACTIVE P.7
WDT_ENBLZ P.8
P.7 ECP2_FINISHED
DLPC DOUT TO DMD
TEXAS INSTRUMENTS
DWN Mike McCormick
DATE 2/17/2023
ISSUE DATE //
C
DRAWING NO 2518420
REV C
SCALE
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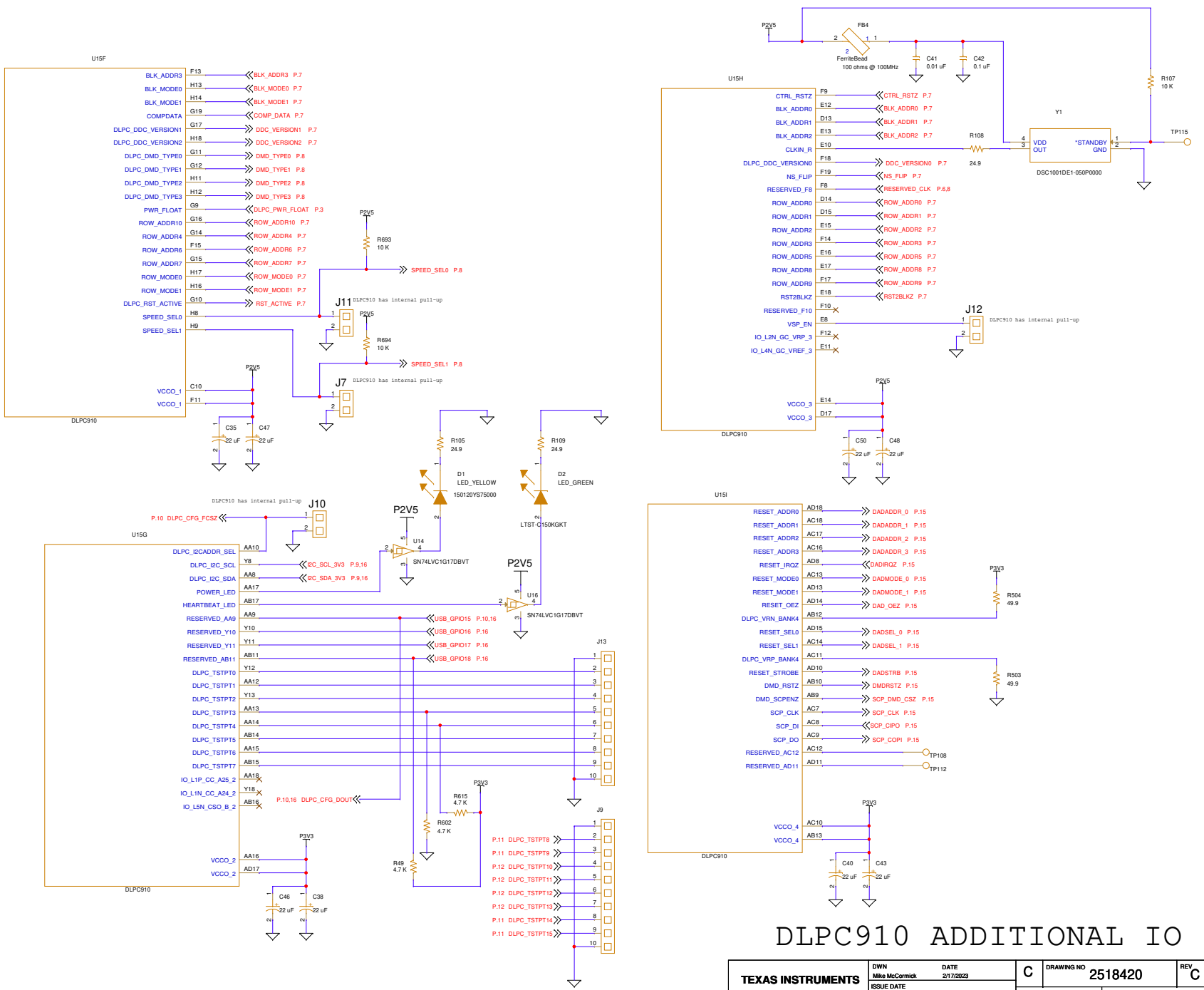

DLPC910 ADDITIONAL IO

TEXAS INSTRUMENTS	DWN Mike McCormick	DATE 2/17/2023	C	DRAWING NO 2518420	REV C
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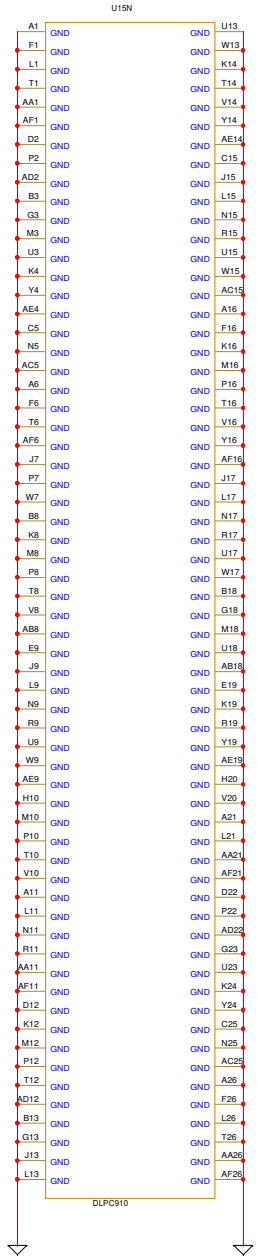
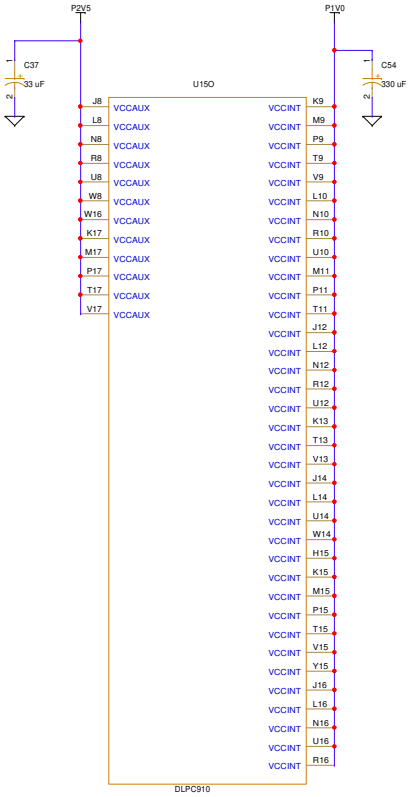
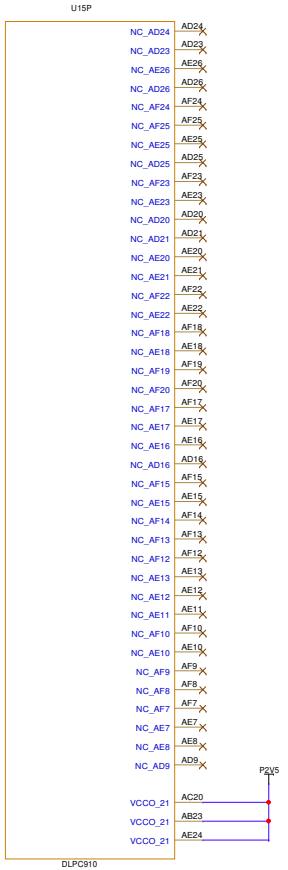
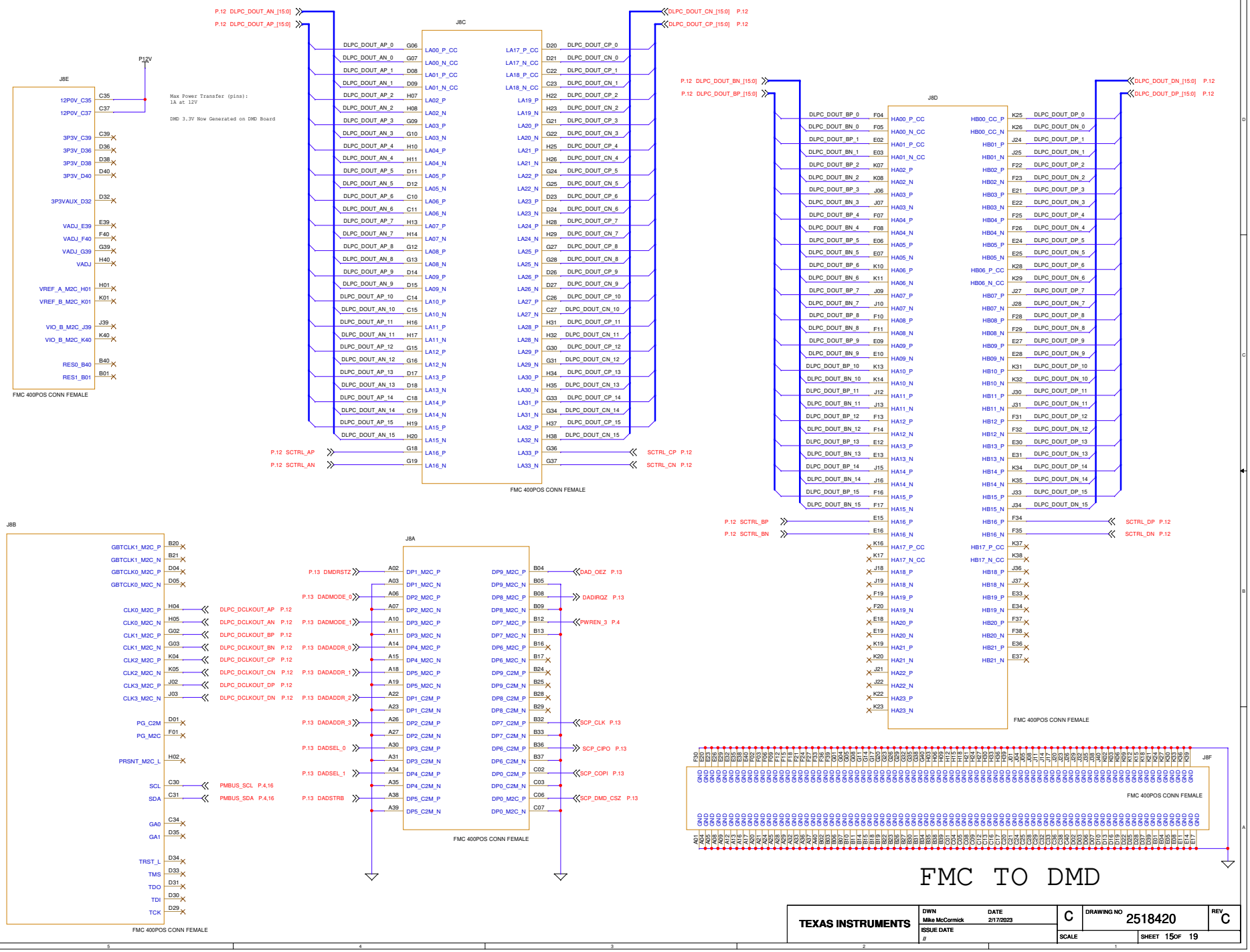






DLPC910 POWER, GROUND

TEXAS INSTRUMENTS	DWN Mike McCormick	DATE 2/17/2023	C	DRAWING NO 2518420 REV C
	ISSUE DATE //		SCALE	SHEET 14 OF 19


J8E
P12V
12P0V_C35
12P0V_C37
3P3V_C39
3P3V_D36
3P3V_D38
3P3V_D40
3P3VAUX_D32
VADJ_E39
VADJ_F40
VADJ_G39
VADJ
VREF_A_M2C_H01
VREF_B_M2C_K01
VIO_B_M2C_J39
VIO_B_M2C_K40
RES0_B40
RES1_B01
Max Power Transfer (pins):
1A at 12V
DMD 3.3V Now Generated on DMD Board
FMC 400POS CONN FEMALE
J8C
P.12 DLPC_DOUT_AN_[15:0]
P.12 DLPC_DOUT_AP_[15:0]
DLPC_DOUT_CN_[15:0] P.12
DLPC_DOUT_CP_[15:0] P.12
P.12 SCTRL_AP
P.12 SCTRL_AN
SCTRL_CP P.12
SCTRL_CN P.12
FMC 400POS CONN FEMALE
J8D
P.12 DLPC_DOUT_BN_[15:0]
P.12 DLPC_DOUT_BP_[15:0]
DLPC_DOUT_DN_[15:0] P.12
DLPC_DOUT_DP_[15:0] P.12
P.12 SCTRL_BP
P.12 SCTRL_BN
SCTRL_DP P.12
SCTRL_DN P.12
FMC 400POS CONN FEMALE
J8B
GBTCLK1_M2C_P
GBTCLK1_M2C_N
GBTCLK0_M2C_P
GBTCLK0_M2C_N
CLK0_M2C_P
CLK0_M2C_N
CLK1_M2C_P
CLK1_M2C_N
CLK2_M2C_P
CLK2_M2C_N
CLK3_M2C_P
CLK3_M2C_N
DLPC_DCLKOUT_AP P.12
DLPC_DCLKOUT_AN P.12
DLPC_DCLKOUT_BP P.12
DLPC_DCLKOUT_BN P.12
DLPC_DCLKOUT_CP P.12
DLPC_DCLKOUT_CN P.12
DLPC_DCLKOUT_DP P.12
DLPC_DCLKOUT_DN P.12
PG_C2M
PG_M2C
PRSNT_M2C_L
SCL
SDA
PMBUS_SCL P.4,16
PMBUS_SDA P.4,16
GA0
GA1
TRST_L
TMS
TDO
TDI
TCK
FMC 400POS CONN FEMALE
J8A
P.13 DMDRSTZ
P.13 DADMODE_0
P.13 DADMODE_1
P.13 DADADDR_0
P.13 DADADDR_1
P.13 DADADDR_2
P.13 DADADDR_3
P.13 DADSEL_0
P.13 DADSEL_1
P.13 DADSTRB
DAD_OEZ P.13
DADIRQZ P.13
PWREN_3 P.4
SCP_CLK P.13
SCP_CIPO P.13
SCP_COPI P.13
SCP_DMD_CSZ P.13
FMC 400POS CONN FEMALE
J8F
FMC 400POS CONN FEMALE
FMC TO DMD
TEXAS INSTRUMENTS
DWN Mike McCormick
DATE 2/17/2023
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C
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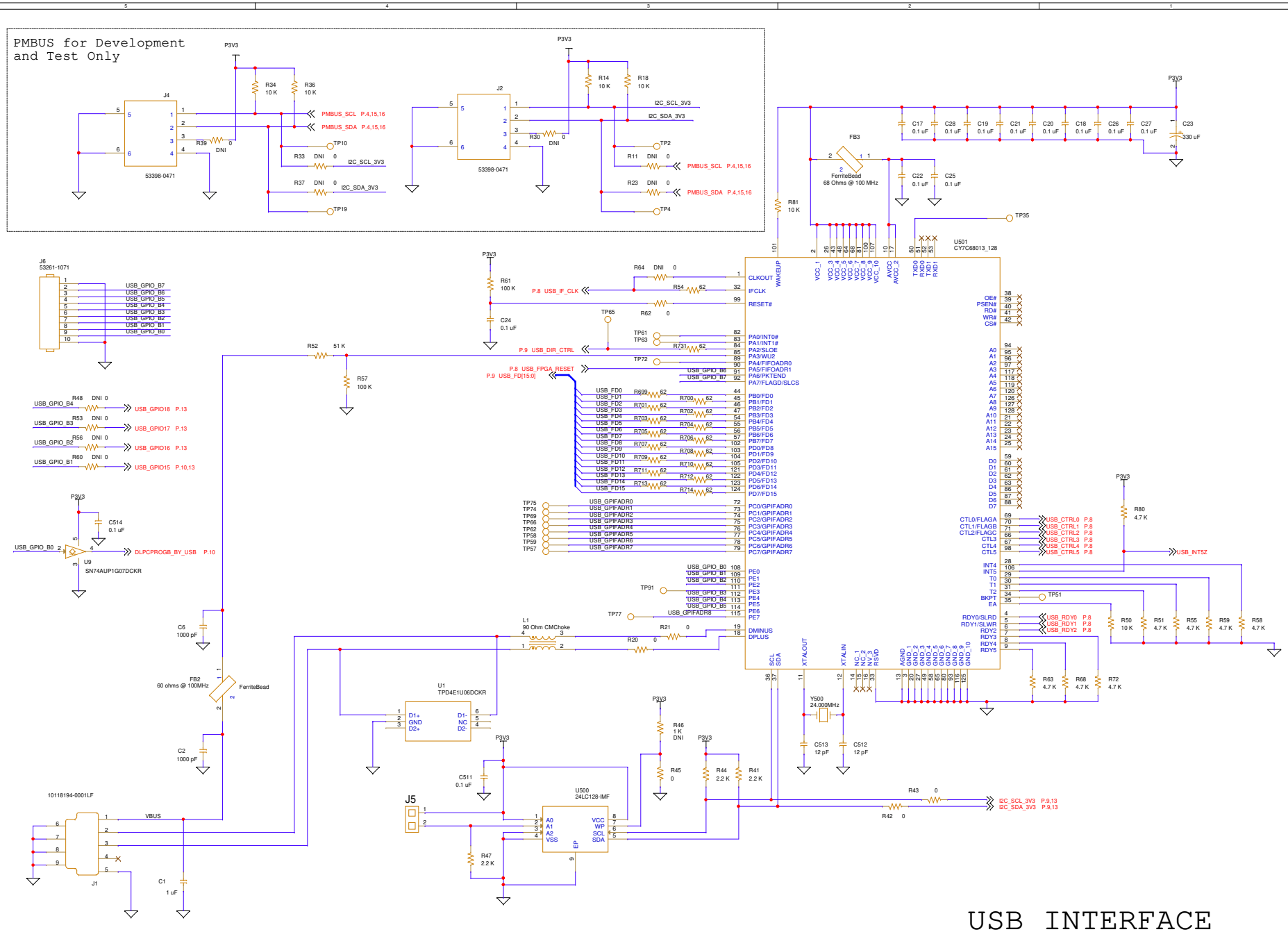
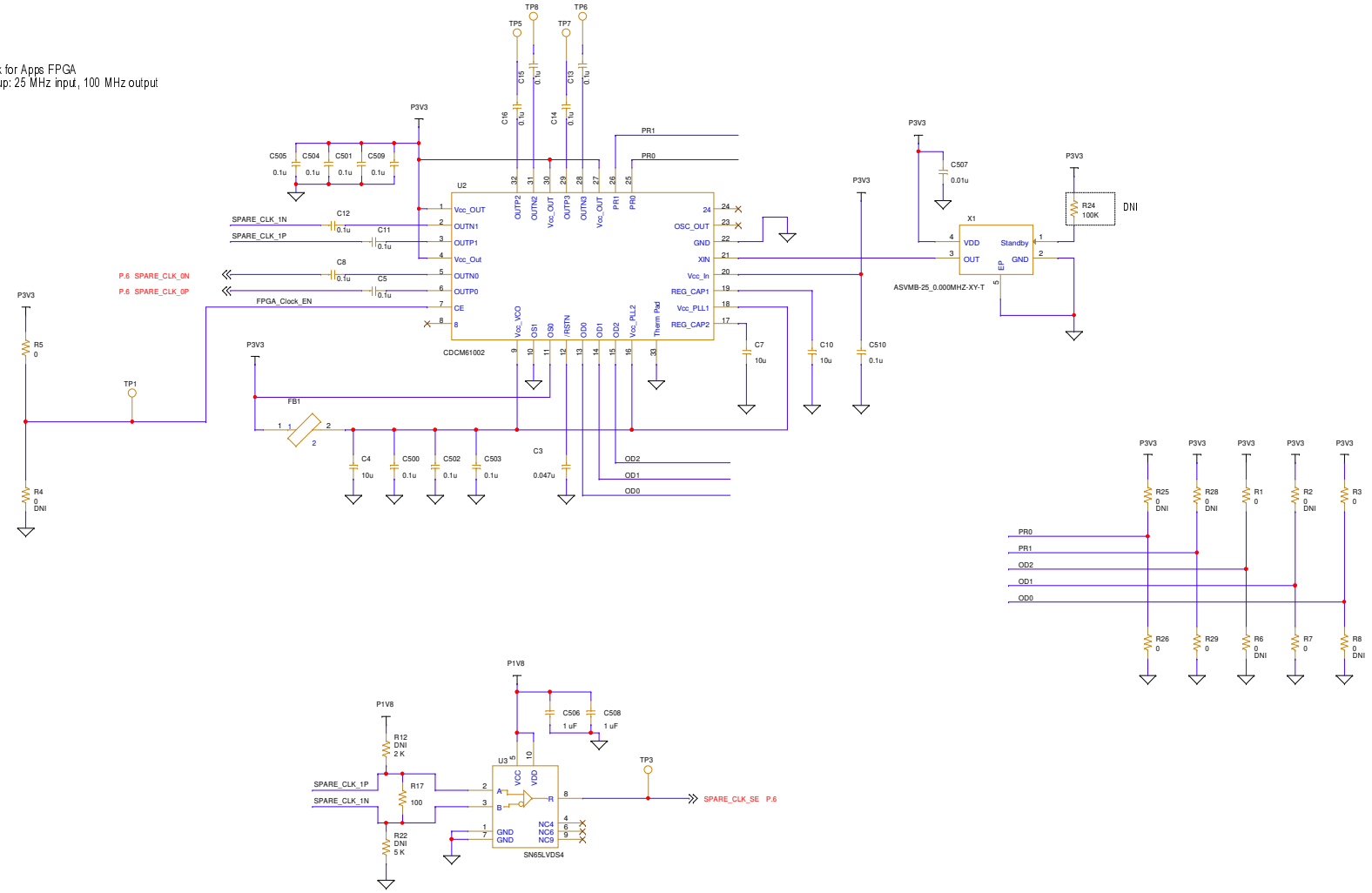


USB INTERFACE

TEXAS INSTRUMENTS	DWN Mike McCormick	DATE 2/17/2023	C	DRAWING NO 2518420	REV C
	ISSUE DATE //			SCALE	SHEET 16 OF 19

Spare Clock for Apps FPGA
Default Setup: 25 MHz input, 100 MHz output



SPARE CLOCK

TEXAS INSTRUMENTS	DWN Mike McCormick	DATE 2/17/2023	C	DRAWING NO 2518420	REV C
	ISSUE DATE //		SCALE	SHEET 17 OF 19	

Revision B:

-Changed D5 to 15V part
-Changed R655 to 4.64 KOhm
-Changed R668 to 6.81 KOhm
-Changed R654 to 6.74 KOhm
-Connected 1.8V to J501 pins J39 and K40.
-Added C560 to J501 pins J39 and K40.
-Added R692 to J16 pin 2
-Rotated D1 to connect Anode to U14 and Cathode to R105. Connected R105 to GND. D1 will illuminate when POWER_LED pin is 'High'.
-Connected J11 pin 1 to J500 pin D24 - Added R693 pullup to 2.5V - Passes SPEED_SEL0 status to APPS FPGA
-Connected J7 pin 1 to J500 pin H28 - Added R694 pullup to 2.5V - Passes SPEED_SEL1 status to APPS FPGA
-Changed D2, R109 to different values, logic high=on
-U8 changed from TXB0102DCUR to NLSX4014DTR2G, for higher throughput, added decoupling caps
-U4,U6,U7 changed from TXB0108DQSR to NLSX3018DTR2G, for higher throughput, added decoupling caps
-Changed 139 to 1k. Necessary for stronger pull on power float switch
-Routed SPEED_SEL0,1 through level shifter U11 to signals APP_SPEED_SEL0,1. Connected to FMC J500C pins D24,H28 respectively. Signals needed to be level shifted and sent to FPGA
-Changed net APP_USB_IF_CLK to connect to F04 instead of F05 on J500D (From N to P side). FPGA specifies this.
-J500C connector connected to APP_DMD_TYPE0, APP_DMD_TYPE1, APP_DMD_TYPE2, APP_DMD_TYPE3 instead of DMD_TYPE0, DMD_TYPE1, DMD_TYPE2, DMD_TYPE3. On C26,H35,H34,H22 respectively.
Signals needed to be level shifted
-R52 changed to 51k. Voltage divider was exceeding VIN max of Cypress device
-SN74AVC32T245NMJR was Split to 2 SN74AVC16T245DGGR. Extra decoupling caps added. Done for part supply reasons.
-A number of parts changed to alternates, some with new footprints
-Changed DLPC910 symbol, lines so that DOUT_CP_15 is on pin AC23, and DOUT_CN_15 is on pin AC22
-Changed SW3 to be toggle switch
-Added Jumper from APP_CTRL_RSTZ to 1.8V
-Connected to testpoints: ROW_ADDR8, ROW_ADDR9, ROW_ADDR10, ROW_MODE0, ROW_MODE1, BLK_ADDR0, BLK_ADDR1, BLK_ADDR2
-Changed R133 to Do Not Install
-Added a Not Installed 0k resistor between U15 pin N18 (CS_B_0) and U22 pin C2 (FLASH_CFG_CSZ)
-Added a Not Installed 4.7k pullup resistor on U15 pin N18 (CS_B_0)
-Changed R105 to 24.9 ohm
-Fixed TDO/TDI connections between DLPC910 (V11,W100) , J17 (p8,p10) and DLPR910 (E6,G1)
-Replaced U22 with S25FL128LAGMFM010
-Removed R123, not needed for S25FL128LAGMFM010
-Changed C533 to 06031A4R7CAT2A
-Changed Q1,Q500 to DMN3065LW-13

Revision C:

-Added R696
-Installed R134
-Connected J18 pin 5 to U22 pin 2 through R696
-Changed U4, U6, and U7 to SN74AVX8T245 level shifters
-Added R715 - R730 15 ohm resistors
-Added R699 - R714 62 ohm resistors
-Added USB_DIR_CTRL line to PA2 output of U501
-Removed U7, C575, and C576
-Added PWREN_3 connection to Pin B12 of J8A for 3.3V Power Enable on DMD Board
-Changed U22 to S25FL032 FLASH Device
-Changed GP1,GP2,GP3, and GP4 to 5001
-Changed C541 to CL10A474KB8NNNC
-Changed FB4 to MPZ1608S101ATDH5

REVISIONS

TEXAS INSTRUMENTS	DWN Mike McCormick	DATE 2/17/2023	C	DRAWING NO 2518420	REV C
	ISSUE DATE #		SCALE	SHEET 18 OF 19	

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IMPORTANT NOTICE

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	ISSUE DATE //			SCALE	SHEET 19 OF 19