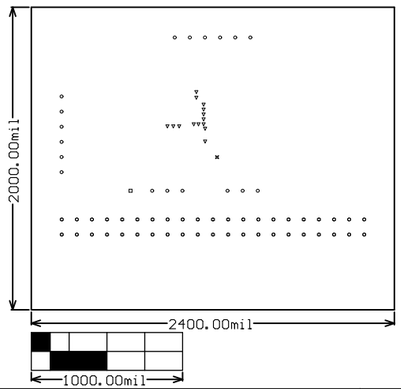
Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	0.40mil	3.5	
1	Top Layer		2.80mil		
	Dielectric1	FR-4 High Tg	56.40mil	4.8	
2	Bottom Layer		2.80mil		
	Bottom Solder	Solder Resist	0.40mil	3.5	



Symbol	Quantity	Finished Hole Size	Plated	Hole Type	Drill Layer Pair	Hole Tolerance
▽	14	8.00mil (0.203mm)	PTH	Round	Top Layer - Bottom Layer	
⌘	1	30.00mil (0.762mm)	PTH	Round	Top Layer - Bottom Layer	
⌖	42	40.16mil (1.020mm)	PTH	Round	Top Layer - Bottom Layer	
○	18	45.28mil (1.150mm)	PTH	Round	Top Layer - Bottom Layer	
□	1	63.00mil (1.600mm)	PTH	Round	Top Layer - Bottom Layer	
	76 Total					

DESIGN INFORMATION

MIN. TRACK WIDTH: 8 MIL
MIN. CLEARANCE: 6.69 MIL
MIN. VIA PAD SIZE: 24 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
☐ FR-408 ☒ FR-4 High Tg ☐ OTHER _____
THICKNESS: ☒ 62 MIL (1.6mm) +/-10% ☐ OTHER _____
TOLERANCE: ☒ ANSI IPC-6012 TYPE 3 CLASS 2
☐ OTHER +/- _____
BOW & TWIST: ☒ ANSI IPC-6012 TYPE 3 CLASS 2
☐ OTHER +/- _____

DRILLING:
REFERENCE: ☒ AS SHOWN ☒ NC_DRILL FILES
PTH COPPER THICKNESS: ☒ 20-30 um ☐ OTHER _____

BOARD FINISH:
SILKSCREEN: ☒ TOP ☐ BOTTOM
SILKSCREEN COLOR: ☒ WHITE ☐ OTHER _____
SOLDER RESIST COLOR: ☒ GREEN ☐ OTHER _____
☒ MATTE ☐ SEMI-GLOSS
SURFACE FINISH: ☒ IMMERSION GOLD (ENIG) ☐ ENEPIG
☐ IMM. TIN/SILVER OR EQUIV ☐ OTHER _____
ARRAY/PANEL: ☐ CUT AND TRIM PER M1 BOARD OUTLINE
☐ N.C. ROUTE ☒ V. SCORE
CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
☒ ANSI IPC-A-600F CLASS -> ☐ 1 ☒ 2 ☐ 3
☒ RoHS ☐ OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: ☐ YES
BARE BOARD ELEC. TEST: ☐ NONE ☒ REQUIRED ☐ PER ORDER
☐ XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
☐ XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
☐ OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
☐ LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE: TPS61299EVM-103
DESIGNED FOR: Public Release
FILE NAME: BMC103A.PcbDoc

ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: BMC103	REV: A	SVN REV: Not in version control
LAYER NAME = [illegible]ensions	TID #: N/A		
PLOT NAME = Fabrication Drawing	GENERATED : 3/16/2023 1:49:54 PM		TEXAS INSTRUMENTS

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ENGINEER:	LAYOUT BY:
Feng Ji	Wenhao Wu
SCALE: 1.00	ALTIUM DESIGNER VERSION: 23.2.1.34