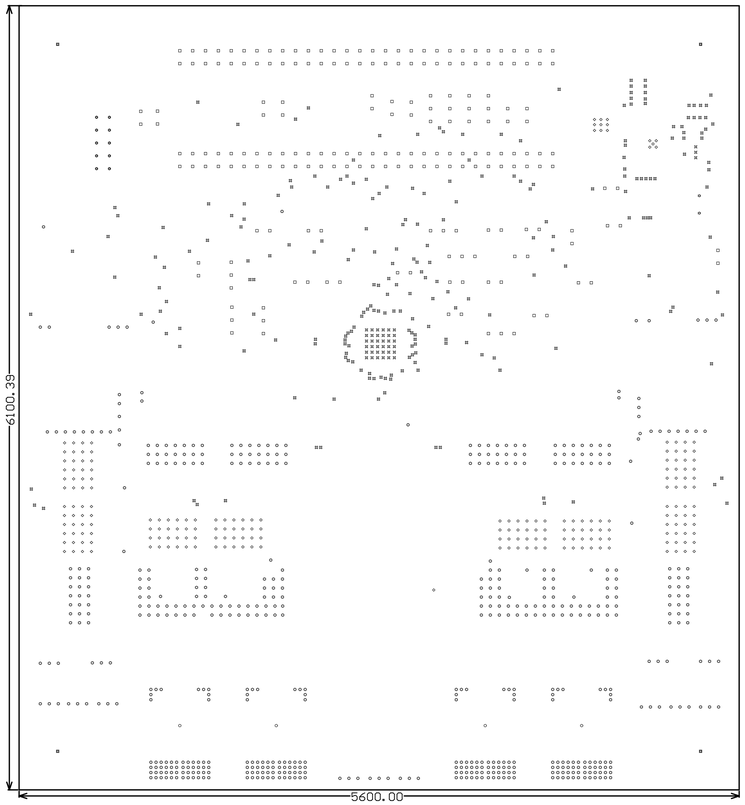
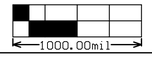
Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	0.40mil	3.5	
1	Top Layer		2.76mil		
	Dielectric1	FR-4 High Tg	5.00mil	4.8	
2	Signal Layer 1		2.76mil		
	Dielectric2	FR-4 High Tg	5.00mil	4.8	
3	Signal Layer 2		2.76mil		
	Dielectric3	FR-4 High Tg	5.00mil	4.8	
4	Signal Layer 3		2.76mil		
	Dielectric7	FR-4 High Tg	10.00mil	4.8	
5	Signal Layer 4		2.76mil		
	Dielectric4	FR-4 High Tg	5.00mil	4.8	
6	Signal Layer 5		2.76mil		
	Dielectric6	FR-4 High Tg	5.00mil	4.8	
7	Signal Layer 6		2.76mil		
	Dielectric5	FR-4 High Tg	5.00mil	4.8	
8	Bottom Layer		2.76mil		
	Bottom Solder	Solder Resist	0.40mil	3.5	
	Bottom Overlay				



Symbol	Count	Hole Size	Plated	Hole Type	Drill Layer Pair	Hole Tolerance
	39	7.87mil (0.200mm)	PTH	Round	Top Layer - Bottom Layer	
	207	8.00mil (0.203mm)	PTH	Round	Top Layer - Bottom Layer	
	229	10.00mil (0.254mm)	PTH	Round	Top Layer - Bottom Layer	
	570	16.00mil (0.406mm)	PTH	Round	Top Layer - Bottom Layer	
	2	37.99mil (0.965mm)	PTH	Round	Top Layer - Bottom Layer	
	10	40.00mil (1.016mm)	PTH	Round	Top Layer - Bottom Layer	
	204	45.28mil (1.150mm)	PTH	Round	Top Layer - Bottom Layer	
	4	125.98mil (3.200mm)	PTH	Round	Top Layer - Bottom Layer	
	4	270.00mil (6.858mm)	PTH	Round	Top Layer - Bottom Layer	
	1269 Total					



DESIGN INFORMATION

MIN. TRACK WIDTH: 8 MIL
MIN. CLEARANCE: 7.874 MIL
MIN. VIA PAD SIZE: 19.685 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
[ ] FR-4 [X] FR-4 High Tg [ ] OTHER _____
THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER _____
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/- _____
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/- _____

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER _____

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER _____
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER _____
[X] MATTE [ ] SEMI-GLOSS
SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER _____
ARRAY/PANEL: [ ] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [X] V. SCORE
CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER
ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
[X] 8 MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
[ ] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
[ ] LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE: LM5171EVM-BIDIR
DESIGNED FOR: Public Release
FILE NAME: BMC112A.PcbDoc

ENGINEER:	LAYOUT BY:
SCALE: 1.00	ALTIUM DESIGNER VERSION: 23.9.2.47

ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: BMC112	REV: A	SUN REV: Not in version control
LAYER NAME = [illegible]ensions			
PLOT NAME = Fabrication Drawing	GENERATED : 9/28/2023 7:32:43 PM		TEXAS INSTRUMENTS

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