

CLOCK-PERFDATA-DESIGN

Clock performance data and register settings for clock generators, network synchronizers, jitter cleaners, and other clocking devices.

Release Notes



Rev. 2024-11-22
22-Nov-2024

Document License

This work is licensed under the Creative Commons Attribution –NoDerivs 3.0 Unported License. To view a copy of this license, visit <http://creativecommons.org/licenses/by-nd/3.0/> or send a letter to Creative Commons, 171 Second Street, Suite 300, San Francisco, California, 94105, USA.

Copyright © 2024 Texas Instruments Incorporated - <https://www.ti.com/>

Contents

1	Overview.....	4
2	Licensing.....	4
3	Documentation.....	4
4	Device Support.....	4
5	Supported Features.....	5
5.1	Version 2024-11-22.....	5
5.2	Version 2024-11-19.....	5
6	Known Issues.....	5
7	Technical Support and Product Updates.....	5
8	Release History.....	5

Release Notes

CLOCK-PERFDATA-DESIGN

Release 2024-11-22

1 Overview

This document is the Release Notes of the CLOCK-PERFDATA-DESIGN site. This release gives list of features/known issues of every release.

2 Licensing

Please refer to the software manifest which outlines the licensing status for all packages included in this release.

3 Documentation

- **.tcs files:** Provides the TICS Pro v1.7.7.6 configuration file for the setup.
- **.txt files:** Provides the raw output phase noise data exported from the Keysight E5052A or E5052B phase noise analyzer.
- **.png files:** Provides the output phase noise plot capture or setup diagram. Refer to the file name for content detail.

4 Device Support

The devices supported with this release include (new devices are bolded):

Supported Devices
LMK5C33216A
LMK5B33216

5 Supported Features

5.1 Version 2024-11-22

- Added Configuration Files and Data
 - LMK5B33216
 - LMK5B33216_ConfigurationAndData_REF_is_25MHzSML01_XO_is_48MHz LMK6C_OUT_is_625MHz
 - DPLL reference = 25 MHz from SML01
 - XO input = 48 MHz from SMB100A
 - Output = 625 MHz
 - Data contains phase noise plots with and without 4 MHz high-pass (HPF) applied
 - LMK5B33216_ConfigurationAndData_REF_is_25MHzSML01_XO_is_48MHz SMB100A_OUT_is_625MHz
 - DPLL reference = 25 MHz from SML01
 - XO input = 48 MHz from LMK6C oscillator
 - Output = 625 MHz
 - Data contains phase noise plots with and without 4 MHz high-pass (HPF) applied

5.2 Version 2024-11-19

- First release
- Added Configuration Files
 - LMK5B33216
 - LMK5B33216_Configuration_ROM0_to_ROM8.zip
 - LMK5C33216A
 - LMK5C33216A_Configuration_ROM0_to_ROM8

6 Known Issues

None

7 Technical Support and Product Updates

Please post questions for support on to the TI E2E Community at <https://e2e.ti.com/support/clocks/>

8 Release History

Doc No.	Version	Description	Release Date
2	2024-11-22	Added LMK5B33216 configuration files and data	22 Nov 2024
1	2024-11-19	First Release Added LMK5B33216 configuration files	19 Nov 2024