



PLLatinum Sim User Guide

Last Updated 5/16/2025

Document Revision History

| Date | Author | Descriptions |
|-----------|---------------|---|
| 1/30/2022 | Dean Banerjee | Initial Document Created |
| 4/4/2022 | Dean Banerjee | Updated Active Filter Information Updated N Divider Fractional Settings Updated Spur Section |
| 8/29/2022 | Dean Banerjee | Added cascaded simulation descriptions. |
| 4/21/2023 | Dean Banerjee | Updated discrete lock time modeling descriptions. Added updates for Fastlock, update pictures for phase noise & filter |
| 4/1/2024 | Dean Banerjee | Added cascade noise analysis |
| 5/16/2025 | Dean Banerjee | Updated phase noise for UsePoints option |

Table of Contents

| | | |
|----------|--|-----------|
| 1 | HIGH LEVEL OVERVIEW | 5 |
| 1.1 | SCOPE OF PLLATINUM SIM | 5 |
| 1.2 | TYPICAL SIMULATION ACCURACY | 5 |
| 1.3 | FEATURE LEVEL | 6 |
| 1.4 | TOOL TIPS AND WARNING BOXES | 7 |
| 1.5 | OTHER RESOURCES THAT INTERACT WELL WITH PLLATINUM SIM | 7 |
| 1.6 | HELP BOXES WITH BUILT IN HELP | 7 |
| 2 | MENU OPTIONS | 9 |
| 2.1 | FILE | 9 |
| 2.2 | OPTIONS | 9 |
| 2.3 | DATA EXPORT | 9 |
| 2.4 | RESOURCES | 9 |
| 2.5 | HELP | 9 |
| 3 | SELECT DEVICE TAB | 10 |
| 3.1 | OPTIONALLY ENTER THE FREQUENCY, DEVICE TYPE, FEATURES, AND USE SCROLL BARS | 10 |
| 3.2 | CLICK ON THE DEVICE, CONFIGURE THE DEVICE, CASCADE NOISE IF DESIRED AND PRESS “LOAD DEVICE” BUTTON | 10 |
| 4 | MAIN DIAGRAM | 11 |
| 4.1 | MENU OPTIONS FOR MAIN DIAGRAM | 11 |
| 4.2 | FEATURE LEVEL, MAX CALCULATION TIME, AND LOOP GAIN CHANGE | 11 |
| 4.3 | N DIVIDER FRACTIONAL SETTINGS | 12 |
| 5 | FILTER DESIGNER TAB | 13 |
| 5.1 | DESIGN TIPS AND SIMULATION SHOWN | 13 |
| 5.3 | FILTER ORDER AND FILTER TYPE | 14 |
| 5.4 | FILTER TYPE | 14 |
| 5.5 | FILTER PARAMETERS | 15 |
| 5.6 | RESTRICT COMPONENTS | 16 |
| 5.7 | THE ADVANCED OPTIMIZER | 18 |
| 6 | PHASE NOISE TAB | 20 |
| 6.1 | PHASE NOISE TIPS | 21 |
| 6.2 | LOADING PHASE NOISE TRACES | 21 |
| 6.2.1 | GENERAL METHOD OF LOADING PHASE NOISE TRACES | 21 |
| 6.3 | GRAPH SETTINGS & COMPARISON TRACE | 21 |
| 6.4 | TOTAL PHASE NOISE AT OFFSETS | 22 |
| 6.5 | CROSSOVER METRICS | 22 |
| 6.6 | INTEGRATED NOISE AND OTHER NOISE METRICS | 22 |
| 6.7 | OTHER NOISE SOURCES | 22 |
| 6.8 | OSC, PLL, AND VCO NOISE | 23 |
| 6.8.1 | DISABLE OPTION | 23 |
| 6.8.2 | USE METRICS OPTION | 23 |
| 7 | SPURS TAB | 25 |
| 7.1 | SPUR CHART AND DECOMPOSITION CHART | 25 |
| 7.2 | SPUR TIPS AND GRAPH SETTINGS | 26 |
| 7.3 | SPURS BOX | 26 |
| 7.4 | INTEGRATED SPUR METRICS | 26 |
| 7.5 | SPUR MECHANISMS | 26 |
| 7.6 | SPUR DIAGNOSTICS | 27 |
| 7.7 | MASH SEEDS | 27 |

| | | |
|----------|---|-----------|
| 8 | LOCK TIME TAB | 28 |
| 8.1 | LOCK TIME FREQUENCY AND PHASE CHART | 29 |
| 8.2 | LOCK TIME TIPS | 29 |
| 8.3 | GRAPH SETTINGS AND COMPARISON TRACE | 30 |
| 8.4 | VCO CALIBRATION TIME | 30 |
| 8.5 | PHASE RESPONSE BOX | 30 |
| 8.6 | DISCRETE TIME MODELING OF LOCK TIME | 31 |
| 8.6.1 | TRANSIENT PHASE RESPONSE FOR DISCRETE MODELING OF LOCK TIME | 32 |
| 8.6.2 | NONLINEAR MODELING OF THE CHARGE PUMP | 33 |
| 8.7 | FASTLOCK | 35 |
| | | |
| 9 | BODE PLOT TAB | 36 |
| 9.1 | GRAPH AND POLES AND TIME CONSTANTS | 36 |

1 High Level Overview

1.1 Scope of PLLatinum Sim

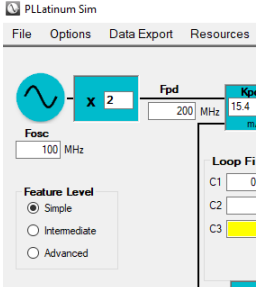
- **Select Devices** by specifying criteria such as output frequency, required features, device type, current, chip area, and noise performance. These criteria are focused on the PLL in the device. At the time of these instructions being written, buffers & divider buffers are just starting to be added. The device selection is focused on the PLL portion of integrated devices. For instance, for a device with integrated PLL + Mixer (LMX8410L), the tool only focuses on the PLL portion of this device
- **Set Up Devices** on the main setup tab. This includes frequencies, charge pump current, option to manually enter loop filter components, and more. There is some feedback given regarding frequencies and divider ranges if they are not legal for a device, but the diagram is a high-level abstracted view of the device and does not include the full complexity of devices. In order to see the full detail of a device, use the Texas Instruments TICSPRO tool that has more detailed device level diagrams and also generates registers
- **Design Loop Filter** based on loop bandwidth and optionally parameters such as phase margin, gamma, and pole ratios. An advanced optimizer also can design based on optimizing one parameter subject to constraints, such as designing for the lowest possible jitter subject to the constraint that the phase noise at 1 MHz offset is -120 dBc/Hz or better
- **Simulate Loop Filter** for phase noise, spurs (including fractional spurs), lock time (including VCO calibration options for discrete time modeling), and bode plot. The simulations are very powerful and based on mathematical models that use performance indices that are extracted from actual measurement during characterization of the device.

1.2 Typical Simulation Accuracy

The actual performance can vary from the simulation and can also vary over process, voltage, and temperature. There will be some mismatch between simulation and actual and this can vary significantly based on setup conditions. ***This table is only a rough estimate and simulation accuracy results will vary with setup and with the device being simulated.***

| Tab | Parameter | Typical Simulation Accuracy | Common Factors Leading to Simulation Accuracy Greater than Stated Value |
|---------------|----------------------|-----------------------------|---|
| Filter Design | Loop Bandwidth | <10% | <ul style="list-style-type: none">• VCO gain, charge pump gain, or loop filter components stated in simulation not matching the actual values• For active filters, non-ideal op-amp properties |
| Phase Noise | Spot phase noise | <2 dB | <ul style="list-style-type: none">• Input reference noise not entered correctly or not at all• Slow slew rate on input reference• VCO high order capacitor too small (tool gives warning) |
| Spurs | All spurs | <15 dB | <ul style="list-style-type: none">• Slow slew rate on input reference• Crosstalk on board/power supply• Multiple factors not modeled impacting spur at same offset• Comment: Simulation/Actual mismatch can vary wildly based on spur type and setup. For a given spur and setup, variation is typically <5 dB, but spurs are very sensitive to setup, and PLLatinum Sim does not model all of this |
| Lock Time | VCO Calibration Time | <15% | <ul style="list-style-type: none">• VCO programmable settings• Board/supply pin crosstalk• The models themselves. |
| | Analog Lock time | <15% | <ul style="list-style-type: none">• Mismatch for Kvco, Kpd, or components• Railing at power supply• Discrete phase detector sampling action• Dielectric absorption in capacitors |

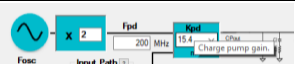

1.3 Feature Level

| | |
|---|--|
|  | <p>The Feature Level allows the user to select the details shown. Selection the Advanced option will show the maximum details, although this may be overwhelming to the user. For this reason, there are also the Intermediate and Simple feature levels that hide details and make assumptions about the parameters that are hidden. In the Simple feature level, far less details are shown and assumptions are made about parameters that are not show.</p> |
|---|--|

| What | Basic Feature Level | Intermediate Feature Level | Advanced Feature Level |
|---------------------|--|--|---|
| Menu Bar | Load/Save Design, Import from TICSPRO, Options for Main Diagram and Filter Designer Tab, Export Design to Excel and traces as text files, Links to help and product folders and E2E. | | |
| Part Selection Tab | Selects the device based on frequency, device type, and features | Allows use to also screen based on current, PLL figure of merit, VCO figure of merit, and Package size | |
| Main Diagram | Set up the frequencies and settings for the selected device | VCO Core selection | Fractional Settings and input path Input Path |
| Filter Designer Tab | Design loop filter based on loop bandwidth. Allows passive and active filters and theoretical ideal filters | Also choose loop bandwidth | Choose pole ratios and gamma optimization factor. Advanced filter optimizer. |
| Phase Noise Tab | Model phase noise and jitter. Set up graph and integration limits. Graph phase noise based on causes. | Phase noise import, other integrated noise metrics, spot phase noise | Distribution path noise, VCO noise metric override |
| Spurs tab | Graph setup | Integrated spur metrics | MASH_Seed, Spur mechanisms, spur decomposition chart |
| Lock Time Tab | Graph Setup Analog Lock time VCO Calibration | VCO Calibration Start | Lock Time to Phase Discrete Lock Time modeling |
| Bode Plot Tab | Graph Setup | Parameters Spot Metrics | Closed Loop Parameters |

Pictures in this document are shown using the Advanced Feature Level in order to show all of the capability. Realize that in Basic or Intermediate Feature Level, some features will not be visible.

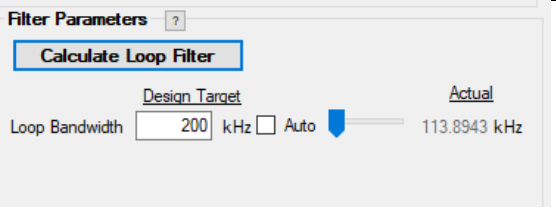
1.4 Tool Tips and Warning Boxes

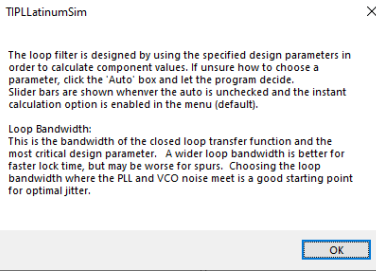
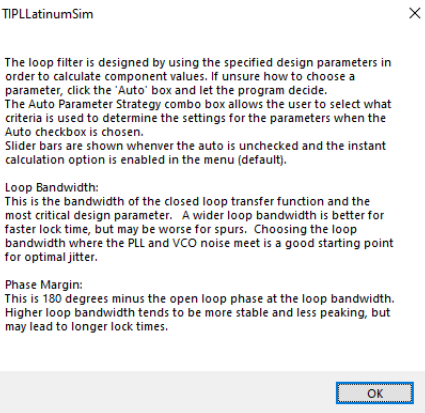
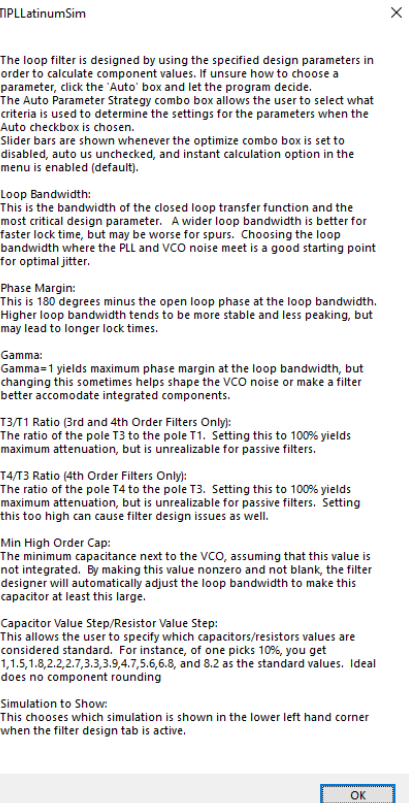
| | |
|---|--|
|  | <p>Several controls and entry boxes will show tool tips when the mouse pointer hovers over them.</p> |
|  | <p>Boxes that change yellow means there is a warning, red means a more severe warning. Mouse over the box to see the warning. If no warning message appears, try selecting the box and pressing <enter>.</p> |

1.5 Other Resources that Interact well with PLLatinum Sim

- *PLL Performance, Simulation, and Design* by Dean Banerjee includes formulas and concepts that PLLatinum Sim is based off of
- The Texas Instruments TICSPRO tool is excellent for configuring registers and PLLatinum Sim supports importing TICSPRO files for many Texas Instruments devices

1.6 Help Boxes with Built in Help

| | |
|---|--|
|  | <p>The PLLatinum Sim tool is being upgraded often and it includes useful, context sensitive built in help based on the user level settings of the device. The tool may be updated after these instructions are created, but the online help will get upgraded with the tool. There are a great many concepts that are not obvious.</p> <p>Do NOT forget to click on the "?" for help!</p> |
|---|--|

| Simple Feature Level | Intermediate Feature Level | Advanced Feature Level |
|---|--|---|
|  |  |  |

Many of these help boxes have very comprehensive and context sensitive help. There are many concepts that are complicated that are explained in these text boxes. The help box for the N divider is a good example.

The screenshot shows the PLLatinum Sim software interface. The main window displays a block diagram of a PLL system. Key components include an input signal, a phase-locked loop (PLL) block, and an N divider block. The N divider block is highlighted, and a help box titled "TIPLLatinumSim" is open, providing detailed information about the fractional settings.

TIPLLatinumSim Help Box Content:

Fnum and Fden:
This is the fractional numerator and fractional denominator, respectively. In general, lowest term fractions are best for simulation and the program will try to find one if the VCO frequency is changed (this can be disabled in the menu options). Avoid unnecessarily large fractions to represent randomization. In other words do not enter fractions like 419430/4194301 to simulate a fraction of 1/10 with a large amount of randomization.

Fractional Order:
The fractional order can improve the primary fractional spurs at the expense of creating extra sub-fractional spurs.

Randomization:
Randomization reduces sub-fractional spurs at the expense of adding PLL phase noise. It is a mathematical concept representing how well the fraction is randomized; it is NOT a single programmable setting in the device, but the combination of the fraction, modulator order, and dithering settings.

Although it can vary in degree, most applications can be modeled with just the two cases of unrandomized (Randomization = 0%) and perfectly randomized (Randomization = 100%). Settings in between this are to allow the user to use the slider bar to get a visual understanding of what randomization does to spurs and phase noise, but typically not needed for design values.

Consider the setting to be perfectly randomized if (1) reduced fraction has a denominator greater than 1000000, (2) fraction has denominator greater than 1000 and dithering mode is enabled, or (3) fractional denominator is greater than 1000000 and the programmable seed value is nonzero.

For example, fraction of 1/10 is 0% randomization. Fraction of 1000000/1000001 is expressed in this tool a fraction of 1/10 with 100% randomization. The fraction expressed in lowest terms has a denominator greater than 1000000 or a dithering mode is enabled. Otherwise consider as unrandomized. For instance, a fraction of 1/10 is unrandomized, a fraction of 1000000/1000001 is expressed in this tool as a fraction of 1/1000 with randomization of 100%. A fraction of 1000000/1000000 would be modeled as a fraction of 1/10 with 0% randomization if there is no dithering mode or initial state (MASH_SEED) or 100% if it was.

Specific Comments to this Setup:

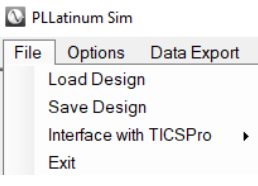
Simplified Fraction: 341/1000
Simplified Fractional Denominator: 1000

-the simplified fractional denominator is divisible by 2, but not 3. Therefore the 3rd order modulator will have the same 1/2 sub-fractional spurs. However, the 4th order modulator will have 1/4 sub-fractional spurs.

OK

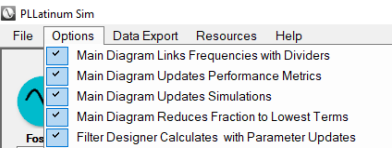
2 Menu Options

2.1 File

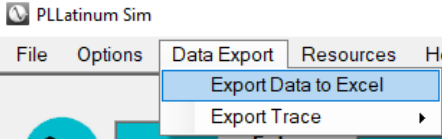
| | |
|---|--|
|  | <p>Load Design/Save Design allows a file to be loaded or saved in a *.sim format (a format specific to PLLatinum Sim). If an older version of a saved file is detected, then PLLatinum Sim will convert it and alert the user</p> <p>Interface with TICSPRO allows a TICSPRO file (*.tcs format) to be imported so that the frequencies, formats, charge pump current, and other features mainly on the main setup screen can be updated. There is also an option to “Add Filter to TICSPRO”. This option just adds the loop filter information to the *.tcs file from TICSPRO. So that a single file can have the loop filter information and programmable settings. However, this does nothing special when it is loaded in TICSPRO.</p> |
|---|--|

2.2 Options

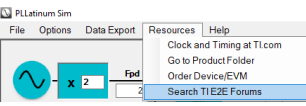
These options are straightforward and many of them have been already discussed. Then can be enabled or disabled.

| | |
|---|---|
|  | <p>Main Diagram ... The top four options apply to the main diagram. The defaults are that it updates frequencies, performance, simulations, and fractions to lowest terms. But sometimes this is undesirable, so this feature can be disabled.</p> <p>Filter Designer Calculates with Parameter Updates will automatically calculate the loop filter when a parameter is changed without requiring the user to press the “Calculate Loop Filter” button</p> |
|---|---|


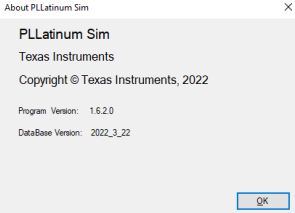
2.3 Data Export

| | |
|---|--|
|  | <p>Export to Excel exports the whole design into one elegant workbook with separate tabs for each tab. As a bonus, it gives some additional information not in the GUI, such as the MASH sequence for fractional dividers</p> <p>Export Trace exports phase noise and lock time traces as text files</p> |
|---|--|

2.4 Resources

| | |
|---|--|
|  | <p>The resources menu option has links to product folders and websites. The Search TI E2E forums option automatically goes to the Texas Instruments E2E (Engineer to Engineer) website and searches for posts on the currently selected device.</p> |
|---|--|

2.5 Help

| | | |
|---|---|--|
|  |  | <p>Help-> Users Guide opens the users guide from the program.</p> <p>Help->About option displays the program version information. The program version gives an indication of when the source code of the program was updated. There is also a database version that indicates when the database was updated as it is possible for the PLLatinum Sim database to be updated without updating the source code.</p> |
|---|---|--|

3 Select Device Tab

3.1 Optionally enter the frequency, device type, features, and use scroll bars

Select DeviceFilter DesignerPhase NoiseSpursLock TimeBode Plot

Specify Device Selection Criteria

Frequency

Fixed

Tunable

5541 MHz

Clear Filters

Choose Device Type

All Devices

Click Required Features

5V Charge PumpDistribution ModeFractional PLLIntegrated VCOExternal VCO OptionMultiple OutputMultiple PLLHero Device

Select a Device

LMX2572LMX2572LP
LMX2592
LMX2594
LMX2595
LMX2615
LMX2694
LMX2820
LMX8410L
Custom

Device Description

Wideband Synthesizer (45-22600 MHz)

PLL Description:
PLL(VCO1)

VCO Description:
Multicore VCO

Output Description:
Dual Differential Open Drain Outputs

☐ Cascade Noise from Previous Device

Configure Device

PLL(VCO1)
VCO1

Load Device

To search devices, a fixed or tunable frequency may be entered, but is not required. It is also possible to use the slider bars to screen for current, PLL figure of merit, VCO figure of merit, or package size. Using these tools, one can quickly narrow down the device choices for the application.

3.2 Click on the device, configure the device, cascade noise if desired and press “Load Device” button

Select a Device

LMX2572
LMX2572LP
LMX2592
LMX2594
LMX2595
LMX2615
LMX2694
LMX2820
LMX8410L
Custom

Device Description

Wideband Synthesizer (45-22600 MHz)

PLL Description:
PLL(VCO7)

VCO Description:
Multicore VCO

Output Description:
Dual Differential Open Drain Outputs

☐ Cascade Noise from Previous Device

Configure Device

PLL(VCO7)
VCO7

Load Device

When a device is clicked on, the configure device box may appear and it may show different options. A default option is selected, but can be changed. This default is based on choosing a PLL and VCO core that hits the desired frequencies. For multi-core VCO devices, one can select the core. For devices with more than one PLL, you can choose which PLL. Be sure this is the correct PLL before you press the “Load Device” button.

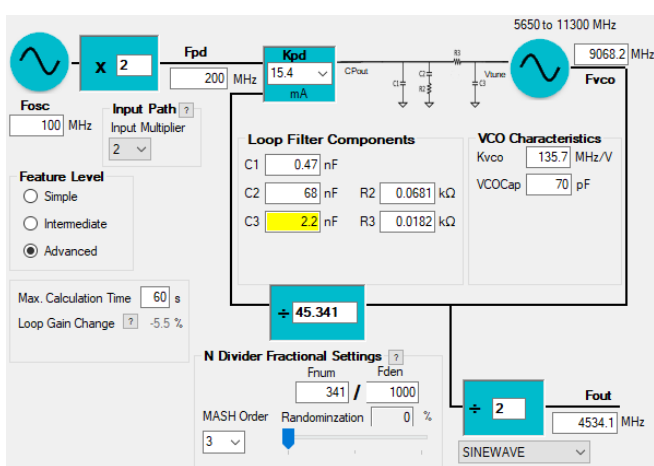
For dual PLLs or dual loop jitter cleaners, be sure the desired PLL is selected. You can only simulate one PLL at a time.

☒ Cascade Noise from Previous Device

Load Device

If the “Cascascade Noise from Previous Device” option is checked a the time that the <Load Device> button is pressed, then phase noise and frequency for the output at the time before the <Load Device> button was pressed becomes the frequency and imported phase noise for the new Fosc frequency after the <Load Device> button is pressed.

4 Main Diagram



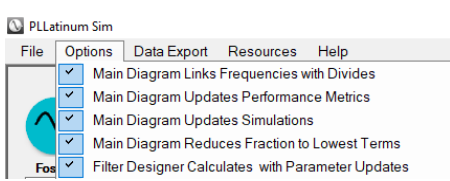
Frequencies, loop filter component values, charge pump gain, divide/multiply values, VCO characteristics, and N divider settings can be entered in the white boxes. Output format, input multiplier, and charge pump gain (also can be directly entered) can be selected from a list of options. Divide and multiply signs can be toggled by clicking on them.

When the loop filter is designed, these components are updated. It is also possible to enter the existing components and conditions for an existing design in order to simulate its performance.

Note that this setup is with the LMX2820 and is used in many of the examples in this document.

4.1 Menu Options for Main Diagram

However, if the GUI is fighting your entries, you can disable the options in the main menu. The top 4 options on the menu apply to the main diagram; the last one applies to the filter designer tab.



Main Diagram Links Frequencies with Divides causes any update of a frequency on the main screen to update the divides (or multiplies) and the other way around as well. In some cases, such as when the VCO frequency is mixed down before going to the N divider, this option needs to be disabled.

Main Diagram Updates Performance Metrics causes updates on the main screen such as frequencies, divides, charge pump gain, VCO core, MASH Order, and output format to update performance metrics.

Main Diagram Updates Simulations causes any update of a frequency on the main to trigger simulations to be calculated. If the simulation takes a long time, then it might make sense to disable this option

Main Diagram Reduces Fractions to Lowest Terms reduces fractions to lowest terms. In cases where there is simulation value in not reducing the fraction, such as a nonzero MASH_SEED, it may make sense to disable this option.

4.2 Feature Level, Max Calculation Time, and Loop Gain Change

- **Feature Level** allows user to show more or less details. Default values are set for unseen parameters
- **Max. Calculation Time** limits the amount of time that is allowed for the advanced filter optimizer, fractional spur calculations, and discrete lock time modeling.
- **Loop Gain Change:** This gives an indication of how much the loop gain ($Kpd \cdot Kvco / N$) has changed from the value when the filter was designed. A large change suggests that the filter may be unoptimized and one should re-design the loop filter or adjust the charge pump gain to compensate for the change in loop gain.

4.3 N Divider Fractional Settings

The N divider shown is a calculated value and can be the combination of several components including the PreN divider and fractional circuitry.

- **PreN Divider** is a fixed divider that some devices have that contributes to the total N divide value. These are sometimes necessary to reduce the frequency or for phase synchronization. A PreN divider can impact the impact of the fraction and fractional spurs
- **MASH Order** is the order of the fractional modulator. This impacts spur levels and offsets. One can change this and dynamically see the impact it has on phase noise and spurs.
- **Randomization** is an abstract concept necessary that represents how well the fraction is randomized and is necessary for the modeling of fractional noise and spurs. There is no programmable setting in devices called "Randomization" and there is no simple closed form equation to calculate "% randomization". Randomization relates to how long the fractional sequence is before it repeats and this can be increased in devices by using dithering, nonzero MASH_SEED, or representing the fraction in larger irreducible terms. In general, reduced fractional denominator larger than one million or even one billion would be needed to be considered 100% randomized. In most cases, it makes sense to represent randomization as either 0% or 100%, but there might be some cases where an intermediate value might make sense. Also, the ability to move the slider bar to intermediate states gives the user a more visual understanding of the impact of dithering. The following table gives an idea of how randomization might be chosen.
- **Fnum and Fden** represent the fractional numerator and denominator. They are reduced to lowest terms if so instructed by the menu option. This is done by dividing out the greatest common divisor of Fnum and Fden.

For the purposes of fractional spur calculations only, the fraction is reduced internally to lowest terms, however, the greatest common divisor must also divide MASH_SEED. The fraction may also be internally reduced when calculating spurs. For the spur calculations, the fraction is reduced to lowest terms, but after this, there is a limit to the denominator size based on the MASH_ORDER and factors in the reduced fractional denominator.

| | | Maximum Fraction Denominator for Spur Calculations | | | |
|--------------------------------|---------------------------|--|--------------|--------------|--------------|
| | | MASH_ORDER=1 | MASH_ORDER=2 | MASH_ORDER=3 | MASH_ORDER=4 |
| Reduced Fractional Denominator | Not divisible by 2 or 3 | 64000 | 64000 | 64000 | 64000 |
| | Divisible by 2, but not 3 | 64000 | 32000 | 32000 | 16000 |
| | Divisible by 3, but not 2 | 64000 | 64000 | 21333 | 21333 |
| | Divisible by both 2 and 3 | 64000 | 32000 | 10666 | 5333 |

Below is a table with some examples one might model actual fractional settings in PLLatinum Sim.

| Actual Device Settings | PLLatinum Sim Representation |
|--|--|
| Fraction = 1/1000 | Fnum=1 Fden=1000 Randomomization=0% |
| Fraction = 1000000/1000000000 MASH_SEED=0 | |
| Fraction = 1000000/1000000000 MASH_SEED=1 | |
| Fraction = 1000000/1000000000 Dithering Mode = Strong Dithering | Fnum=1 Fden = 1000 Randomomization=100% |
| Fraction = 1000000/1000000001 MASH_SEED=0 | |
| Fraction = 1001/1000000 MASH_ORDER=3 | Fnum = 1 Fden = 1000 Randomization = 50% |

5 Filter Designer Tab

Select Device

Filter Designer

Phase Noise

Spurs

Lock Time

Bode Plot

Simulation Shown

Phase Noise

LMX2820 Design Tips

Filter Architecture

Filter Order

Filter Type

3rd Order

Passive

Filter Parameters

Calculate Loop Filter

Auto Parameter Strategy

Optimize Jitter

Design Target

Actual

Loop Bandwidth

200 kHz

419.8079 kHz

Phase Margin

70 deg

55.045 deg

Gamma

0.24

7.0675

T3/T1 Ratio

20 %

2.7913 %

Min. High Order Cap

1500 pF

Actual

2200 pF

Capacitor Value Step

10%

Resistor Value Step

10%

Design Warnings

Restrict Components

C1

nF

C2

nF

R2

kΩ

C3

nF

R3

kΩ

Smart force selected values

Performance Summary

Setup Conditions other Tabs

Optimize

Disabled

Parameter

Achieved

Jitter (fs)

40.16

Phase Noise at MKR1

-99.9

Phase Noise at MKR2

-109.7

Phase Noise at MKR3

-118.3

Total Lock Time

56.6

The Filter Designer tab gives maximum power for filter optimization. Note that in Advanced Mode, the “Performance Summary” group box changes to the optimizer settings when the “Optimize” combo box is set to anything other than “Disabled”.

5.1 Design Tips and Simulation Shown

Select Device

Filter Designer

Phase Noise

Spurs

Lock Time

Simulation Shown

Phase Noise

LMX2820 Design Tips

The **Design Tips** box gives part specific loop filter design information when clicked.

Select Device

Filter Designer

Phase Noise

Simulation Shown

Phase Noise

Filter Architecture

The simulation chart shown on the filter designer tab can be changed. This is useful for the user to directly see the impact of design parameters.

Select Device

Filter Designer

Phase Noise

Simulation Shown

Spurs

Filter Architecture

Device Specific Loop Filter Design Tips

Filter Design Comments:

1. The charge pump gain is programmable. Consider using the highest gain for best PLL phase noise.

2. When used in fractional mode, the noise of the delta sigma modulator peaks around half of the phase detector frequency. If this noise is noticeable in the design, consider using a higher order filter.

3. This device has a minimum high order capacitance. What this means is that if the capacitor closest to the VCO is too small, there can be phase noise degradation in the 200kHz - 1 MHz range. If this value is 3.3 nF or larger, there is no degradation. If it is 1.5 nF, it can be a few dB. It may make sense to use a value less than 3300 pF if this requirement restricts the loop bandwidth, but not recommended to go below 1500 pF. This device has a minimum high order capacitance. What this means is that if the capacitor closest to the VCO is too small, there can be phase noise degradation in the 200kHz - 1 MHz range. If this value is 3.3 nF or larger, there is no degradation. If it is 1.5 nF, it can be a few dB. It may make sense to use a value less than 3300 pF if this requirement restricts the loop bandwidth, but not recommended to go below 1500 pF.

OK

Phase Noise at 4534.1 MHz

Phase Noise (dBc/Hz)

Offset (Hz)

Total

PLL

VCO

Filter

Output

Spurs at Fout

Srr (dBc)

Offset (kHz)

Primary Fractional

Sub Fractional

Fvco%Fosc

Fout%Fosc

5.3 Filter Order and Filter Type

| | |
|---|--|
| Filter Architecture ? Filter Order: 2nd Order Filter Type: Passive | |
| Filter Architecture ? Filter Order: 3rd Order Filter Type: Passive | |
| Filter Architecture ? Filter Order: 4th Order Filter Type: Passive | |

5.4 Filter Type

| | |
|---|--|
| Passive Filter has only capacitors and resistors | |
| Active Type A Filter with op amp to boost voltage. C1 & R1 reduce speed requirements on op amp while still allowing charge pump to operate at mid voltage | |
| Active Type B Filter with op amp to boost voltage. Less optimal than Active A or Active C, but might be easier for board layout that can accommodate both active and passive filter | |
| Active Type C Filter with op amp to boost voltage. Most intuitive approach where a simple voltage gain is used and also least demanding for the op amp. However, this approach also multiplies the voltage noise of the op amp. | |
| Infinite Loop Bandwidth Theoretical filter that passes all in-band noise sources and eliminates all out-band noise sources. Useful to analyze input reference and PLL noise. | |
| 0 Hz Bandwidth Theoretical filter that passes all out-band noise sources and eliminates all in-band sources. Useful to analyze VCO phase noise. | |
| Brick Wall Theoretical filter passes in-band sources in the loop bandwidth and eliminates them outside the loop bandwidth. Vice versa for out-band sources. Good to set a limit for best possible jitter. | |
| Ideal NonComponent Ideal filter that ignores component restrictions and the restrictions they put on parameters. | |

5.5 Filter Parameters

| Design Target | | Actual | |
|----------------|---------|--|--------------|
| Loop Bandwidth | 200 kHz | <input type="checkbox"/> Auto | 419.8079 kHz |
| Phase Margin | 70 deg | <input checked="" type="checkbox"/> Auto | 55.045 deg |
| Gamma | 0.24 | <input checked="" type="checkbox"/> Auto | 7.0675 |
| T3/T1 Ratio | 20 % | <input checked="" type="checkbox"/> Auto | 2.7913 % |

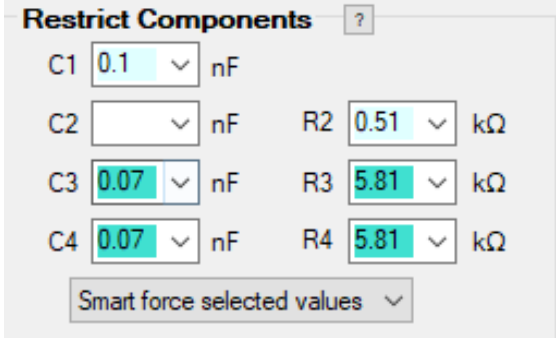
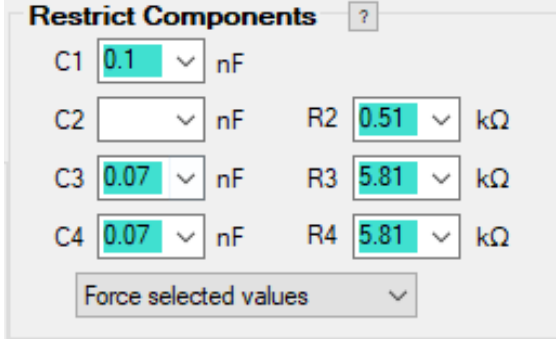
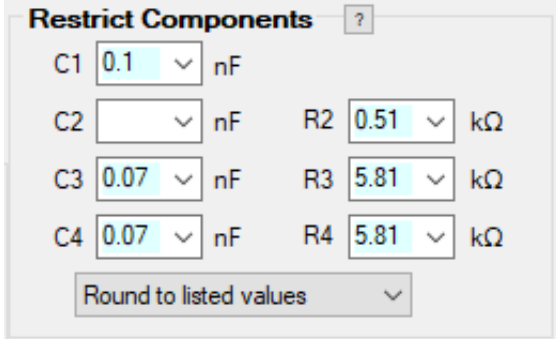
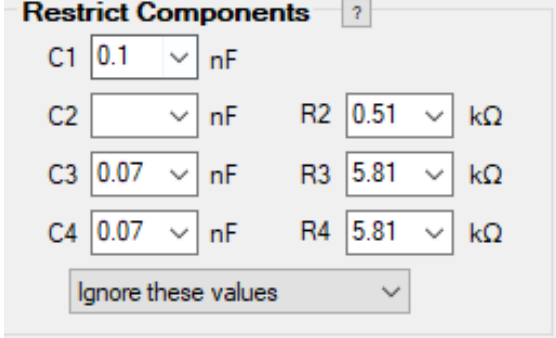
| | | | |
|----------------------|---------|---------------------|---------|
| Min. High Order Cap | 1500 pF | Actual | 2200 pF |
| Capacitor Value Step | 10% | Resistor Value Step | 10% |

The Filter Parameters group box has the filter design parameters of loop bandwidth, phase margin, gamma, and pole ratios.

- Auto Parameter Strategy and Auto Check boxes
 - The Auto Parameter Strategy chooses the method for choosing Loop Bandwidth, Phase Margin, Gamma, T3/T1 ratio, or T4/T3 ratio when the “Auto” checkbox is chosen and not in advanced optimizer mode. Options are Optimize Jitter, Maximize Loop Bandwidth, Minimize Loop Bandwidth, or Balance for Spurs.
 - Note that in Advanced Optimizer is used, the Auto Parameter Strategy combo box disappears
- Sliders
 - When not using the advanced optimizer and the Auto checkbox is selected, this allows the user to slide the parameter value to see interactively with the graphs what the impact is.
- Actual Value
 - The design target specifies the design target, but the actual value may be different due to component rounding.
- Min High Order Cap
 - The high order capacitor is the one closest to the VCO. It is desirable for this not to be too small so that it is not swamped out by the VCO input capacitance. Also, some devices with integrated VCO get phase noise degradation if this value is too small. PLLatinum Sim will reduce the loop bandwidth to achieve this value if necessary. **The loop bandwidth can be restricted due to the Min High Order Cap or VCO input capacitance.**
- Capacitor Value Step/Resistor Value Step
 - The design target specifies the design target, but the actual value may be different due to component rounding.
- Design Warnings
 - When there is some non-ideal issue that happens when the filter is designed, a design warning will appear. Be sure to click on the “?” box to see the meaning of this warning

5.6 Restrict Components

Some devices have partially integrated loop filters where one is restricted to a discrete set of values. Other times, a user might want to force a particular component value. **These forced components are for the loop filter design, not the actual values that are being simulated (these are on the main diagram).** Dark teal indicates the value is forced to the and the components designed around these values. Light blue indicates that the loop filter will be designed and then the closest value on this list will be chosen.

| | |
|---|--|
|  | <p>Smart force selected values uses the closest known partially integrated filter method and forces the dark teal components and designs the filter. Then it rounds the values to the closest value in the light teal boxes. For this example, C1, C3, C4, R2, R3, and R4 are restricted, but there is no design equations for this case, so the smart force option forces C3, C4, R3, and R4 and designs as normal, but then rounds C1 and R2 to the values on the list.</p> |
|  | <p>Force selected values forces the dark teal values, regardless if there are design equations or not. Be cautious with this approach as it can lead to design failure.</p> |
|  | <p>Round to listed values designs the loop filter as it normally would with no restricted values, but then rounds to the closest value on the list.</p> |
|  | <p>Ignore these values totally ignores these values.</p> |

There are only certain combinations of forced combinations allowed that are listed in the table below:

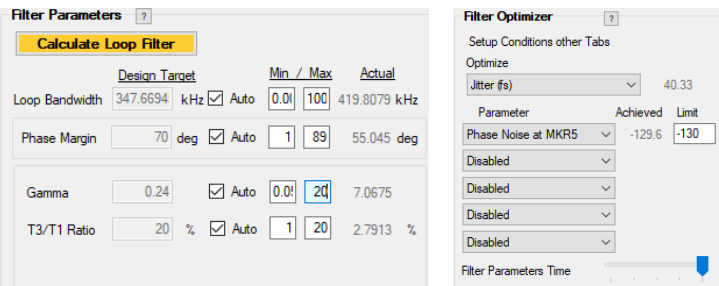
| Filter Type | Rules |
|---------------------|---|
| All Filters | <ul style="list-style-type: none"> • No Forced Components is always allowed for any filter order or type • All Forced Components is always allowed for any filter order or type • R3 & C3 can be forced if it is both components in the case of a 3rd order filter • R3, C3, R4, & C4 be forced if it is all components in the case of a 4th order filter |
| Active Type A | <ul style="list-style-type: none"> • R1 & C1 both be forced only for a 2nd order filter with no other components forced • R1 or C1 can be forced for all filter orders if it is not both of them • R2 or C2 can only be forced in a 2nd order when it is not both of them • R3, C3, R4, or C4 can be forced if exactly one or all of these are forced. |
| Active Type B and C | <ul style="list-style-type: none"> • C1, C2, & R2 can only be forced in 2nd order filter and only up to one of these. • R3, C3, R4, & C4 can be forced if exactly one or all of these are forced. |
| Passive | <ul style="list-style-type: none"> • Any One Component can be forced for any filter order |

There are also some things to keep in mind when forcing components:

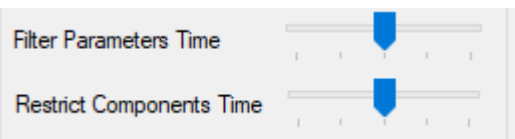
- The smart force option will steer the design towards one of these valid combinations. If the regular force option is used, then the filter designer will return with an error message saying the design is not supported.
- Even in the case that the design is supported, forcing some individual may work for only a narrow range and going out side this range may result in a design failure.
- If the high order capacitor is forced, then the minimum high order capacitance constraint for the loop filter design is ignored.
- The VCO input capacitance can interact with forced components. If one forces the capacitor next to the VCO, then PLLatinum Sim adds the VCO capacitance to that. However, if one forces a different component, then it can distort the results.
 - Consider the case of a 3rd order filter passive filter with R3 forced and the value for C3 for zero VCO input capacitance is 200 pF. Now consider if one modifies this exact same design and makes the VCO input capacitance 100 pF. This will still work and it will just modify C3 to be 100 pF and all other components the same. However, if one modifies the VCO input capacitance above 200 pF, then this will return a valid filter, but the loop bandwidth and other design parameters will be off due to the VCO input capacitance
- In the case the higher order poles are forced (R3 & C3 for 3rd Order filter, R3, R4, C3, & C4 for 4th Order filter), the loop bandwidth may be restricted and the poles T3 and T4 will be restricted by these components. It is also possible to have “degenerate” filter which has C1 = 0 and T1 = 0, but that is still stable.

5.7 The Advanced Optimizer

The advanced optimizer appears in advanced mode when the Optimize box is set to a setting other than “disabled” as shown below. In this case, the user is optimizing the jitter subject to the condition that the phase noise at marker 5 is better than -130 dBc/Hz. These parameters are all taken from the phase noise, spur, and lock time tabs. **The maximum calculation time is limited to the value specified in the Max Calculation Time box on the main diagram.**



When the advanced optimizer enabled, the filter parameters box is updated. And the “Auto Parameter Strategy” combo box disappears as it no longer applies. Instead, PLLatinum Sim iterates using numerical methods for any parameter that has its box checked as Auto. The user can specify Min/Max limits for the optimizer to choose to prevent it from running to an undesired solution.



At the bottom of the filter optimizer group box are Filter Parameters Time and Restrict Components Time (only if there are a list of restricted components). Moving these sliders to the gives the optimizer more power, but takes time. Specifically, here is what the slider is really doing.

| Slider Value | Time | Accuracy | Optimization Details |
|--------------|----------|----------|---|
| 0 | Shortest | Minimum | <ul style="list-style-type: none"> None |
| 1 | ... | ... | <ul style="list-style-type: none"> Sweep BW Hook-Jeeves parameter sweep, 8 Steps, 12 Iterations |
| 2 | ... | ... | <ul style="list-style-type: none"> Sweep BW, ϕ Hook-Jeeves parameter sweep, 16 Steps, 24 Iterations Perturb Components 2 steps up/down from design value |
| 3 | ... | ... | <ul style="list-style-type: none"> Initial parameter search with ideal NonComponent filter Sweep BW, ϕ, γ Hook-Jeeves parameter sweep, 32 Steps, 48 Iterations Perturb Components 3 steps up/down from design value |
| 4 | Longest | Maximum | <ul style="list-style-type: none"> Initial parameter search with ideal NonComponent filter Sweep BW, ϕ, γ Hook-Jeeves parameter sweep, 64 Steps, 96 Iterations Perturb Components 4 steps up/down from design value |

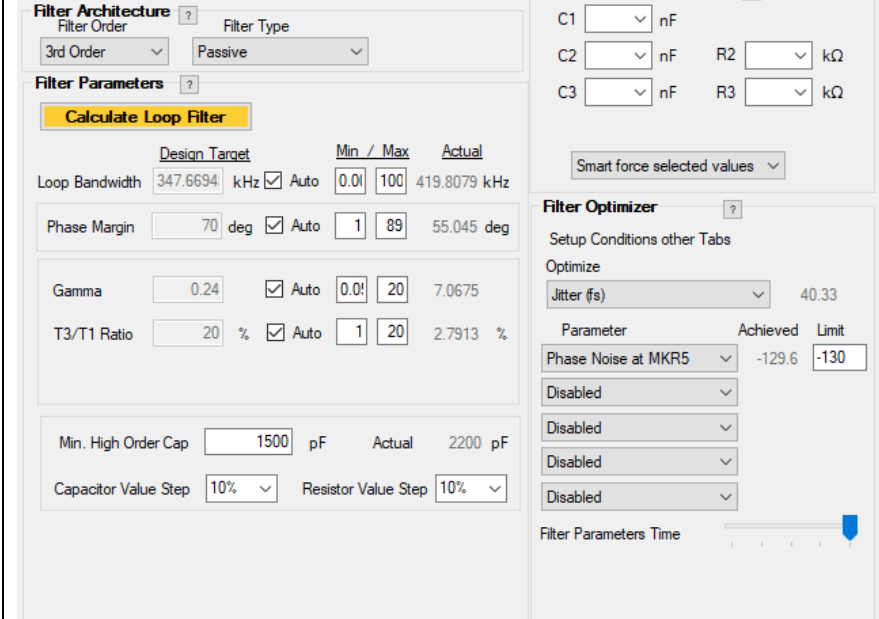
The forced components (dark teal, not the rounded light blue ones) are iterated through according to the following chart.

| Slider Value | Time | Accuracy | Optimization Details |
|--------------|----------|----------|---|
| 0 | Shortest | Minimum | Only selected values considered |
| 1 | ... | ... | Up to 3 values and always includes selected value, minimum value, and maximum value |
| 2 | ... | ... | Up to 5 values and always includes selected value, minimum value, and maximum value |
| 3 | ... | ... | Up to 7 values and always includes selected value, minimum value, and maximum value |
| 4 | Longest | Maximum | All Values |

Tips for the Advanced Optimizer

- Optimizer starts out at specified parameter values. These closer that these are to optimal, the better the optimizer performs
- If optimizer runs out of time, it returns the best solution so far
- For the higher settings, increase the Max. Calculation Time

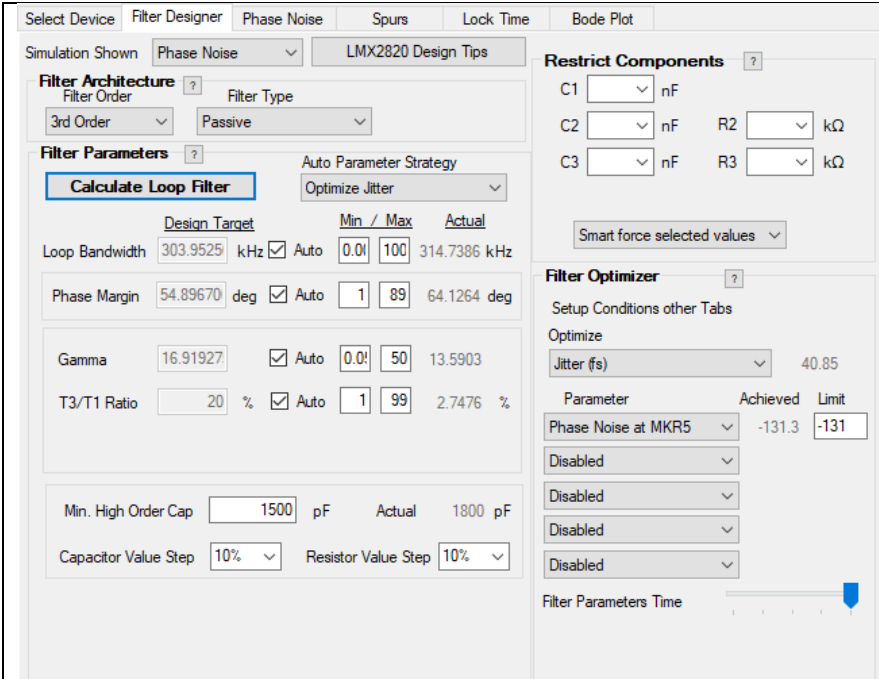
Example Using the Advanced Optimizer



Before Running the Optimizer

The jitter is 40.33 fs and the phase noise at 1 MHz offset (marker 5) is -129.6 dBc/Hz.

This is the same setup using the LMX2820 that has been used in previous figures. The LMX2820 loop filter is fairly well optimized for jitter already, so the impact will not be as much as it would be for a less optimized design. Nevertheless, there is still room for optimization.



After Running the Optimizer

Now impose the constraint that the phase noise at 1 MHz (marker 5) needs to be at least -131 dBc and find the optimal jitter under these conditions.

The max calculation time on the main screen was changed to 300 seconds and the filter parameter time was moved to the last slider position to allow maximum computational power.

Although the original loop filter was pretty well optimized already, the new filter from the advanced optimizer improves the phase noise at 1 MHz from -129.6 to -131.3 dBc/Hz while increasing the jitter by 0.5 fs.

Phase Noise Tab

The phase noise tab gives the user to specify phase noise metrics. However, realize that these are read in and calculated from a database and modified automatically based on settings, so it is not necessary to override these metrics in most cases.

LMX2820 Phase Noise Tips

Graph Settings

Points 101 ☒ Autoscale Axes

min max

X Axis 0.0001 100 MHz

Y Axis -200 -90 dBc/Hz

☐ Load Comparison Trace

Total Phase Noise at Offsets

| Offset (kHz) | Noise |
|--------------|--------|
| MKR1 0.1 | -99.9 |
| MKR2 1 | -109.7 |
| MKR3 10 | -118.3 |
| MKR4 100 | -120.9 |
| MKR5 1000 | -129.6 |
| MKR6 10000 | -152.4 |

Crossover Metrics

InBand to VCO 346.4 kHz

PLL 1/f to Floor 31.7 kHz

VCO 1/f³ to 1/f² 95.5 kHz

VCO 1/f² to Floor 10.1 MHz

Integrated Noise

Lower Limit 1 kHz

Upper Limit 20 MHz

RMS Jitter 40.37 fs

Other Noise Metrics

RMS Phase Error 0.066 deg

EVM .115 %

Integrated Noise 1.321e-6

SNR -58.8 dBc/Hz

Avg Noise Floor -134.8 dBc/Hz

Other Noise Sources

☐ Include Spurs

☒ Enable Loop Filter Noise

☒ Enable Distribution Path Noise

Output/Distribution Path Metrics

1/f (Total) -1000 dBc/Hz

Floor (DistPath) -1000 dBc/Hz

Floor (Div/Mult) -158 dBc/Hz

OSC, PLL, and VCO Noise

Input Source (OSC) Noise

☒ Disable ☐ Use Metrics ☐ Use Points ☐ Load Data

VCO Noise

☐ Disable ☒ Use Metrics ☐ Use Points ☐ Load Data

Noise Metrics

1/f³ -158.1

1/f² -147.9

Floor -168

☐ Override

PLL Noise

☐ Disable ☒ Use Metrics ☐ Use Points ☐ Load Data

Noise Metrics (dBc/Hz)

Figure of Merit -235

Normalized 1/f -133

Fractional -99

☐ Manual Override

The Phase Noise tab gives many options to set up and interpret the phase noise.

Phase Noise at 4531.4 MHz

Phase Noise (dBc/Hz)

Offset (Hz)

Legend: Total, PLL, VCO, Filter, Output

The main phase noise chart appears whenever the Phase noise tab is selected. It can also appear on the filter design tab if it is selected as tie simulation shown. The Total line shows the sum of all sources. It also shows the individual noise sources that add up to the total. One can zoom in and click on this cart to get a closer look

PLL

PLL Phase Noise Decomposition at 4531.4 MHz

Phase Noise (dBc/Hz)

Offset (Hz)

Legend: PLL_FLK, PLL_FLR, PLL_FRAC

The phase noise decomposition chart appears in advanced mode and allows one to look closer at the OSC, PLL, VCO, Filter, AMP, or Output noise. The noise source of interest can be selected by the combo box in the upper right.

5.8 Phase Noise Tips

Select DeviceFilter DesignerPhase

LMX2820 Phase Noise Tips

Graph Settings

Many devices have part specific phase noise tips that are either not modeled or need special modifications for modeling. Be sure to click the phase noise tips button to see all the details.

TIPLLatinumSim

Phase Noise Tips:

1. Phase Noise is better for higher charge pump current modes.

2. Phase Noise is better for input slew rates. A high slew rate signal is desirable

3. The input doubler can be used to increase the input frequency and improve phase noise. It adds about 0.5 dB to the PLL figure of merit and 1/f noise

4. Be aware of the phase noise of the delta sigma modulator. This peaks at half the phase detector frequency. The randomization and modulator order has a large impact on this noise.

5. This device has a minimum high order capacitance. What this means is that if the capacitor closest to the VCO is too small, there can be phase noise degradation in the 200kHz - 1 MHz range. If this value is 3.3 nF or larger, there is no degradation. If it is 1.5 nF, it can be a few dB. It may make sense to use a value less than 3300 pF if this requirement restricts the loop bandwidth, but not recommended to go below 1500 pF

6. If using the programmable input multiplier (MULT), it adds about 3 dB to the PLL 1/f noise and 8 dB to the PLL figure of merit.

7. If modeling phase noise using the PFDin pin, keep the correct phase detector and VCO frequencies and ignore that the N divider value is wrong. Let K be the factor the N divider was decreased by. Take note of the PLL 1/f and PLL figure of merit and write it down. Increase the charge pump current by a factor of K. Make the PLL 1/f noise to be the number you wrote down - 20*log(K). Make the PLL figure of merit to be the number you wrote down - 10*log(K)

8. Simulation assumes at least 4.7 uF on Pin 3 so there is no degradation in 1/f noise. If using a lower value (for faster VCO instant calibration), manually degrade PLL 1/f noise.

OK

5.9 Loading Phase Noise Traces

5.9.1 General Method of Loading Phase Noise Traces

The phase noise tab allows the user to load a comparison trace, OSCin phase noise trace, PLL phase noise trace, or VCO phase noise trace. These are under different sections, but the general file format is:

<Offset in Hz> + <Tab> +<Phase Noise>+ <Carriage Return>

Comma or space can also be used in place of the <tab> and any entry with an # is ignored and can be used for comments. If using excel, simply use a the first column for offset and the second one for phase noise and save as tab delimited text. The frequency is assumed to be whatever is specified on the main diagram.

5.10 Graph Settings & Comparison Trace

Graph Settings

Points101Autoscale Axes

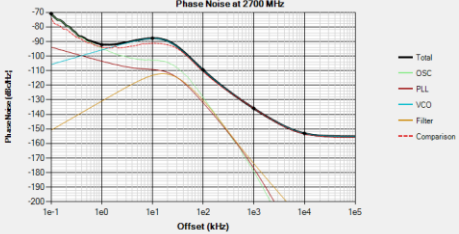
minmax

X Axis0.0001100MHz

Y Axis-200-90dBc/Hz

☐ Load Comparison Trace ?

Phase Noise at 2700 MHz



- Points are used in the graph and having a very large number of points may increase computational time as this is used for numerical integration. The X Axis and Y axis should be self-explanatory.
-

The comparison trace allows the user to load a trace to compare to the actual one. The most common use is to load in actual measured data so that it can be compared directly to the simulation. This is using the LMX2581 EVM with on board XO. Note the red (comparison) and black (Total) traces are in good agreement.

5.11 Total Phase Noise at Offsets

| Total Phase Noise at Offsets | | |
|------------------------------|--------------|--------|
| | Offset (kHz) | Noise |
| MKR1 | 0.1 | -99.9 |
| MKR2 | 1 | -109.7 |
| MKR3 | 10 | -118.4 |
| MKR4 | 100 | -121.6 |
| MKR5 | 1000 | -128.3 |
| MKR6 | 10000 | -152.7 |

- Points are used in the graph and having a very large number of points may increase computational time as this is used for numerical integration. The X Axis and Y axis should be self-explanatory.
- The comparison trace allows the user to load a trace to compare to the actual one. The most common use is to load in actual measured data so that it can be compared directly to the simulation

5.12 Crossover Metrics

| Crossover Metrics ? | |
|--|-----------|
| InBand to VCO | 346.3 kHz |
| PLL 1/f to Floor | 31.7 kHz |
| VCO 1/f ³ to 1/f ² | 95.5 kHz |
| VCO 1/f ² to Floor | 31.3 MHz |

PLLatinum Sim models OSC, PLL, and VCO phase noise using flat, 1/f, 1/f², and 1/f³ curves. These metrics show where these regions cross.

5.13 Integrated Noise and Other Noise Metrics

| Integrated Noise | |
|-----------------------|---------------|
| Lower Limit | 1 kHz |
| Upper Limit | 20 MHz |
| RMS Jitter | 40.33 fs |
| Other Noise Metrics ? | |
| RMS Phase Error | 0.066 deg |
| EVM | .115 % |
| Integrated Noise | 1.32e-6 |
| SNR | -58.8 dBc/Hz |
| Avg Noise Floor | -134.8 dBc/Hz |

- The integrated noise is calculated using the specified Lower and Upper Limit values.
- The RMS Jitter is what the filter optimizer references
- Other interpretations of integrated noise floor are also shown as calculated from the phase noise

5.14 Other Noise Sources

| Other Noise Sources ? | |
|--|--------------|
| <input type="checkbox"/> Include Spurs | |
| <input checked="" type="checkbox"/> Enable Loop Filter Noise | |
| <input checked="" type="checkbox"/> Enable Distribution Path Noise | |
| Output/Distribution Path Metrics | |
| 1/f (Total) | -1000 dBc/Hz |
| Floor (DistPath) | -1000 dBc/Hz |
| Floor (Div/Mult) | -158 dBc/Hz |

- Include Spurs checkbox displays the spurs and adds their energy to the integrated noise metrics
- Enable Loop Filter Noise enables the noise of the resistors in the loop filter as well as the noise of the op-amp if an active filter is used
- Enable Distribution Path Noise enables the noise of the output buffer as well as any multipliers or dividers. Note that for some devices, the output buffer noise is included in the VCO where as in others, it is separated out

5.15 OSC, PLL, and VCO Noise

5.15.1 Disable Option

When the option is set to Disable, the noise source is disregarded.

5.15.2 Use Metrics Option

OSC and VCO Noise Metrics

The OSC and VCO noise are modeled as the sum of $1/f^3$, $1/f^2$, and Floor metrics. These metrics are normalized to 1 GHz carrier and 1 MHz offset. The $1/f^3$ and $1/f^2$ noise are assumed to vary as $20 \cdot \log(\text{frequency})$ and the floor is assumed to vary as $10 \cdot \log(\text{frequency})$. They can either be manually entered or calculated by specifying three phase noise offsets. Ideally one offset should be mainly on the $1/f^3$ slope, another on the $1/f^2$ slope, and the third on the noise floor. PLLatinum Sim tries to solve this using three equations and three unknowns, but if one provides two points on the slope, one of them will be ignored and the noise will be modeled with less than three noise slopes. When the offsets are specified, be sure to push the button to update the VCO or PLL metrics. For the VCO metrics, there is the option to use a two-frequency model in the case that the metrics vary significantly between the minimum and maximum VCO frequency. For any VCO frequency in between, a linear interpolation is used

PLL Noise Metrics

For the PLL noise, the PLL figure of merit, the normalized $1/f$ noise (1 GHz carrier, 10 kHz offset), and the fractional PLL noise.

OSC, PLL, and VCO Noise ?

Input Source (OSC) Noise

☐ Disable ☒ Use Metrics ☐ Use Points ☐ Load Data

Noise Metrics

| $1/f^3$ | -1000 |
|---------|--------|
| $1/f^2$ | -185.1 |
| Floor | -151.6 |

☐ Override

Data for Noise Metrics

| Fosc (MHz) | Offset (kHz) | Noise |
|------------|--------------|-------|
| 100 | 1 | -145 |
| | 10 | -160 |
| | 1000 | -165 |

VCO Noise

☐ Disable ☒ Use Metrics ☐ Use Points ☐ Load Data

Noise Metrics

| | |
|---------|--------|
| $1/f^3$ | -158.1 |
| $1/f^2$ | -147.9 |
| Floor | -168 |

☐ Override

PLL Noise

☐ Disable ☒ Use Metrics ☐ Use Points ☐ Load Data

Noise Metrics (dBc/Hz)

| | |
|------------------|------|
| Figure of Merit | -235 |
| Normalized $1/f$ | -133 |
| Fractional | -99 |

☐ Manual Override

5.15.3 Use Points Option

Up to six points can be specified and points in between will be estimated. If less than six points are used, put “0” for the offset. Once these are entered, press the “Update Noise” for this to actually be applied.

OSC, PLL, and VCO Noise ?
Input Source (OSC) Noise
☐ Disable ☐ Use Metrics ☒ Use Points ☐ Load Data
Data for Use Points

| Fosc (MHz) | Offset (kHz) | Noise | Offset (kHz) | Noise |
|------------|--------------|--------|--------------|--------|
| 100 | 0.01 | -86.4 | 10 | -157.5 |
| | 0.1 | -118.9 | 100 | -164.7 |
| | 1 | -143.4 | 1000 | -168.6 |

Update Noise

VCO Noise
☐ Disable ☐ Use Metrics ☒ Use Points ☐ Load Data
Data for Use Points

| Fvco (MHz) | Offset (kHz) | Noise | Offset (kHz) | Noise | Offset (kHz) | Noise |
|------------|--------------|-------|--------------|--------|--------------|-------|
| 6000 | 10 | -97 | 1000 | -137 | 100000 | -162 |
| | 100 | -117 | 10000 | -156.2 | 0 | 0 |

Update Noise

PLL Noise
☐ Disable ☐ Use Metrics ☒ Use Points ☐ Load Data
Data for Use Points

| Fvco (MHz) | Offset (kHz) | Noise | Offset (kHz) | Noise |
|------------|--------------|--------|--------------|--------|
| 2000 | 0.1 | -145.8 | 100 | -145.8 |
| | 1 | -160 | 1000 | -160 |
| | 10 | -165 | 100000 | -165 |

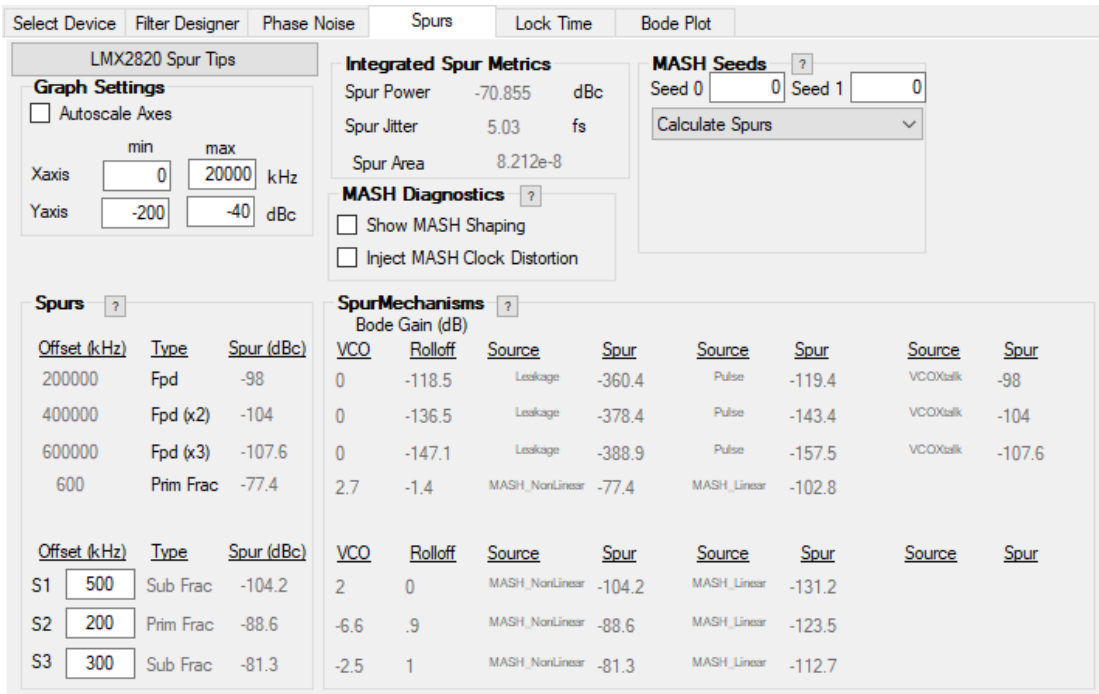
Update Noise

Load Trace Option

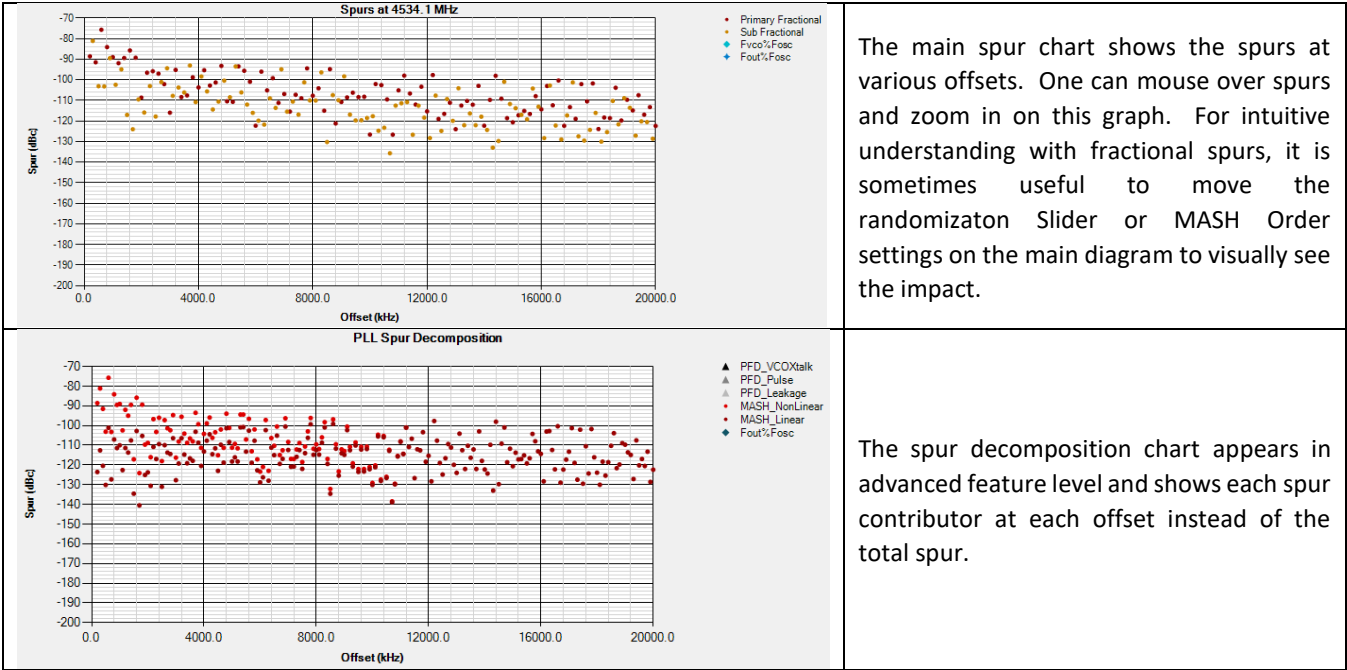
A phase noise trace can be loaded using the method previously stated.

6 Spurs Tab

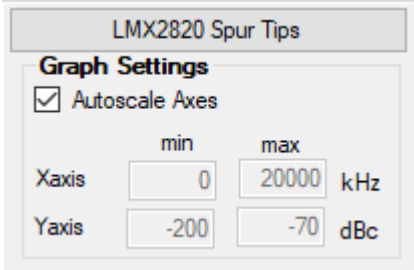
The spurs tab gives detailed modeling of spurs including integer spurs, fractional spurs, and spurs due to crosstalk on the chip. Note that the fourth entry in the “Spurs” section is the highest spur that is not mentioned anywhere else and within the graph settings range. Spur simulations do not always perfectly match measured results and do not account setup conditions, process/temperature variations, layout, and many other factors. That being said, the spur simulator gives good insight as to where the spurs occur and some of the most common contributors to them.

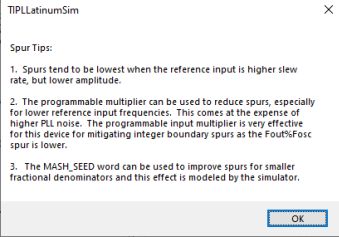


6.1 Spur Chart and Decomposition Chart



6.2 Spur Tips and Graph Settings

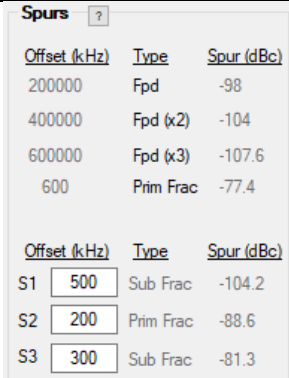




The spur tips button shows part specific spur hints when clicked.

For the graph settings, one thing to keep in mind is that if one is doing fractional spurs, increasing the X axis has a dramatic impact on calculation time for fractional spurs. If this time exceeds Max Calculation Time on the Main Diagram, then the calculation will stop. In summary, if simulating in fractional mode with many small fractional spurs, do not set the max Xaxis to be orders of magnitude larger than needed.

6.3 Spurs Box



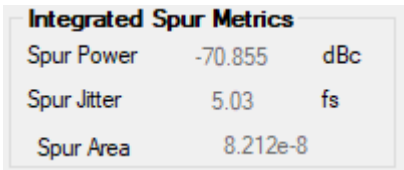
The top half of the box shows the first three phase detector spurs and if fractional mode is used then the integer boundary spur (IBS) and primary fractional spur as well.

Below that are three entry boxes where an offset can be chosen and then PLLatinum Sim will try to find the closes spur to this specified offset.

All the spur types are

Be sure to click on the “?” icon for more information about the spur types.

6.4 Integrated Spur Metrics



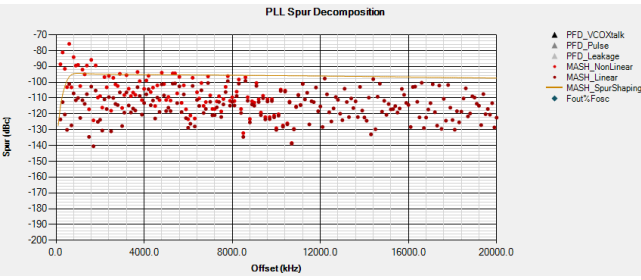
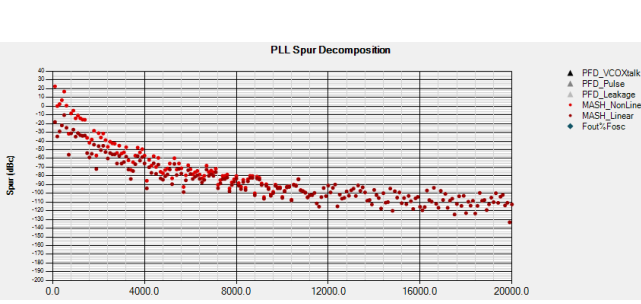
Integrated Spur Metrics are calculated by integrating the spur power. The integration range is the range specified for the “Xaxis” on the graph settings on the spur tab. Be aware that on the Phase Noise tab, the integration range is different and this range on the spur tab also applies to spur energy calculated on the Phase Noise tab.

6.5 Spur Mechanisms



Spur Mechanisms gives an idea of what mechanisms are contributing to each spur. Be sure to click on the “?” icon in spur mechanisms to get detailed descriptions of what each of these mechanisms are.

6.6 Spur Diagnostics

| | |
|---|--|
| <p>MASH Diagnostics ?</p> <p><input checked="" type="checkbox"/> Show MASH Shaping</p> <p><input type="checkbox"/> Inject MASH Clock Distortion</p> <p>When Show MASH Shaping is selected, the MASH_Spur Shaping trace appears on the Spur Decomposition chart. As the randomization approaches 100%, the MASH_Linear spurs approach this curve.</p> |  <p>PLL Spur Decomposition</p> <p>Spur (dBc)</p> <p>Offset (Hz)</p> <p>Legend: PFD_VCOWalk, PFD_Pulse, PFD_Leakage, MASH_NonLinear, MASH_Linear, MASH_SpurShaping, Fout%Fosc</p> |
| <p>MASH Diagnostics ?</p> <p><input type="checkbox"/> Show MASH Shaping</p> <p><input checked="" type="checkbox"/> Inject MASH Clock Distortion</p> <p>Inject MASH Clock Distortion exaggerates the impact of the uneven clock coming from the N divider by assuming the VCO frequency does not move. It us a diagnostic tool to see which spurs are impacted by lower N divider values. This does not represent actual spur levels.</p> |  <p>PLL Spur Decomposition</p> <p>Spur (dBc)</p> <p>Offset (Hz)</p> <p>Legend: PFD_VCOWalk, PFD_Pulse, PFD_Leakage, MASH_NonLinear, MASH_Linear, Fout%Fosc</p> |

6.7 MASH Seeds

MASH seeds impact the initial starting values and numerical sequence of the MASH engine, thus impacting fractional spurs. They can be used to optimize spurs for smaller denominators (say <=1000). Also, they can shift phase and cause unwanted spurs. PLLatinum Sim models their impact.

| | |
|---|---|
| <p>MASH Seeds ?</p> <p>Seed 0 <input type="text" value="0"/></p> <p>Calculate Spurs</p> | <p>Calculate Spurs finds the spur levels with the given seed values.</p> |
| <p>MASH Seeds ?</p> <p>Seed 0 <input type="text" value="0"/></p> <p>Optimize Seeds for Spur Jitter</p> <p>Find Optimal Seeds</p> | <p>Optimize Seeds for Spur Jitter searches through the seeds to find the values that minimize the spur jitter in the integrated spur metrics group.</p> |
| <p>MASH Seeds ?</p> <p>Seed 0 <input type="text" value="0"/></p> <p>Optimize Seeds for Spur Index</p> <p>Find Optimal Seeds</p> | <p>Optimize Seeds for Spur Index searches through the seeds to find the values that minimize $3*S1+2*S2+S3$. S1, S2, and S3 are specified in the Spurs group box.</p> |
| <p>MASH Seeds ?</p> <p>Seed 0 <input type="text" value="0"/></p> <p>Optimize Seeds for Spur Margin</p> <p>S1 <input type="text" value="-100"/> S2 <input type="text" value="-88"/> S3 <input type="text" value="-81"/></p> <p>Find Optimal Seeds</p> | <p>Optimize Seeds for Spur Margin searches for the spurs that gives the most margin. It compares the S1, S2, and S3 spurs in the spur group to the S1, S2, and S3 design targets in the MASH Seeds group and tries to maximize the margin for the worst case spur.</p> |

7 Lock Time Tab

The lock time tab gives the ability to model the lock time. This includes VCO digital calibration time, lock time to frequency, lock time to phase, and a discrete lock time model that accounts for the discrete sampling action of the phase detector and nonlinearity of the charge pump. Due to longer potential computation times, the discrete model is only calculated when the "Calculate Discrete LT" button is pressed.

Select Device | Filter Designer | Phase Noise | Spurs | **Lock Time** | Bode Plot

LMX2820 Lock Time Tips

Graph Settings
Points
☒ Autoscale Axes
X Axis us
Y Axis MHz
☐ Load Comparison Trace ?
☒ Include VCO Calibration Time

VCO Calibration ?
StartCore Cal Start Frequency MHz
? VCO Calibration Time 31.6 us ? ☐ Instant VCO Calibration

Frequency Response ?

| | Analog Model | Discrete Model |
|------------------|---|---|
| Final Frequency | <input type="text" value="4534.1"/> MHz | <input type="text" value="4534.1"/> MHz |
| Start Frequency | <input type="text" value="4400"/> MHz | <input type="text" value="4400"/> MHz |
| Settle Tolerance | <input type="text" value="1000"/> Hz | <input type="text" value="1000"/> Hz |
| Analog Lock Time | 25 us | Discrete Lock Time 24.9 us |
| Total Lock Time | 56.6 us | Total Lock Time 56.5 us |
| Peak Time | us | Peak Time 100 us |
| Peak Frequency | 4400 MHz | Peak Frequency 4534.1 MHz |

Phase Response ?

| | Analog Model | Discrete Model |
|-------------------|------------------------------------|------------------------------------|
| Phase Disturbance | <input type="text" value="0"/> deg | <input type="text" value="0"/> deg |
| Settle Tolerance | <input type="text" value="1"/> deg | <input type="text" value="1"/> deg |
| Analog Lock Time | 26.9 us | Discrete Lock Time 26.9 us |
| Total Lock Time | 58.5 us | Total Lock Time 58.5 us |
| Peak Time | 32.2 us | Peak Time 32.3 us |
| Peak Phase | 1039.8 deg | Peak Phase -1052.6 deg |

Discrete Lock Time Model ?

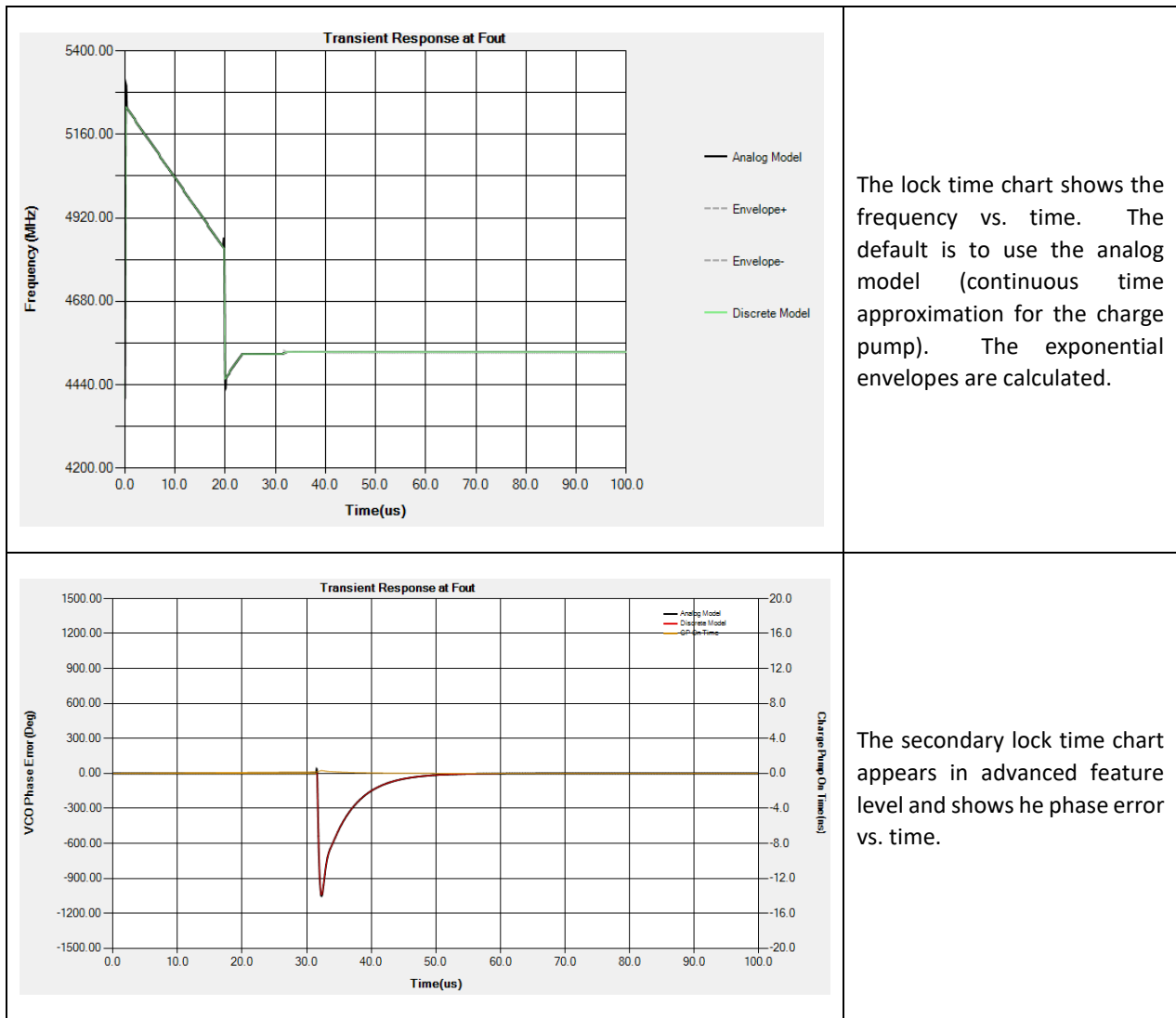
☐ Show Calculated Points
☐ Apply Non Ideal Modeling

Calculate Discrete LT
Cycle Slips
Time to First Cycle Slip n/a us

☒ Enable Fastlock
Fastlock ?

Timeout us
Glitch kHz
Kpd Fpd
C2 R2
C3 R3

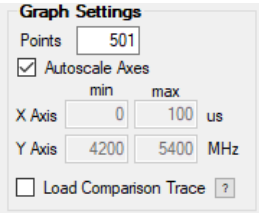
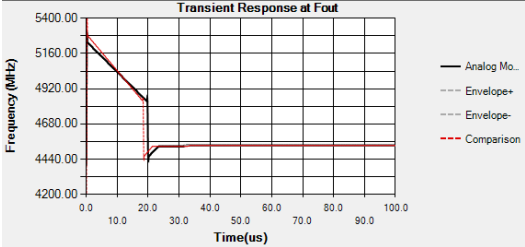
7.1 Lock Time Frequency and Phase Chart



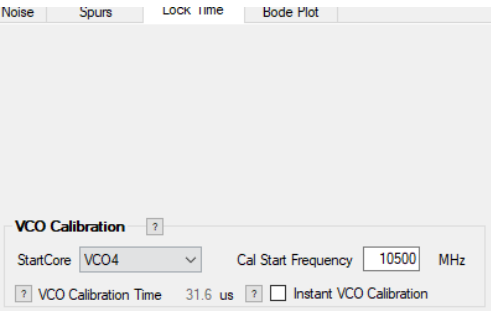
7.2 Lock Time Tips

| | |
|--|---|
| <p>Many devices have part specific lock time tips that are either not modeled or need special modifications for modeling. Be sure to click the lock time tips button to see all the details.</p> | <div data-bbox="259 1428 747 1501"> <p>Select Device Filter Designer Phase Noise Spurs Lock Time Bode Plot</p> <p>LMX2820 Lock Time Tips</p> </div> <div data-bbox="925 1375 1412 1711"> <p>Device Specific Lock Time Tips</p> <p>Lock Time Tips:</p> <ol style="list-style-type: none"> 1. VCO calibration time impacts lock time and is modeled by the simulations. 2. This device has several different modes for the VCO calibration, but PLLatinum Sim only models the fastest and slowest methods. <ul style="list-style-type: none"> a) Regular Calibration (Modeled by PLLatinum Sim): This assumes no frequency specific settings from the user. b) Partially Assisted Calibration (NOT modeled by PLLatinum Sim): User gives the VCO starting core, capcode, and amplitude setting. c) Close Frequency Assist (NOT Modeled by PLLatinum Sim): The VCO uses the same VCO calibration that were used last -- very effective if the frequency change is small. d) Instant VCO Calibration (Modeled by PLLatinum Sim): The user locks the VCO to the desired frequency and reads back the VCO core, capcode, and amplitude settings. Then the next time, these settings are forced so that the VCO does not need to calibrate at all. <p>OK</p> </div> |
|--|---|

7.3 Graph Settings and Comparison Trace

| | |
|---|---|
|  <p>Graph Settings</p> <p>Points: 501</p> <p><input checked="" type="checkbox"/> Autoscale Axes</p> <p>min max</p> <p>X Axis: 0 100 us</p> <p>Y Axis: 4200 5400 MHz</p> <p><input type="checkbox"/> Load Comparison Trace ?</p> | <p>The graph settings are self-explanatory.</p> |
|  <p>Transient Response at Fout</p> <p>Frequency (MHz)</p> <p>Time(us)</p> <p>Legend: Analog Mo., Envelope+, Envelope-, Comparison</p> | <p>There is the option to load a comparison trace. The input format to this is:</p> <p><Time in Seconds> + Tab + <Frequency in Hz> + <Carriage Return></p> <p>The black trace is the simulated value where the red trace is the actual measurement.</p> |

7.4 VCO Calibration Time

| | |
|---|--|
|  <p>Noise Spurs LOCK Time Bode Plot</p> <p>VCO Calibration ?</p> <p>StartCore: VCO4 Cal Start Frequency: 10500 MHz</p> <p>? VCO Calibration Time: 31.6 us ? <input type="checkbox"/> Instant VCO Calibration</p> | <p>For devices with integrated VCO, the calibration time can also be modeled. Often there is a special speed-up mode that goes by different names (Called “Instant VCO Calibration”) for this device. Click the “?” for device specific information on this feature.</p> <p>The VCO Calibration Start group allows the user to specify the starting core and frequency. Depending on the device and choice for the special speed up mode this box will be labeled “Cal Start Frequency” or “Cal Assist Error”.</p> |
|---|--|

Frequency Response Box

Frequency Response ?

| | | | | | |
|------------------|------------|------------------|----------|--------------------|------------|
| Final Frequency | 4534.1 MHz | Analog Model | | Discrete Model | |
| Start Frequency | 4400 MHz | Analog Lock Time | 25 us | Discrete Lock Time | 24.9 us |
| Settle Tolerance | 1000 Hz | Total Lock Time | 56.6 us | Total Lock Time | 56.5 us |
| | | Peak Time | us | Peak Time | 100 us |
| | | Peak Frequency | 4400 MHz | Peak Frequency | 4534.1 MHz |

The frequency response box models the frequency response. The start and final frequencies have restrictions and get automatically updated based on these. The start and final frequencies have to use the same output divider, the Cal Start frequency updates the start frequency for some devices with VCO calibration, and the start and final frequencies cannot be outside the VCO range (including dividers/multipliers). The Analog Model assumes poles and zeros of the loop filter and uses the continuous time approximation to model the charge pump. The Discrete Model can be enabled to model the discrete modeling action of the phase detector.

7.5 Phase Response Box

Frequency Response ?

| | | | | | |
|------------------|------------|------------------|----------|--------------------|------------|
| Final Frequency | 4534.1 MHz | Analog Model | | Discrete Model | |
| Start Frequency | 4400 MHz | Analog Lock Time | 25 us | Discrete Lock Time | 24.9 us |
| Settle Tolerance | 1000 Hz | Total Lock Time | 56.6 us | Total Lock Time | 56.5 us |
| | | Peak Time | us | Peak Time | 100 us |
| | | Peak Frequency | 4400 MHz | Peak Frequency | 4534.1 MHz |

The phase response box models the phase of the output and lock time to a phase. A nonzero entry for the Phase Disturbance can be given to model a step response in phase and this is shown in the graph on the lower left.

7.6 Discrete Time Modeling of Lock Time

The discrete lock time modeling calculates the lock time by calculating the frequencies, phases, and loop filter voltages at every cycle of the charge pump. It is run whenever the “Calculate Discrete LT” button is pushed. Some things to keep in mind.

- The discrete lock time model works after the VCO calibration is finished. For the examples in this section, the VCO calibration was disabled to make the impact of the discrete lock time modeling more obvious.
- The discrete lock time model only calculates when “Calculate Discrete LT” button is pushed
- If the calculation takes longer than Max Calculation Time on the Main Diagram, it truncates the X axis time.

Discrete Lock Time Model ?

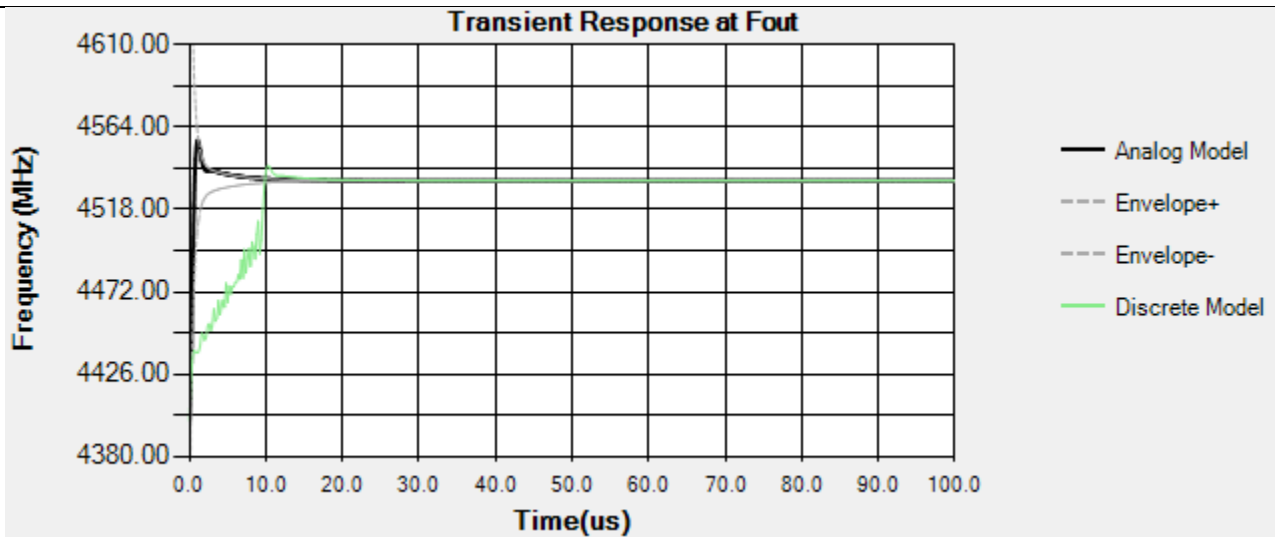
☐ Show Calculated Points

☐ Apply Non Ideal Modeling

Calculate Discrete LT

Cycle Slips 27

Time to First Cycle Slip 0.18 us



Frequency Response ?

Final Frequency 4534.1 MHz
Start Frequency 4400 MHz
Settle Tolerance 1000 Hz

Analog Model

Analog Lock Time 40.1 us
Total Lock Time 40.1 us
Peak Time 1 us
Peak Frequency 4555.8 MHz

Discrete Model

Discrete Lock Time 46.1 us
Total Lock Time 46.1 us
Peak Time 100 us
Peak Frequency 4534.1 MHz

Phase Response ?

Phase Disturbance 0 deg
Settle Tolerance 1 deg

Analog Model

Analog Lock Time 42 us
Total Lock Time 42 us
Peak Time .6 us
Peak Phase 34859.2 deg

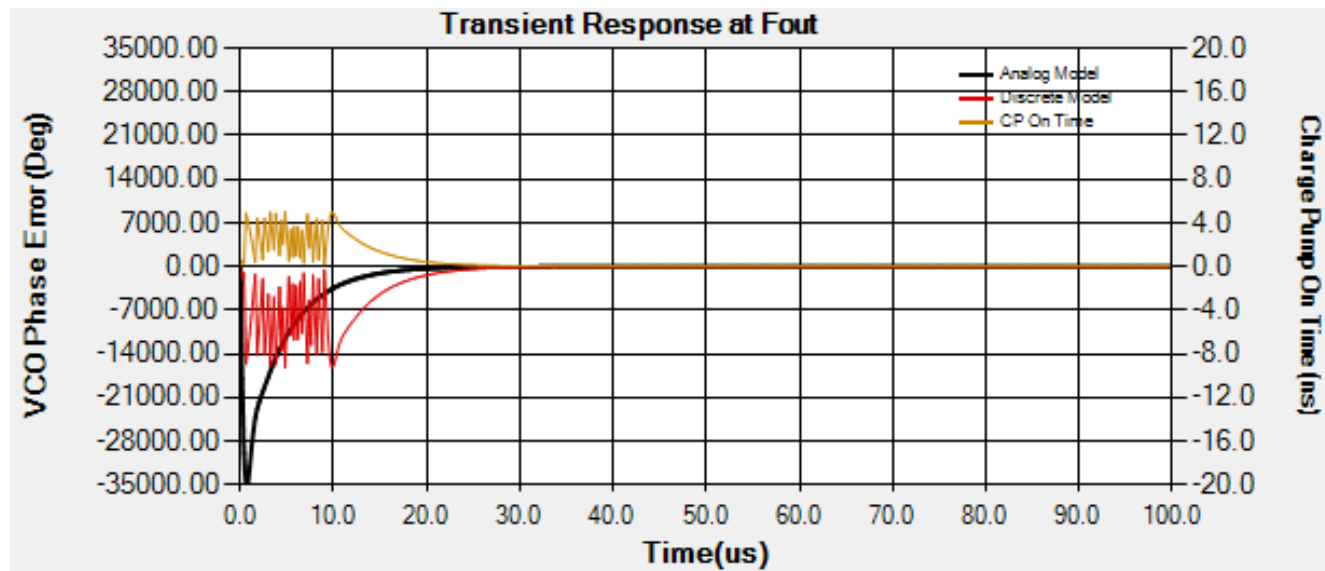
Discrete Model

Discrete Lock Time 48.1 us
Total Lock Time 48.1 us
Peak Time 7.2 us
Peak Phase -16321.9 deg

Comparing the discrete model to the analog model, we see that it shows the true transient response is slower due to the cycle slipping caused by the discrete sampling action of the phase detector.

7.6.1 Transient Phase Response for Discrete Modeling of Lock Time

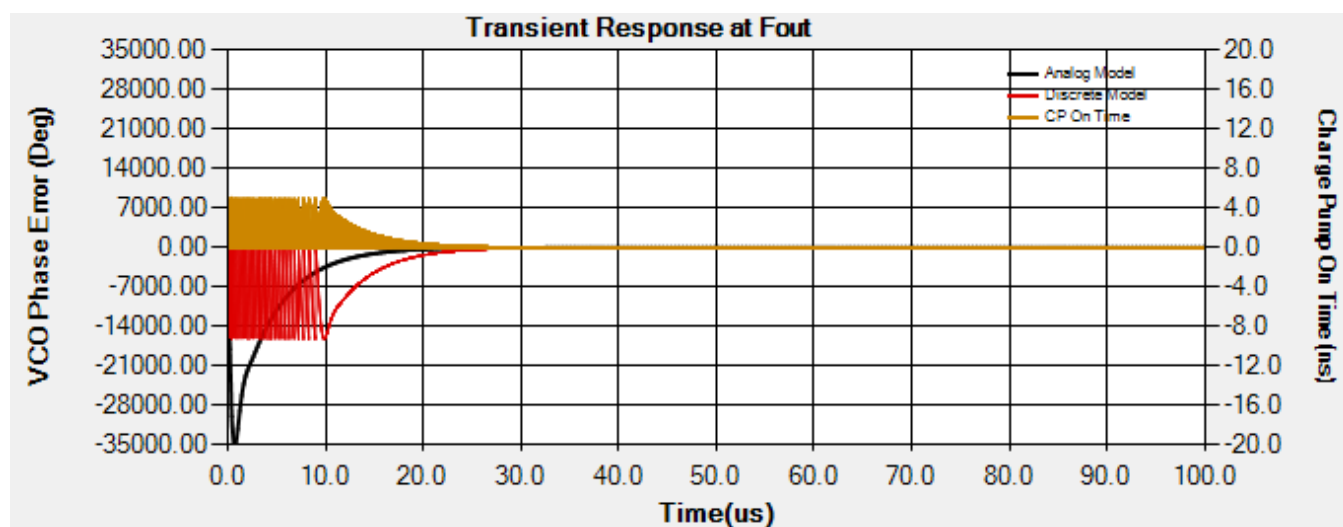
☐ Show Calculated Points



When lock time is modeled in a discrete way, the secondary lock time graph shows some additional information. It compares the analog and discrete modeling of the phase error. If the frequency change is small, then these graphs match at least a little. But if there is a large frequency change (relative to the loop bandwidth), then cycle slipping can occur and the discrete model shows a larger phase error and the graph may not show state phase error (although the actual PLL does settle to zero steady state phase). The charge pump on time shows how long the charge pump comes on. A negative time indicates that the charge pump is pumping in the negative direction. So a -8 ns charge pump on time means that the charge pump is sinking current for 8 ns.

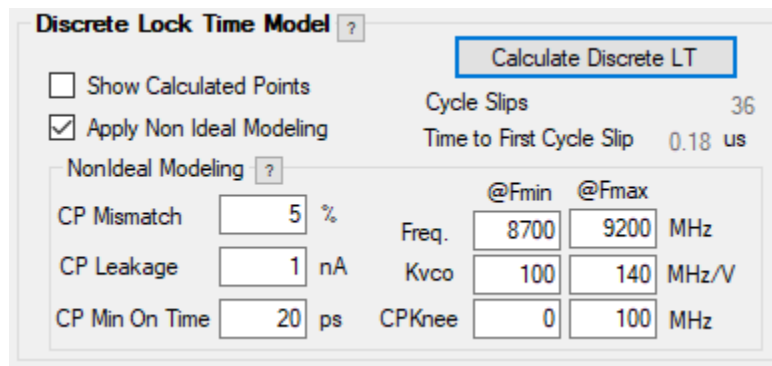
Clicking the "Show All Points" option is useful if one is interested in the charge pump on time. Often times, the number of points is too small to show all the interesting behavior, but checking this option calculates at every charge pump event to really show all the detail. **However, it ,may take much longer to calculate.**

☒ Show Calculated Points



7.6.2 Nonlinear Modeling of the Charge Pump

This is using the same example as before except now adding additional parameters for nonlinear modeling. One can enter a “0” in any of the fields to have it not impact calculations.



Charge Pump Mismatch, Leakage, and Minimum On Time

- **CP Mismatch** is the amount that the positive charge pump current is greater than the negative charge pump current
- **CP Leakage** is the amount of leakage current that occurs when the charge pump is off
- **CP Min On Time** is the minimum charge pump on time
- **CP On Time Low** is calculated on time for the last time the charge pump was sinking current.
- **CP On Time High** is calculated on time for the last time the charge pump was sourcing current.

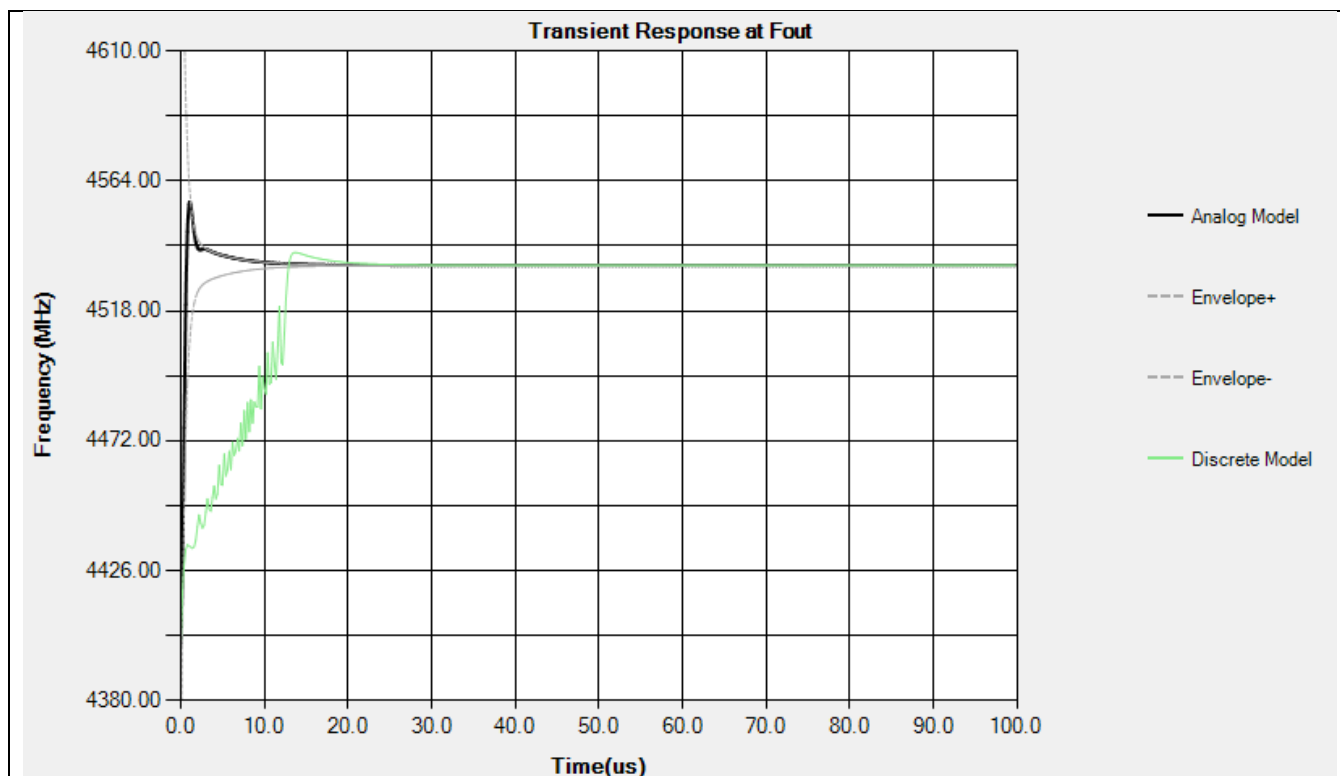
Modeling @Fmin and @Fmax

- **Freq.** specifies the minimum and maximum frequencies that apply to the two boxes below
- **Kvco** is the VCO gain at the above minimum and maximum VCO frequencies
- **CPKnee** is the knee for the charge pump and models the effect of the charge pump current being reduced when the tuning voltage is near the rails of the charge pump. CPKnee of “0” means disregard and CPKnee cannot be negative.

$$\begin{aligned} \text{Sink Current} &= -Kpd \cdot \left(1 - \exp\left(\frac{Fvco - Freq@Fmin}{CPKnee@Fmax}\right)\right) \\ \text{Source Current} &= Kpd \cdot \left(1 - \exp\left(\frac{Freq@Fmax - Fvco}{CPKnee@Fmin}\right)\right) \end{aligned}$$

Here is how the Kvco and charge pump current would be calculated for the above example.

| Frequency (MHz) | Kvco (MHz/V) | Sink Current | Source Current | Settings |
|-----------------|--------------|--------------------|----------------|---|
| 8700 | 84.2 | 0 | Kpd | Fmin = 8700 MHz Fmax = 9200 MHz CPKnee@Fmin = 0 MHz CPKnee@Fmax = 100 MHz Kvco@Fmin = 84.2 MHz Kvco@Fmax = 154.2 MHz |
| 8800 | 98.2 | $-0.632 \cdot Kpd$ | Kpd | |
| 8900 | 112.2 | $-0.865 \cdot Kpd$ | Kpd | |
| 9000 | 126.2 | $-0.950 \cdot Kpd$ | Kpd | |
| 9068.2 | 135.7 | $-0.975 \cdot Kpd$ | Kpd | |
| 9100 | 140.2 | $-0.982 \cdot Kpd$ | Kpd | |
| 9200 | 154.2 | $-0.993 \cdot Kpd$ | Kpd | |



Frequency Response ?

Final Frequency MHz
 Start Frequency MHz
 Settle Tolerance Hz

Analog Model
 Analog Lock Time 40.1 us
 Total Lock Time 40.1 us
 Peak Time 1 us
 Peak Frequency 4555.8 MHz

Discrete Model
 Discrete Lock Time 46.4 us
 Total Lock Time 46.4 us
 Peak Time 100 us
 Peak Frequency 4534.1 MHz

Phase Response ?

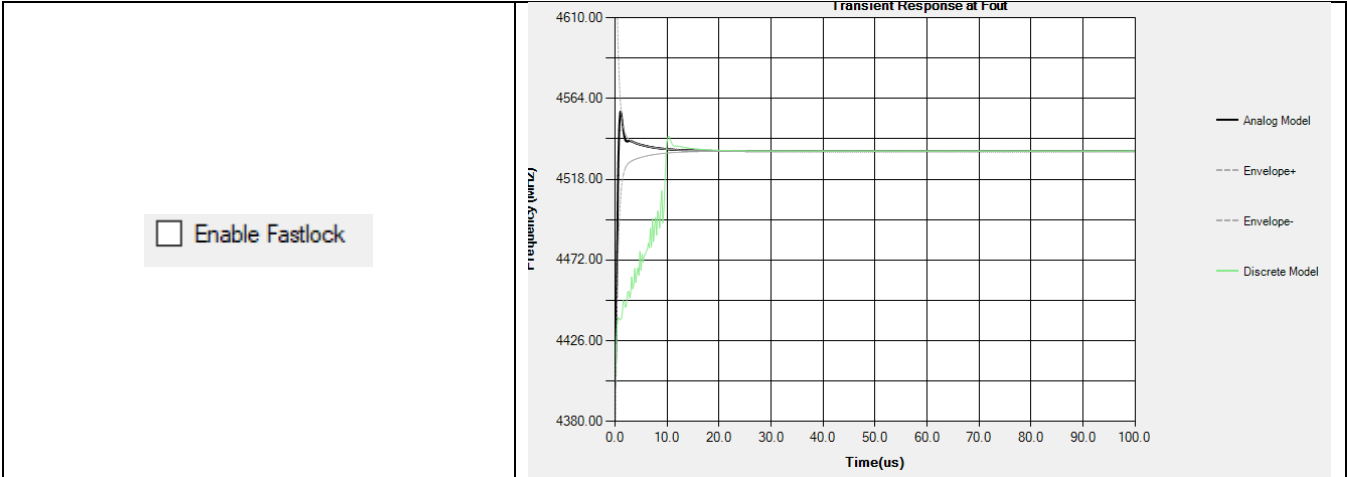
Phase Disturbance deg
 Settle Tolerance deg

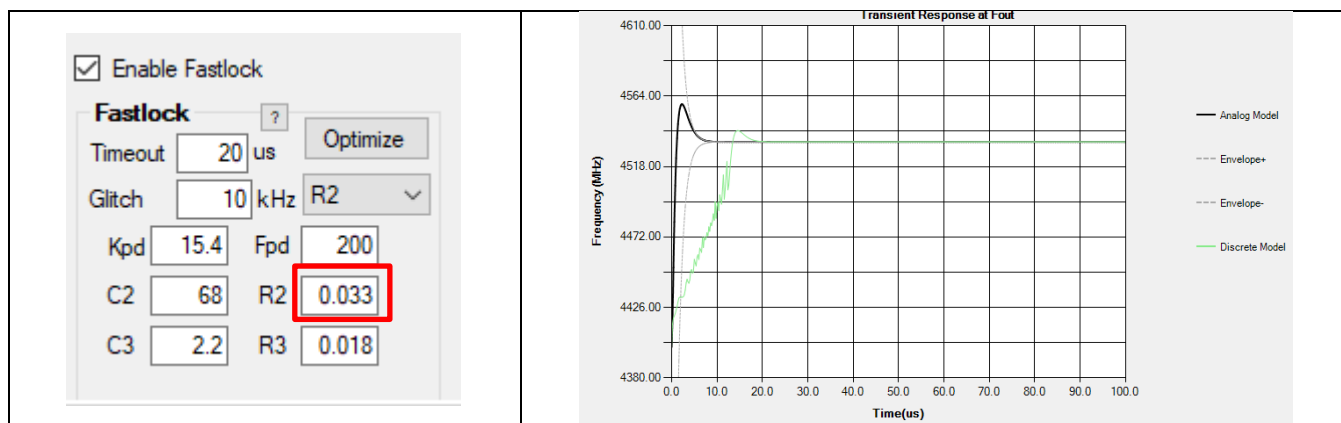
Analog Model
 Analog Lock Time 42 us
 Total Lock Time 42 us
 Peak Time .6 us
 Peak Phase 34859.2 deg

Discrete Model
 Discrete Lock Time 39.9 us
 Total Lock Time 39.9 us
 Peak Time 1 us
 Peak Phase -16288.8 deg

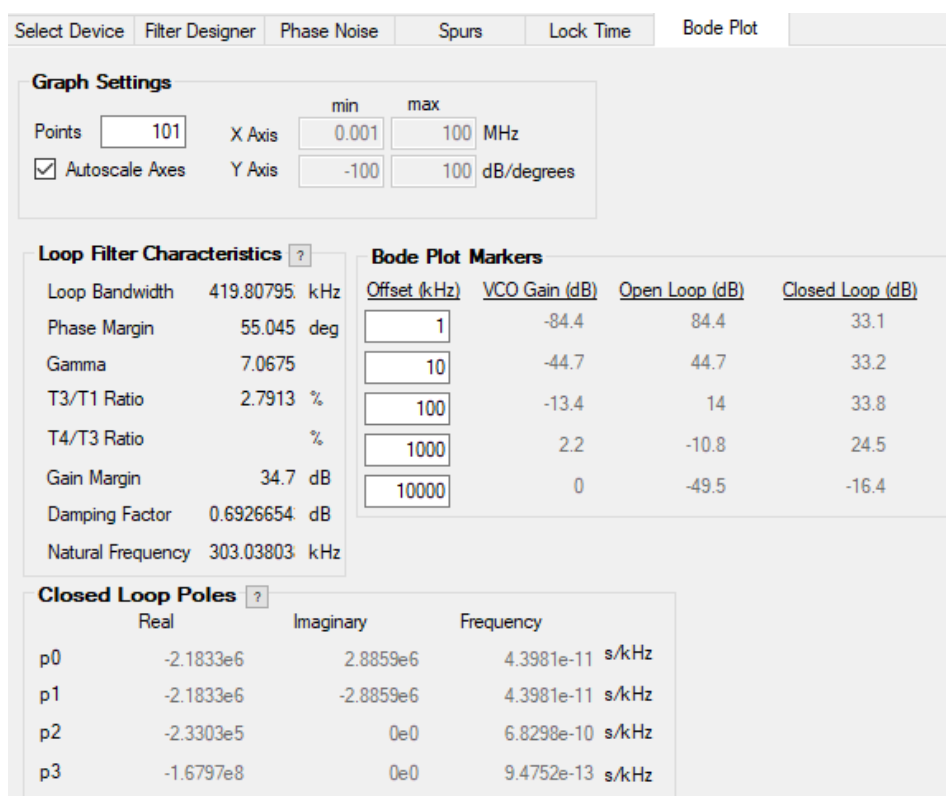
Comparing this to the example without the nonlinear modeling, we see that the lock time is slightly different

| | |
|---|--|
| <div><input checked="" type="checkbox"/> Enable Fastlock</div> | <p>Fastlock refers to switching in a faster switching loop filter initially when the analog lock time begins (after VCO frequency calibration) and then switching it out after a certain amount of time.</p> <p>Note: Although PLLatinum Sim may show Fastlock, this does not imply that the device has timeout counters, switches, and changeable charge pump gain to support Fastlock. In other words, external circuitry would be required if not integrated on the PLL IC itself.</p> |
| <div>Fastlock ? Timeout <input type="text" value="0"/> us <input type="button" value="Optimize"/> Glitch <input type="text" value="0"/> kHz <input type="button" value="Revert"/> <input type="button" value="v"/> Kpd <input type="text" value="15.4"/> Fpd <input type="text" value="200"/> C2 <input type="text" value="68"/> R2 <input type="text" value="0.068"/> C3 <input type="text" value="2.2"/> R3 <input type="text" value="0.018"/></div> | <p>Fastlock Settings</p> <ul style="list-style-type: none">• Timeout is how long fastlock is engaged before it is switched out.• Glitch is assumed glitch that occurs when fastlock is switched out.• Kpd is the effective charge pump current during fastlock.• Fpd is the effective phase detector frequency during fastlock.• C2, C3, C4, R2, R3, R4 are the effective loop filter values during fastlock. <p>Note: If one does NOT want the fastlock timeout count to be automatically applied and show when the discete model is calculated, ensure that the combination box is selected to anything but "Timeout"</p> |
| <div><input type="button" value="Optimize"/> <input type="button" value="R2"/> <input type="button" value="v"/></div> | <p>Fastlock Component Optimizer</p> <p>Pressing the Optimize button optimizes the component values to minimize lock time during fastlock. It has a few different options what to optimize</p> <ul style="list-style-type: none">• Timeout optimizes analog timeout count when the "Optimize" button is pushed. If discrete model is run with this option chosen and a nonzero option for the timeout count, it updates it for the optimal discrete model timeout count.• R2 optimizes only the effective value of R2• C2 optimizes only the effective value of C2• C3, C4, R2, R3, R4 optimizes these components.• All but C1 optimizes all components except C1.• Revert changes all component values back to the ones on the main diagram. |





8 Bode Plot Tab



8.1 Graph and Poles and Time Constants

