


NOTES, UNLESS OTHERWISE SPECIFIED:

1. The netname "P3V3" represents connection to the +3.3V power plane.
2. The netname "P1V8" represents connection to the +1.8V power plane.
3. The netname "V_OFFSET" represents connection to the +10V power plane.
4. The netname "V_RESET" represents connection to the -14V power plane.
5. The netname "V_BIAS" represents connection to the +18V power plane.
6. The symbol  represents connection to the digital ground plane.
7. A "Z" suffix on a signal name indicates an active low signal
8. All components with designators "U" are electrostatic discharge sensitive



INDEX

Sheet 1: Cover
Sheet 2: Front End Interface
Sheet 3: Power
Sheet 4: DMD
Sheet 5: Important Notice

COMPUTER GENERATED DRAWING - DO NOT REVISE MANUALLY

REVISIONS

REV	DESCRIPTION	DATE	APPROVED
A	ECO 2172111: Initial Release	2/8/2018	DH
B	Revision B	7/15/2019	DH
C	Revision C	2/6/2020	DH
D	Revision D	6/16/2020	DH
E	Revision E	9/24/2021	DH
F	Revision F	9/11/2023	MM

Rev. B

Changed P1P8V Net Name to VDD_DMD
Changed R8 Pin 2 connection from P1P8V to P1P8V_LDO
Changed R5 Pin 2 connection from P1P8V to P1P8V_LDO
Added net DMUX_LATCHED to J4 Pin 7
Added net LATCH_CLEAR to J4 Pin 8
Changed U3 Pin 5 from P1P8V to P1P8V_LDO
Added pads for R51 and R52 (Components DNI)
Added C178 (2.2uF) to V_OFFSET
Changed R12 Pin 2 connection from P1P8V to P1P8V_LDO
Added U19: 1.8V LDO supply for DLPC980 Logic Ref.
Added C180 (1uF), C181 (1uF), and R55 (10m) for 1.8V LDO circuit
Added C177 (2.2u) to V_OFFSET
Added R48 (10m), R49 (10m), and R50 (10m) - current monitoring resistors
R29 changed to 63.4k, 1% to adjust V_OFFSET voltage
R36 changed to 0 ohm to adjust compensation network
R42 changed to 1%
V_BIAS circuitry altered:
The output of the positive charge pump (U10 pin 17) is now fed into CPI (U16 pin 16).
V_BIAS is now output from the VGH pin (U16 pin 15)
Added C191, C192, and C193 to V_BIAS
Added C182, C183, C184 (10u) to V_OFFSET (near DMD)
Added C185, C186, C187 (10u) to V_RESET (near DMD)
Added C188, C189, C190 (10u) to V_BIAS (near DMD)
Added U18 to latch DMUX
Added R53, R54, R56, R57, and C179 for latch circuit
Added U22 and U23 buffers to account for VDD_DMD variation

Rev. C

J6 Pin 1 net changed from VDD_DMD to P1P8V_LDO
I2C level shifter removed, I2C from DLPC964 now at 3.3V
U1 removed
R5, R8 removed
VDD_DMD and VDDA_DMD Rails Separated
U2, U3, U4, U5 removed
FB5, FB6 removed
L1 removed
R11, R13, R14, R15, R16, R17, R51, R52 removed
C7, C8, C9, C10, C11, C12, C13, C14, C15, C16, C178 removed
TP3 removed
U24, U25 added
L3, L4 added
R58, R59, R60, R61, R62, R63, R64, R65 added
C194, C195, C196, C197, C198, C199 added
TP15, TP16 added
Net VDDA_DMD added
C39, C41, C44, C58, C68, C77, C82, C90, C94, C96, C97, C98, C106, C108, C128, C140, C141, C142, C148, C149, C155, C158, C159, C165, C168, C169, C170, C113, C115, C123, C124 changed from VDD_DMD to VDDA_DMD
Sheet 3 reference to DLPC980 updated to DLPC964 to reflect updated controller name
L2 (4.7uH), R36 (0), C25 (36pF), C31 (10uF), and C22 (1uF) devices updated to L2 (2.2uH), R36 (56.0K), C25 (47pF), C31 (0.33uF), and C22 (22uF)

Rev. D

L2 (4.7uH), R36 (0), C25 (36pF), C31 (10uF), and C22 (1uF) devices updated to L2 (2.2uH), R36 (56.0K), C25 (47pF), C31 (0.33uF), and C22 (22uF)

Rev. E

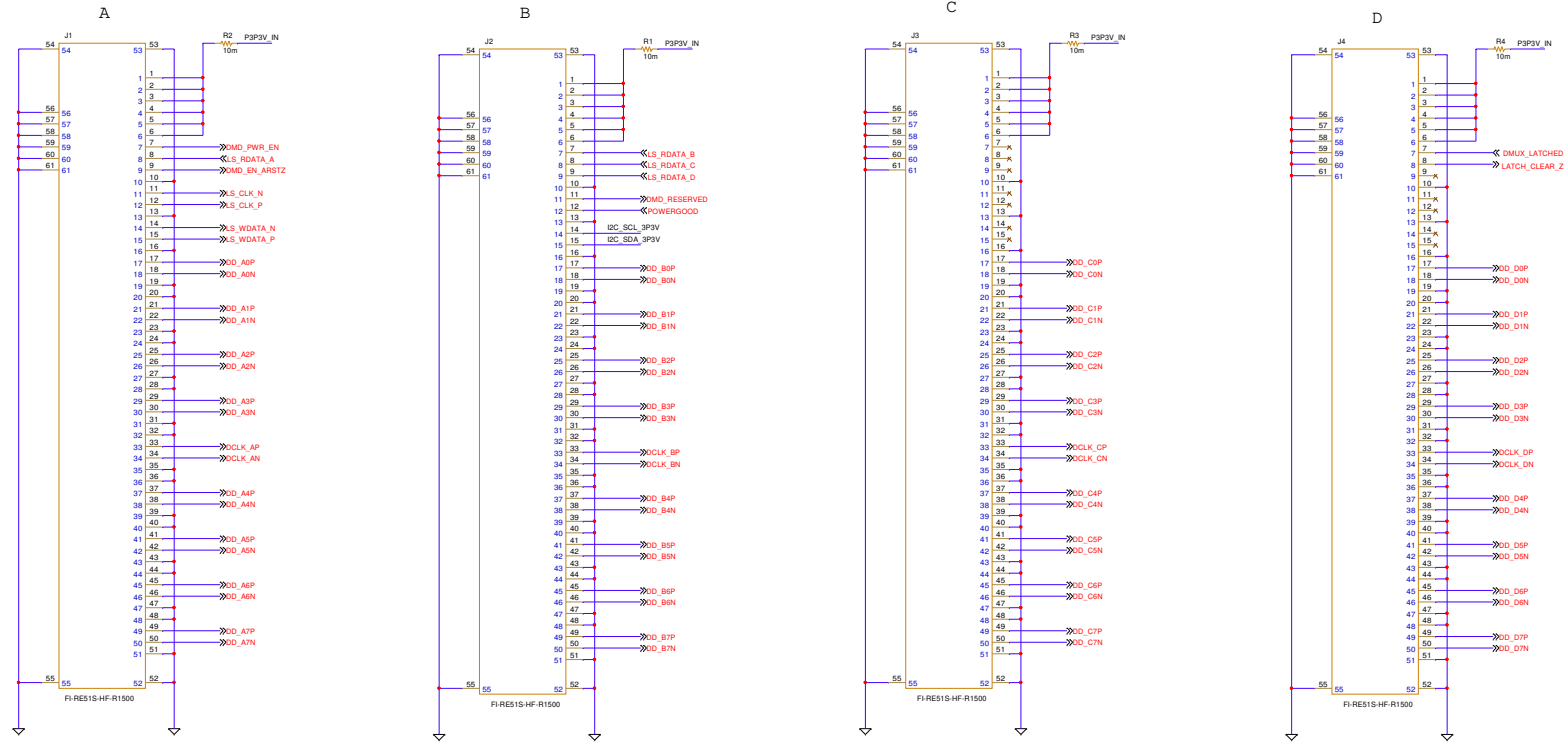
C18 (1000pF) updated to C18 (4700pF)
C27 updated to DNI (Do Not Install)

Rev. F

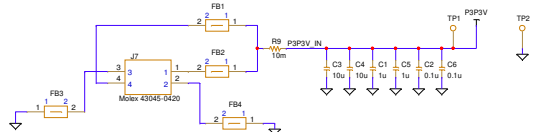
Title updated to "ESD, DLPLCR99UVEVM DMD Board for DLP991UUV L3 (470uH) and L4 (470uH) footprint update.
Values of each inductor stays the same, but footprint pads updated.
Components updated with alternative parts (Footprints remain the same):
R58, R64 -> 215K resistor replaced with 330K resistor
D1, D3-D7, D9 -> CUI510330 updated to PMEG3010 -> Vf updated from .23V to .28V
D2 -> STPS0540Z updated to CBDW0540 -> Vf updated from .5V to .51V
D8 -> M323V3B updated to TDZ3V3J115
U11 - U14 -> FDY302NZ updated to S11062X
U15 -> BSS84 (ONSEM) updated to BSS84 (MDD)
U17 -> TMP411 updated to ADT7461, Analog Digital part

		DWN	Ben Uhing	DATE	2/06/2020	TEXAS INSTRUMENTS (C) COPYRIGHT 2023 TEXAS INSTRUMENTS ALL RIGHTS RESERVED	
		ENGR	Mike McCormick		3/17/2018		
		SYST	Mike McCormick		3/17/2023		
		PRJ	Lida Zhu		1/26/2023		
		QA	Mark Dorak		1/26/2023	TITLE ESD, DLPLCR99UVEVM for DLP991UUV DMD	
NEXT ASSY	USED ON						
APPLICATION		SW	Cadence Capture V.17.2			A3 DRAWING NO	DLP070
						SCALE	SHEET 1 of 5
						REV	F

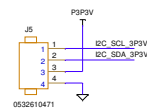
Flex Cable 51-pin Connectors to Emulation / ASIC boards



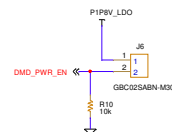
Alternate 3.3V Input



3.3V I2C Connector



Jumper to Enable DMD_PWR without connection to ASIC



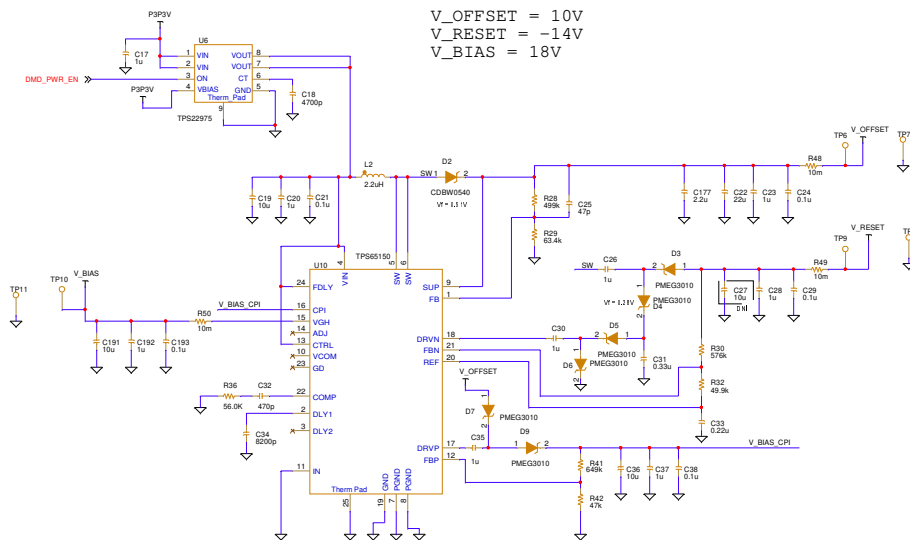
I2C Level Shifter (Removed)

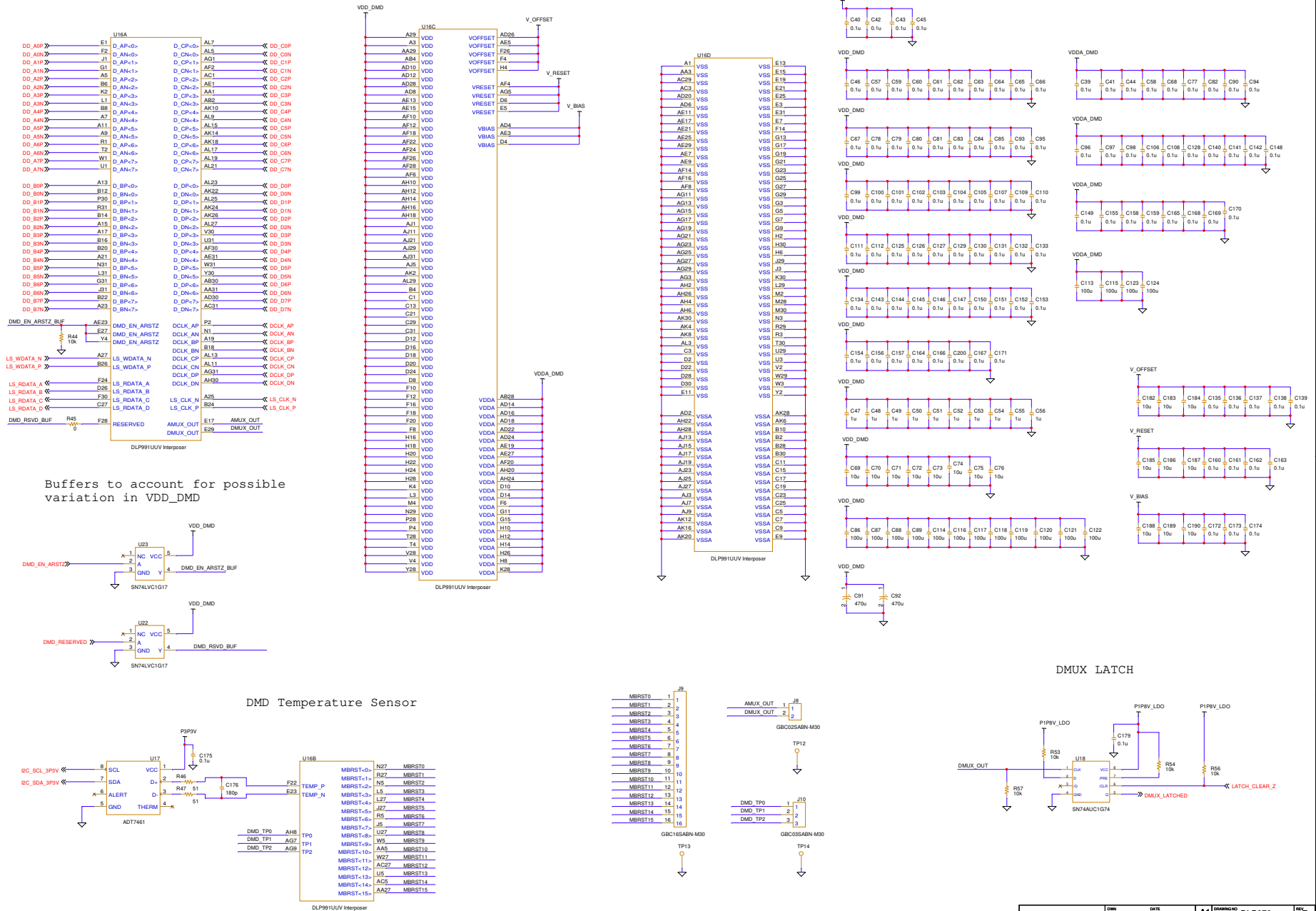


[illegible]

The schematic diagram shows the DMC_PWL_EN pin driver circuit. It starts with a P33V supply connected to a 4.7 uF capacitor (C197) and a 100k resistor (R62). The signal then passes through a U205 driver IC, which is configured with its 6-pin input (VIN) connected to the signal source, its 5-pin output (VOUT) connected to the output node, and its 4-pin enable (EN) connected to the DMD pin. The output node is connected to a 470 ohm resistor (L4) and a 100k resistor (R62). The output is also connected to TP16, VDDA, and DMD. A 300k resistor (R4) and a 100k resistor (R5) are connected to the output node. A 33uF capacitor (C199) is connected to the output node and ground.

```
V_OFFSET = 10V
V_RESET = -14V
V_BIAS = 18V
```

[illegible]



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TEXAS INSTRUMENTS	DWN Ben Uhing	DATE 10/02/2017	A3	DRAWING NO DLP070	REV F
	ISSUE DATE 3/15/2024				
				SCALE	SHEET 5 OF 5