NOTES, UNLESS OTHERWISE SPECIFIED:

1. The netname "P3P3V" represents connection to the +3.3V digital power plane.
2. The netname "P1P8V" represents connection to the +1.8V digital power plane.
3. The netname "P1P1V" represents connection to the +1.1V digital power plane.
4. The symbol ⏚ represents connection to the digital ground plane.
5. A "Z" suffix on a signal name indicates an active low signal.
6. A "_S" suffix on a signal name indicates a trace that is between a driver and a series termination resistor.
7. All components with designators "U", "D", "Y" and "Q" are electrostatic discharge sensitive.
8. The letters DNI near a part mean "do not install".

COMPUTER GENERATED DRAWING. DO NOT REVISE MANUALLY

REVISIONS

REV	DESCRIPTION	DATE	APPROVED
A	Initial Release		GP
B	Corrected wiring from DVI receiver to DLPC230. Changed DLPC230 pulldown on JTAGRSTZ to 1K. Changed C615-C618 to 22pF. Changed U511 to LCV1G04.		GP
C	Fixed TPS99000 connections for TIA_PD1_FILT and TIA_PD2_FILT. Added C642 to TPS99000 inductor LS net. Connected PWM1_COMPOUT_S to DLPC230 GPIO16. Changed R575 to DNI. Changed connector, diode and transistor part number attribute to non-visable. Added PCB part.	3/22/2018	GP

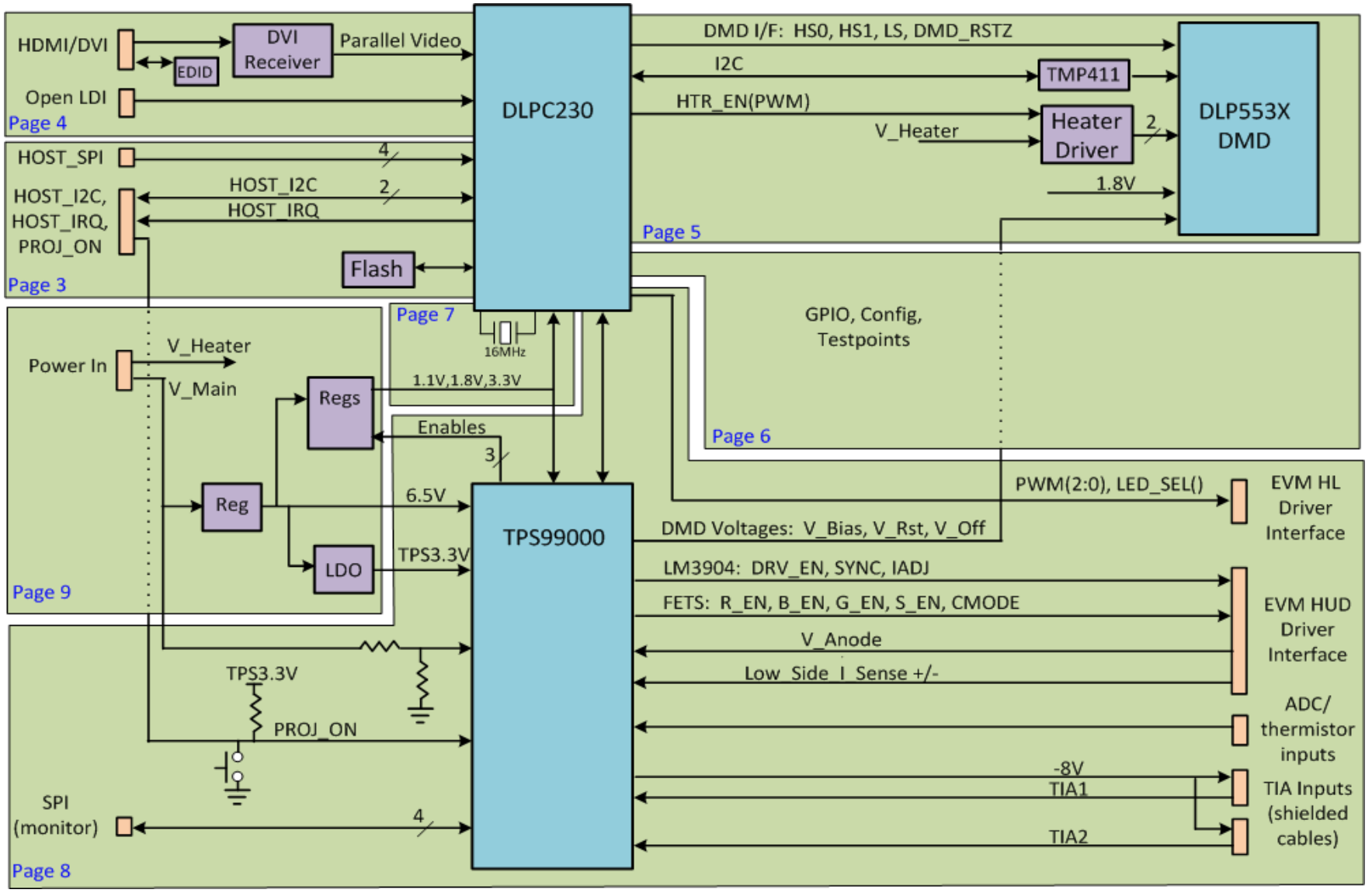
Z_PCB1

PCB, DLP553X Formatter
DLP005
2515619

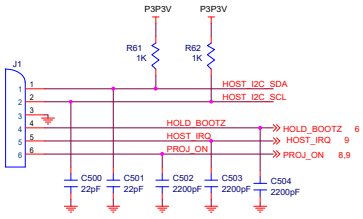
Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

TI Information - Selective Disclosure

		DWN George Pawlowski DATE 4/18/2017	TEXAS INSTRUMENTS (C) COPYRIGHT 2017 TEXAS INSTRUMENTS ALL RIGHTS RESERVED
		ENGR	
		SYST	
		PRJ	TITLE DLP553x EVM Formatter - DLP005
2515620			
NEXT ASSY	USED ON		D DRAWING NO 2515618 REV C
APPLICATION		SW Cadence Capture 16.6	SCALE SHEET 1 of 9

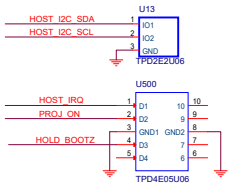


HOST I2C, PROJ_ON, IRQ, HOLD_BOOT CONNECTOR

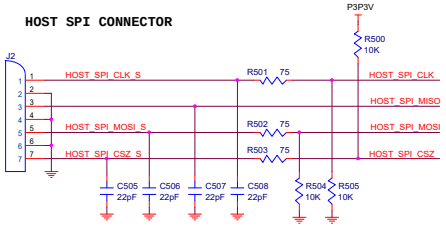


Capacitors to ground are for EMC reduction if needed.

ESD PROTECTION

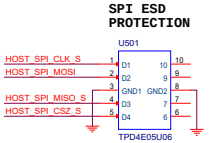


HOST SPI CONNECTOR

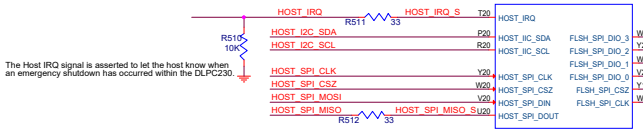


75 ohm series resistors are to reduce undershoot and overshoot with Cheetah adapter. Capacitors to ground are for EMC reduction if needed.

SPI ESD PROTECTION



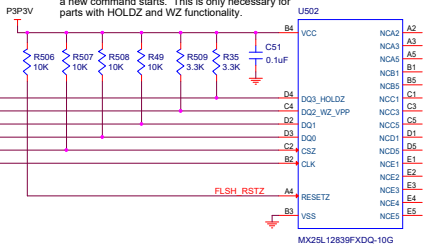
DLPC230 HOST INTERFACE

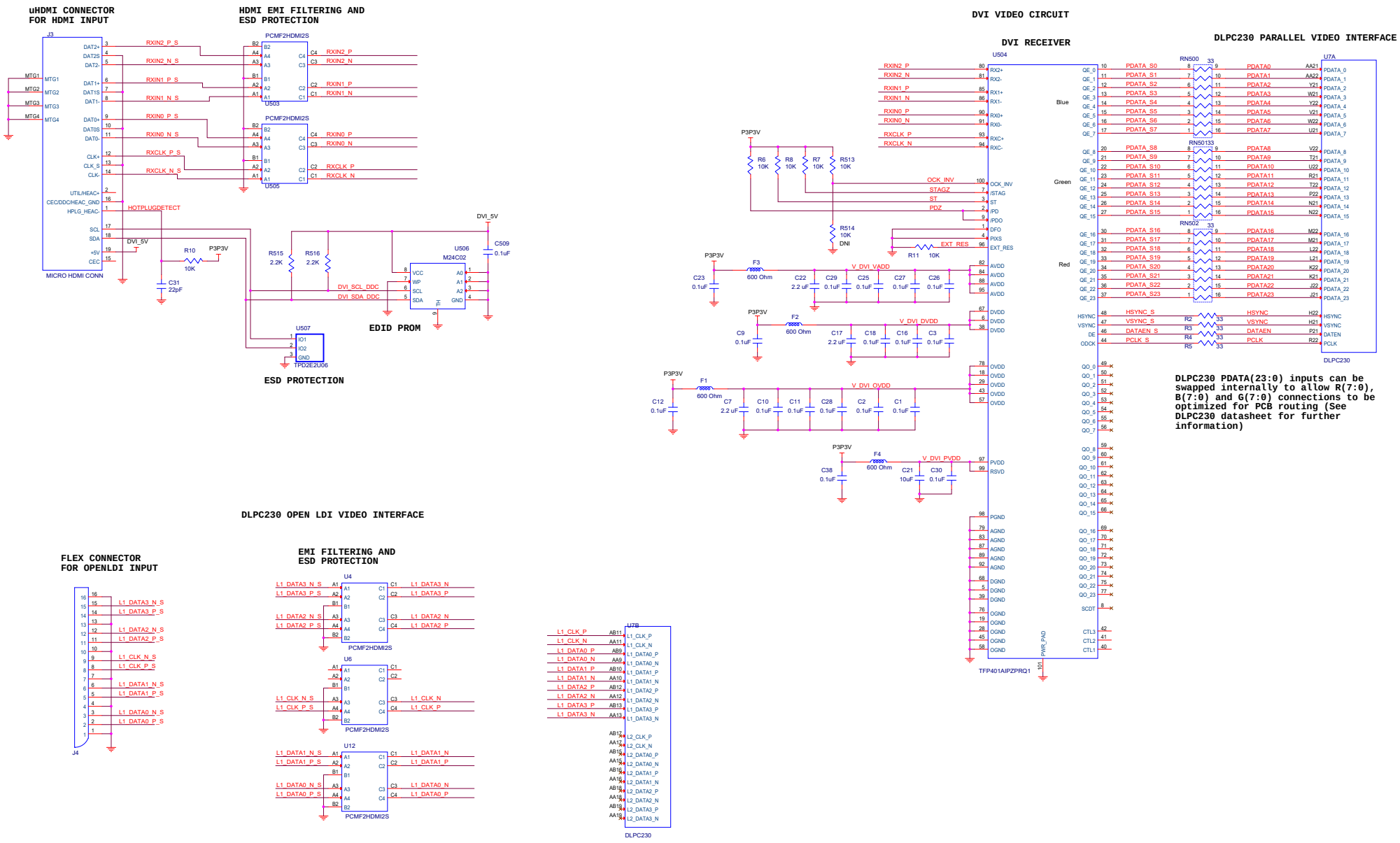


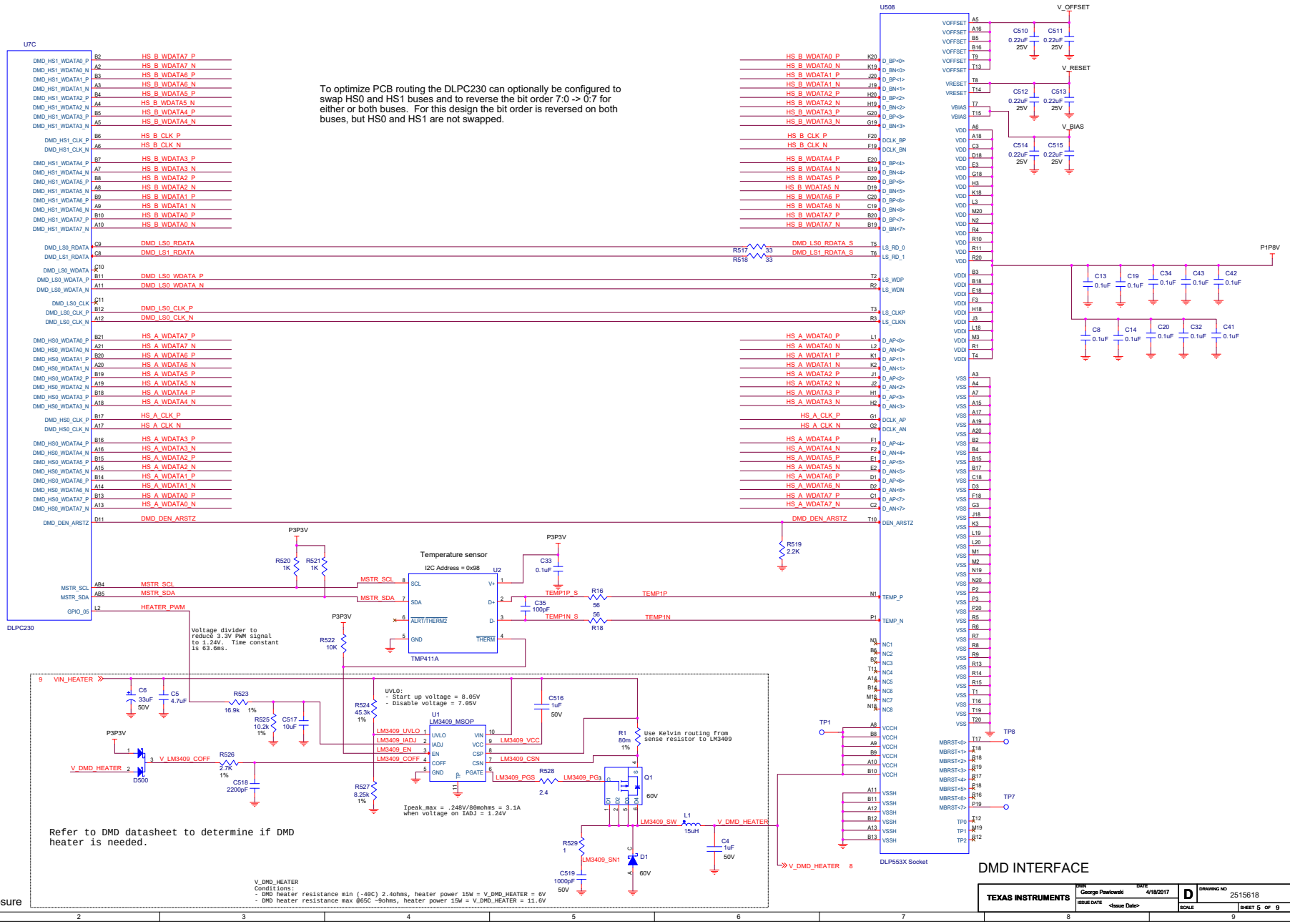
The Host IRQ signal is asserted to let the host know when an emergency shutdown has occurred within the DLPC230.

DLPC230 CONFIGURATION FLASH

DQ2 and DQ3 have smaller pullup resistors to ensure they are high after a quad operation before a new command starts. This is only necessary for parts with HOLDZ and WZ functionality.







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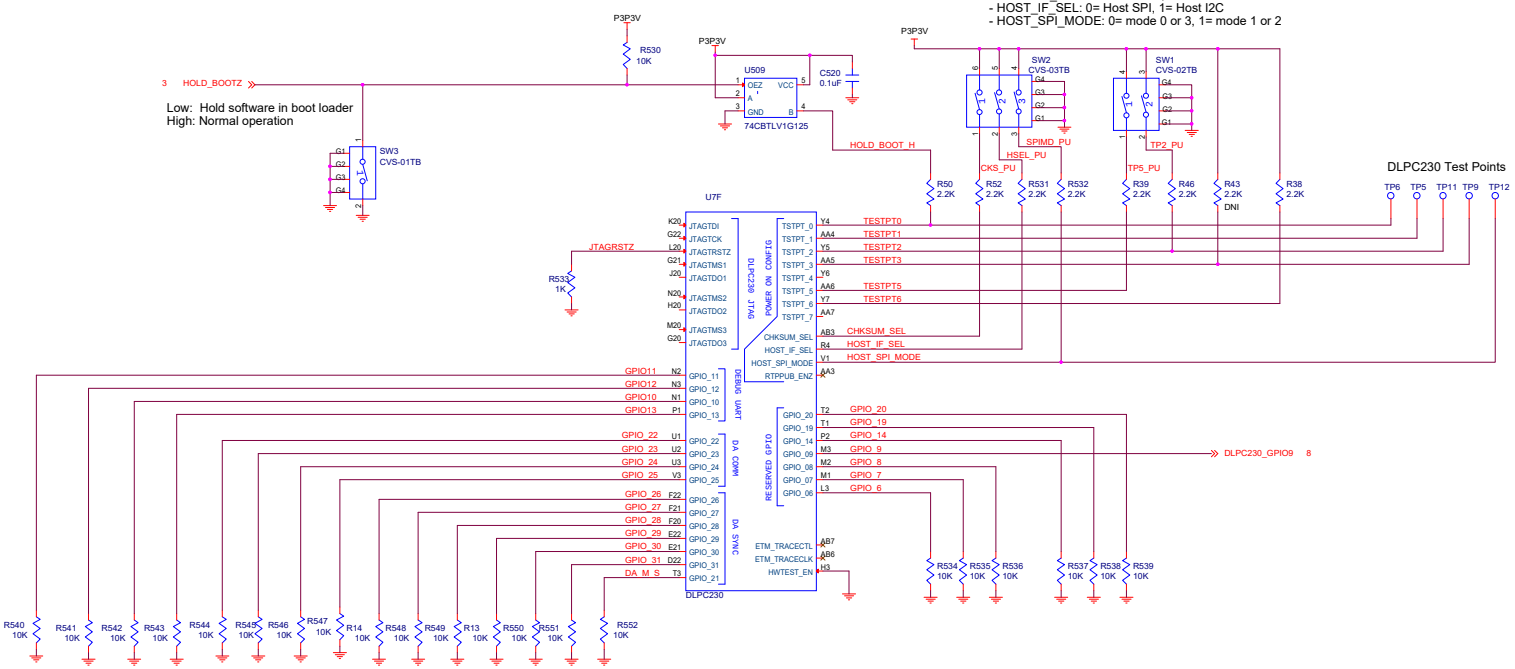
- TSTPT(7:0), CHKSUM_SEL, HOST_IF_SEL, HOST_SPI_SEL are inputs when RESETZ is low and have internal weak pulldown resistors. The states of the inputs are sampled after reset transitions from low to high to determine configuration options. Pins are then set as outputs.

CONFIGURATION OPTIONS
- TSTPT0 (STAY-IN-BOOT): 0= load main app, 1= stay in boot app
- TSTPT1 (EXT-BOOT-EN): 0= internal boot (must be low)
- TSTPT2 (I2C-ADDR-SEL): 0=0x36, 1=0x34
- TSTPT3 (ALT-MADR-SEL): 0= load main app 1, 1= load main app 2
- TSTPT4 (BOOT-SPI-MASTER-EN): 0= disabled (must by low)
- TSTPT5 (Spread Spectrum Enable): 0= disabled, 1= enabled
- TSTPT6 (Crystal Frequency): 0= reserved, 1= 16MHz (must be high)
- CHKSUM_SEL: 0= 8 bit CRC, 1= 8 bit checksum
- HOST_IF_SEL: 0= Host SPI, 1= Host I2C
- HOST_SPI_MODE: 0= mode 0 or 3, 1= mode 1 or 2



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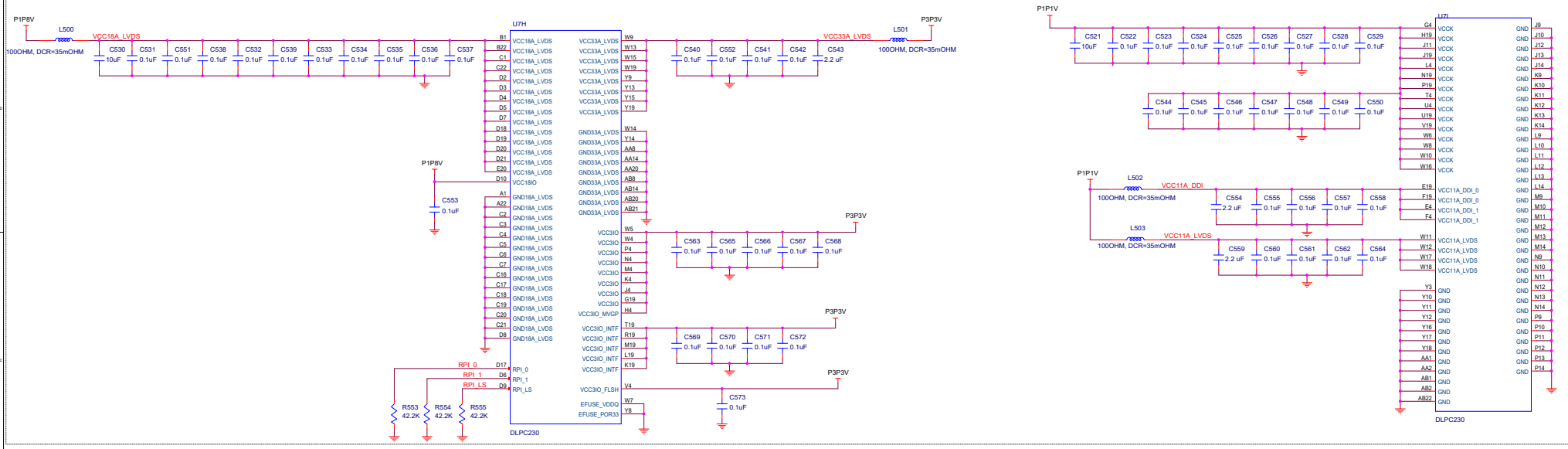
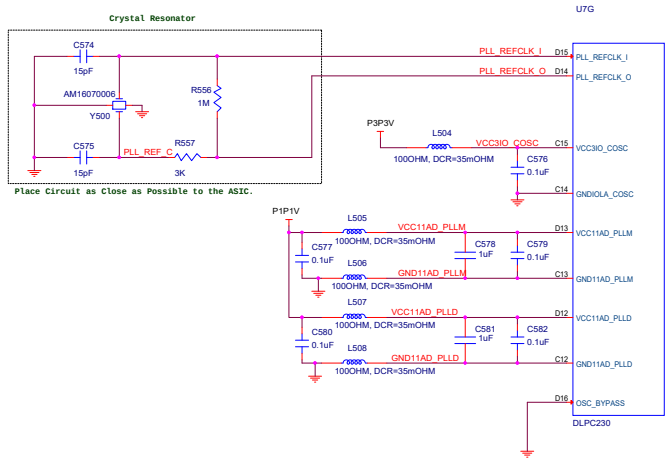
DLPC230 POWER



DLPC230 REFERENCE CLOCK INTERFACE



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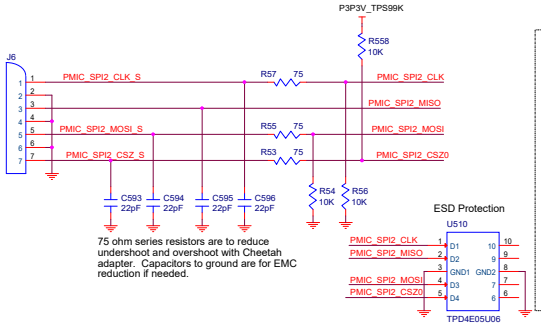
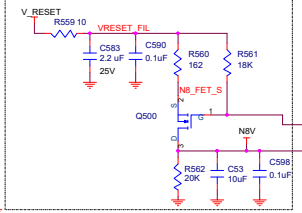
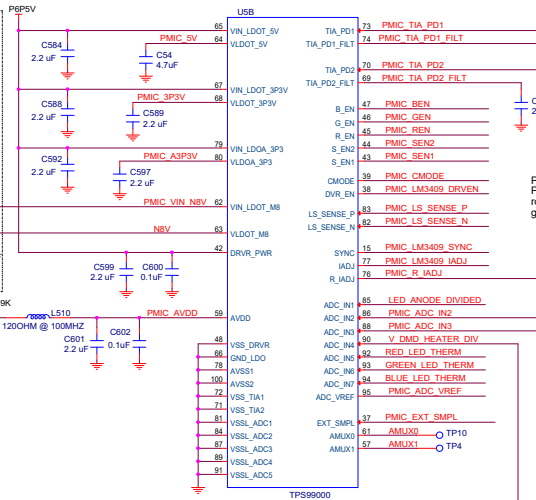
TPS99000 SPI DEBUG CONNECTOR



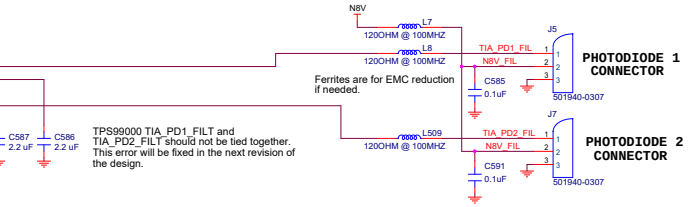
If photodiodes are not needed then negative 8V (N8V) circuit can be removed as long as negative 8V regulator it is not enabled in software configuration. TPS99000 pins VIN_LDOT_M8 and VLDOT_M8 can be left unconnected.



TPS99000 ANALOG INTERFACE

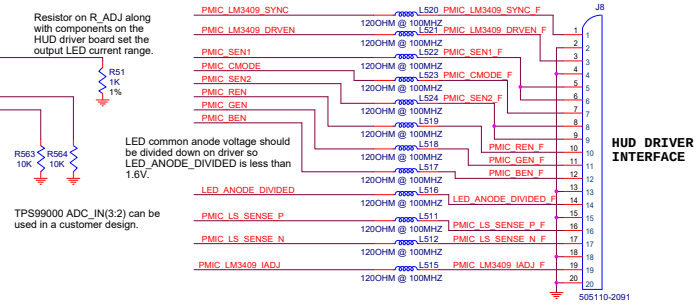


TPS99000 TIA_PD1_FILT and TIA_PD2_FILT should not be tied together. This error will be fixed in the next revision of the design.



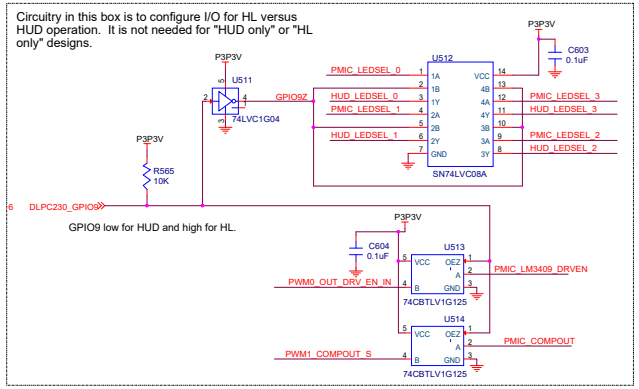
PMIC_LS_SENSE_P and PMIC_LS_SENSE_N should be routed tightly coupled with ground gaurd traces.

Resistor on R_ADJ along with components on the HUD driver board set the output LED current range.

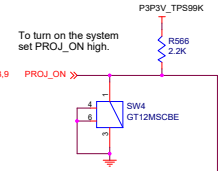


TPS99000 ADC_IN(3:2) can be used in a customer design.

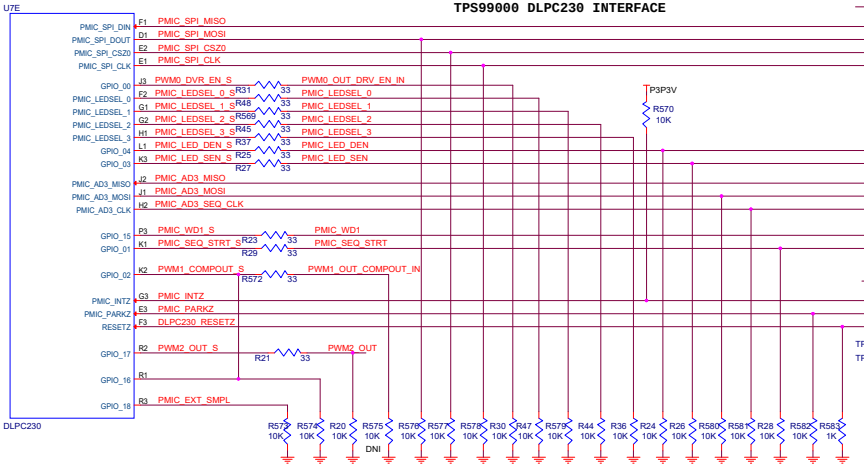
Circuitry in this box is to configure I/O for HL versus HUD operation. It is not needed for "HUD only" or "HL only" designs.

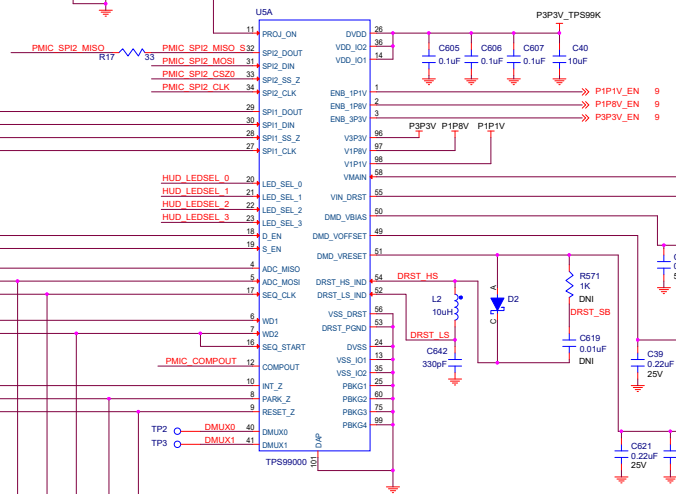


To turn on the system set PROJ_ON high.

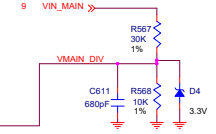


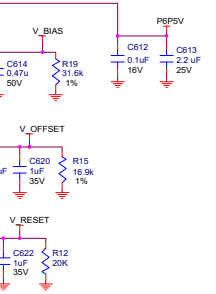
TPS99000 DLPC230 INTERFACE



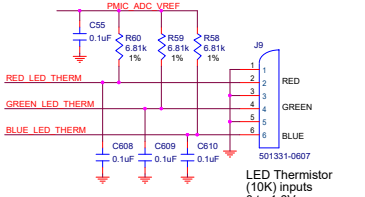


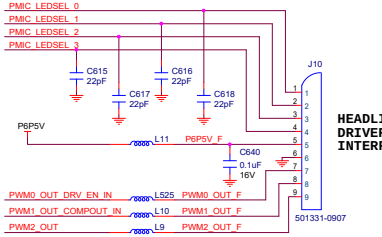
VMAIN shutdown threshold set to 5V (VMAIN_DIV = 1.25 when VBATT = 5V). 5.1us time constant filter.





Resistors to ground on V_reset, V_offset and V_bias are to insure minimum load current of 0.5mA.





Ferrites and capacitors to ground are for EMC reduction if needed. Note that COMP_OUT from TPS99000 is sensitive to capacitive loading.

TPS99000 Interface

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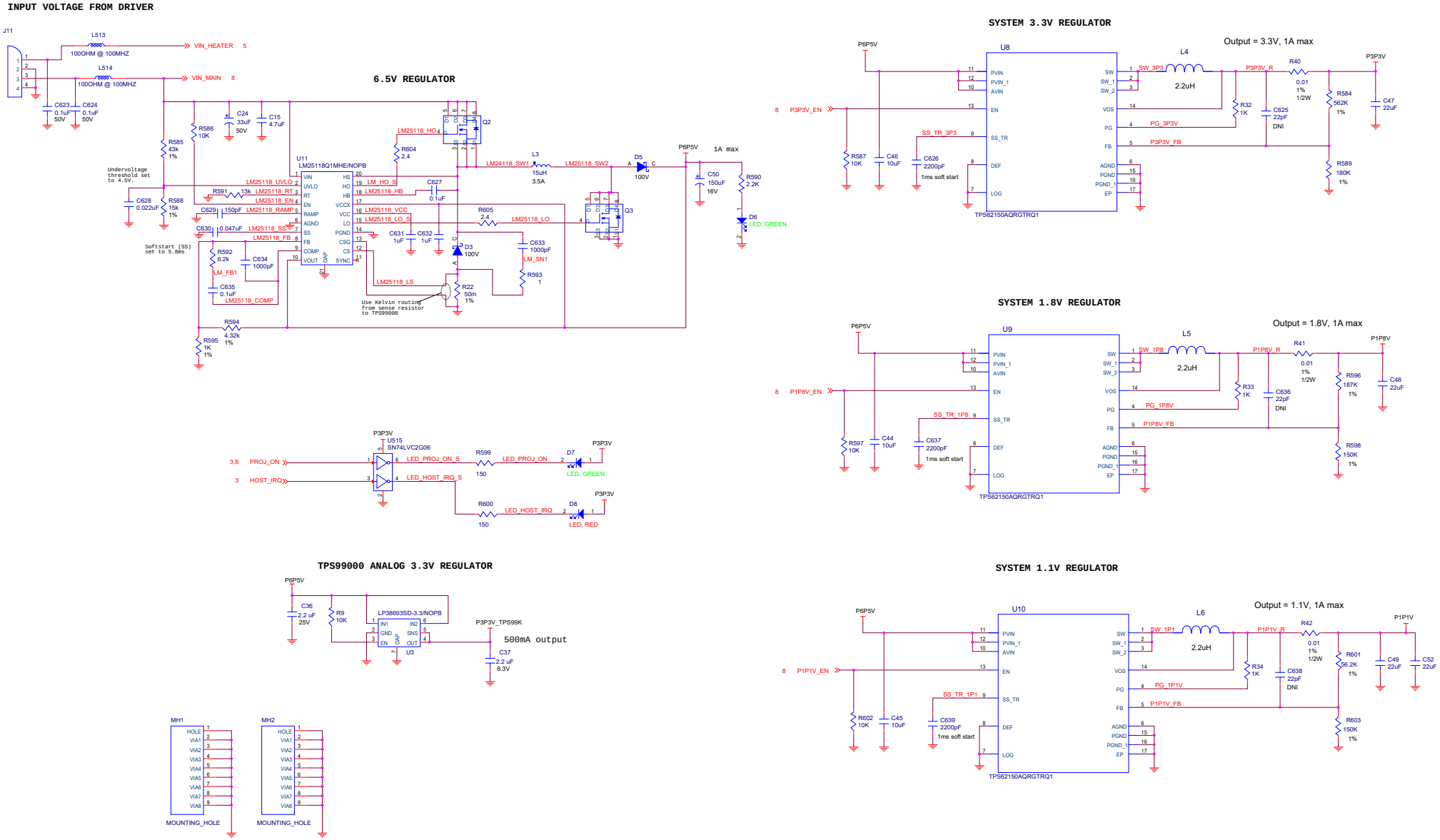

TEXAS INSTRUMENTS	DWN George Pawlowski	DATE 4/18/2017	D	DRAWING NO 2515618	REV C
	ISSUE DATE <Issue Date>			SCALE	SHEET 9 OF 9