

NOTES, UNLESS OTHERWISE SPECIFIED:

1. The netname "P3P3V" represents connection to the +3.3V digital power plane.
2. The netname "P1P8V" represents connection to the +1.8V digital power plane.
3. The netname "P1P1V" represents connection to the +1.1V digital power plane.
4. The symbol ∇ represents connection to the digital ground plane.
5. A "Z" suffix on a signal name indicates an active low signal.
6. A "_S" suffix on a signal name indicates a trace that is between a driver and a series termination resistor.
7. All components with designators "U", "D", "Y" and "Q" are electrostatic discharge sensitive.
8. The letters DNI near a part mean "do not install".

IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (<http://www.ti.com/sc/docs/stdterms.htm>) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's noncompliance with the terms and provisions of this Notice.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2017, Texas Instruments Incorporated

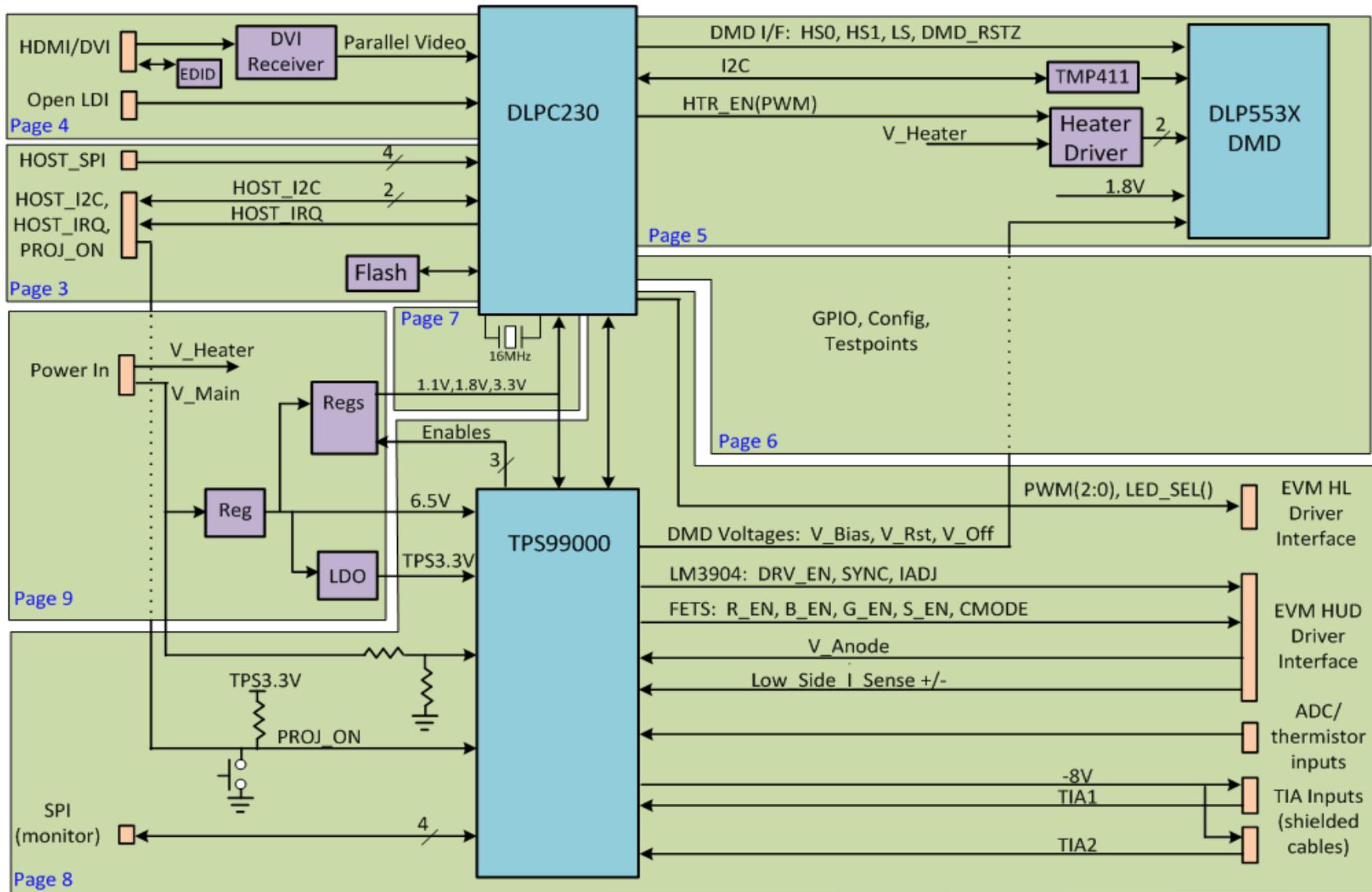
COMPUTER GENERATED DRAWING. DO NOT REVISE MANUALLY			
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
A	Initial Release		GP
B	Corrected wiring from DVI receiver to DLPC230. Changed DLPC230 pulldown on JTAGRSTZ to 1k. Changed C615-C618 to 22pF. Changed U511 to LCV1G04.		GP
C	Fixed TPS99000 connections for TIA_PD1_FILTER and TIA_PD2_FILTER. Added C642 to TPS99000 inductor_LS net. Connected PWM1_COMPOUT_S to DLPC230 GPIO16. Changed R575 to DNI. Changed connector, diode and transistor part number attribute to non-visible. Added PCB part.	3/22/2018	GP

Z_PCB1

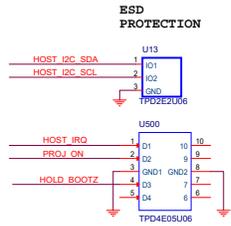
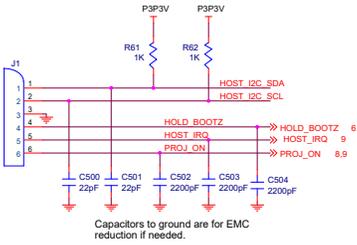
PCB_DLP553X Formatter
DLP005
2515619



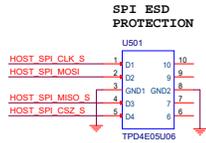
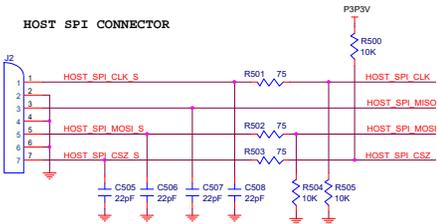
	DWN	George Pawlowski	DATE	4/18/2017	TEXAS INSTRUMENTS (C) COPYRIGHT 2017 TEXAS INSTRUMENTS ALL RIGHTS RESERVED				
	ENGR								
	SYST								
	PRJ								
	TITLE				DLP553x EVM Formatter - DLP005				
2515620									
NEXT ASSY	USED ON				D	DRAWING NO	2515618	REV	C
APPLICATION		SW	Cadence Capture 16.8		SCALE	SHEET 1 of 9			



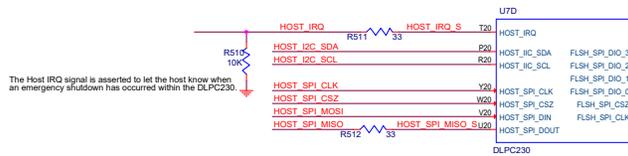
HOST I2C, PROJ_ON, IRQ, HOLD_BOOT CONNECTOR



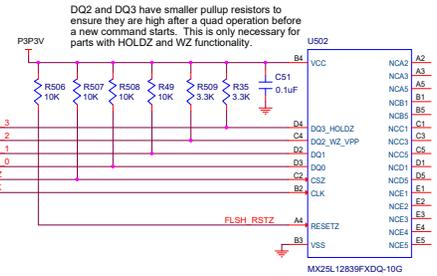
HOST SPI CONNECTOR



DLPC230 HOST INTERFACE

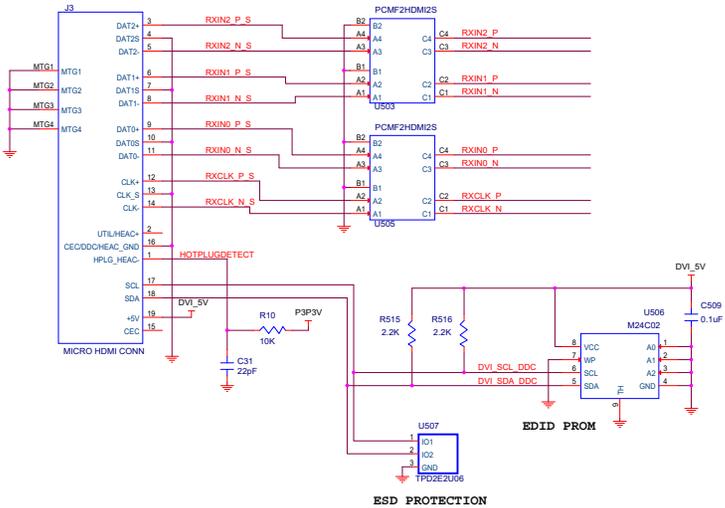


DLPC230 CONFIGURATION FLASH



UHDMI CONNECTOR FOR HDMI INPUT

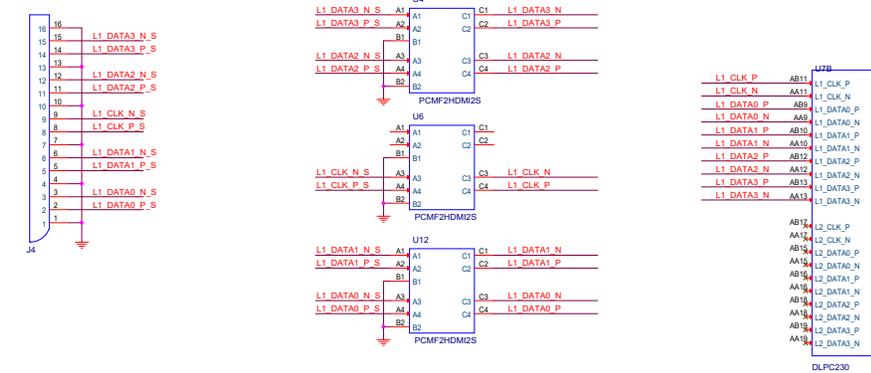
HDMI EMI FILTERING AND ESD PROTECTION



DLPC230 OPEN LDI VIDEO INTERFACE

FLEX CONNECTOR FOR OPENLDI INPUT

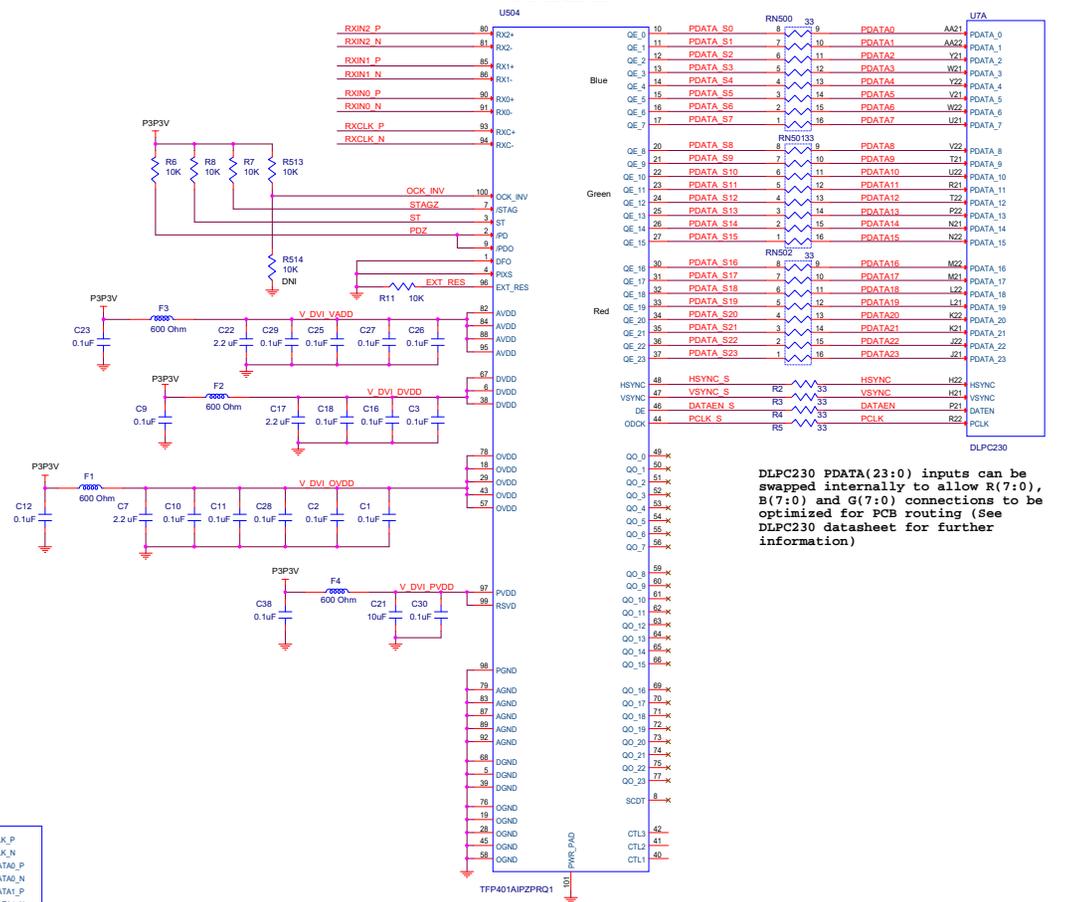
EMI FILTERING AND ESD PROTECTION



DVI VIDEO CIRCUIT

DVI RECEIVER

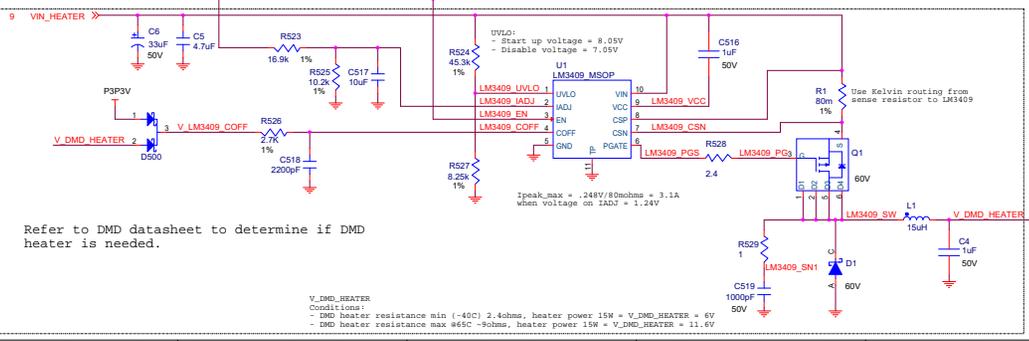
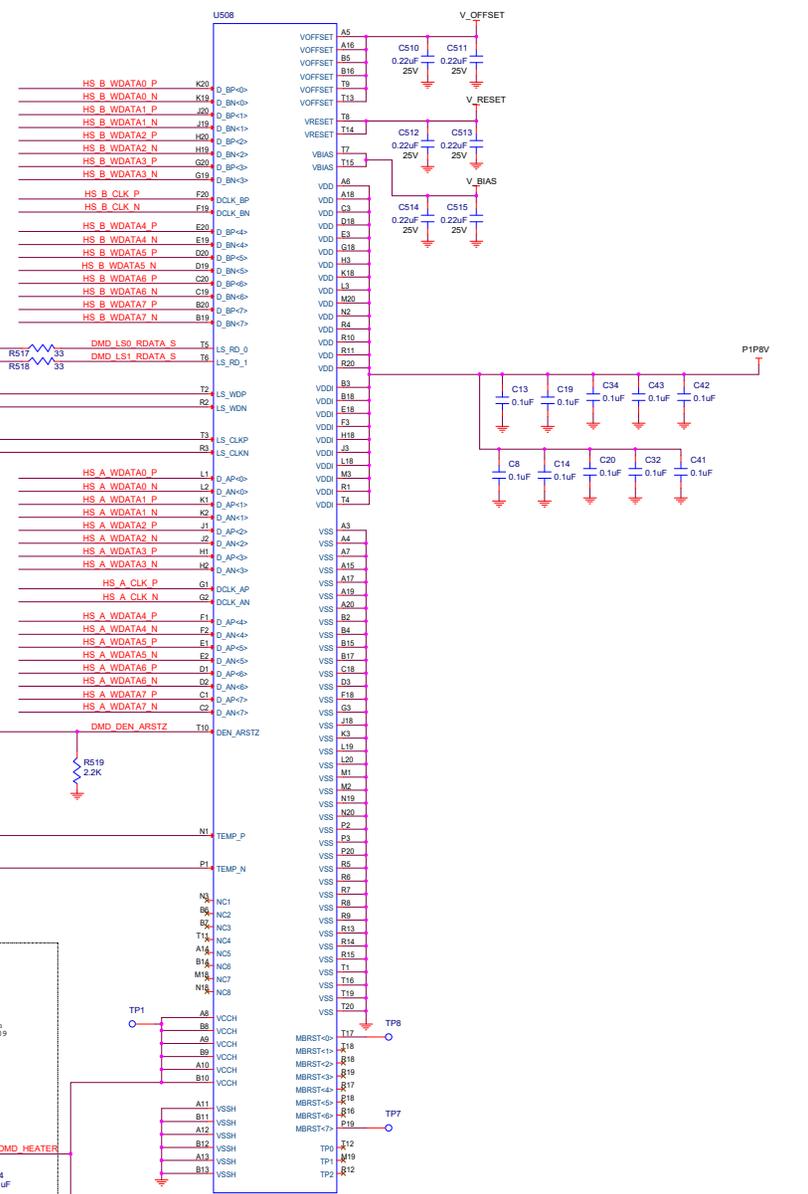
DLPC230 PARALLEL VIDEO INTERFACE



DLPC230 PDATA(23:0) inputs can be swapped internally to allow R(7:0), B(7:0) and G(7:0) connections to be optimized for PCB routing (See DLPC230 datasheet for further information)

DMD_HS1_WDATA0_P	B2	HS_B_WDATA7_P
DMD_HS1_WDATA0_N	A2	HS_B_WDATA7_N
DMD_HS1_WDATA1_P	B3	HS_B_WDATA6_P
DMD_HS1_WDATA1_N	A3	HS_B_WDATA6_N
DMD_HS1_WDATA2_P	B4	HS_B_WDATA5_P
DMD_HS1_WDATA2_N	A4	HS_B_WDATA5_N
DMD_HS1_WDATA3_P	B5	HS_B_WDATA4_P
DMD_HS1_WDATA3_N	A5	HS_B_WDATA4_N
DMD_HS1_CLK_P	B6	HS_B_CLK_P
DMD_HS1_CLK_N	A6	HS_B_CLK_N
DMD_HS1_WDATA4_P	B7	HS_B_WDATA3_P
DMD_HS1_WDATA4_N	A7	HS_B_WDATA3_N
DMD_HS1_WDATA5_P	B8	HS_B_WDATA2_P
DMD_HS1_WDATA5_N	A8	HS_B_WDATA2_N
DMD_HS1_WDATA6_P	B9	HS_B_WDATA1_P
DMD_HS1_WDATA6_N	A9	HS_B_WDATA1_N
DMD_HS1_WDATA7_P	B10	HS_B_WDATA0_P
DMD_HS1_WDATA7_N	A10	HS_B_WDATA0_N
DMD_LSO_RDATA	C9	DMD_LSO_RDATA
DMD_LSO_RDATA	C8	DMD_LSO_RDATA
DMD_LSO_WDATA	B11	DMD_LSO_WDATA_P
DMD_LSO_WDATA	A11	DMD_LSO_WDATA_N
DMD_LSO_CLK	C11	DMD_LSO_CLK_P
DMD_LSO_CLK_P	B12	DMD_LSO_CLK_P
DMD_LSO_CLK_N	A12	DMD_LSO_CLK_N
DMD_HS0_WDATA0_P	B21	HS_A_WDATA7_P
DMD_HS0_WDATA0_N	A21	HS_A_WDATA7_N
DMD_HS0_WDATA1_P	B20	HS_A_WDATA6_P
DMD_HS0_WDATA1_N	A20	HS_A_WDATA6_N
DMD_HS0_WDATA2_P	B19	HS_A_WDATA5_P
DMD_HS0_WDATA2_N	A19	HS_A_WDATA5_N
DMD_HS0_WDATA3_P	B18	HS_A_WDATA4_P
DMD_HS0_WDATA3_N	A18	HS_A_WDATA4_N
DMD_HS0_CLK_P	B17	HS_A_CLK_P
DMD_HS0_CLK_N	A17	HS_A_CLK_N
DMD_HS0_WDATA4_P	B16	HS_A_WDATA3_P
DMD_HS0_WDATA4_N	A16	HS_A_WDATA3_N
DMD_HS0_WDATA5_P	B15	HS_A_WDATA2_P
DMD_HS0_WDATA5_N	A15	HS_A_WDATA2_N
DMD_HS0_WDATA6_P	B14	HS_A_WDATA1_P
DMD_HS0_WDATA6_N	A14	HS_A_WDATA1_N
DMD_HS0_WDATA7_P	B13	HS_A_WDATA0_P
DMD_HS0_WDATA7_N	A13	HS_A_WDATA0_N
DMD_DEN_ARSTZ	D11	DMD_DEN_ARSTZ

To optimize PCB routing the DLPC230 can optionally be configured to swap HS0 and HS1 buses and to reverse the bit order 7:0 -> 0:7 for either or both buses. For this design the bit order is reversed on both buses, but HS0 and HS1 are not swapped.

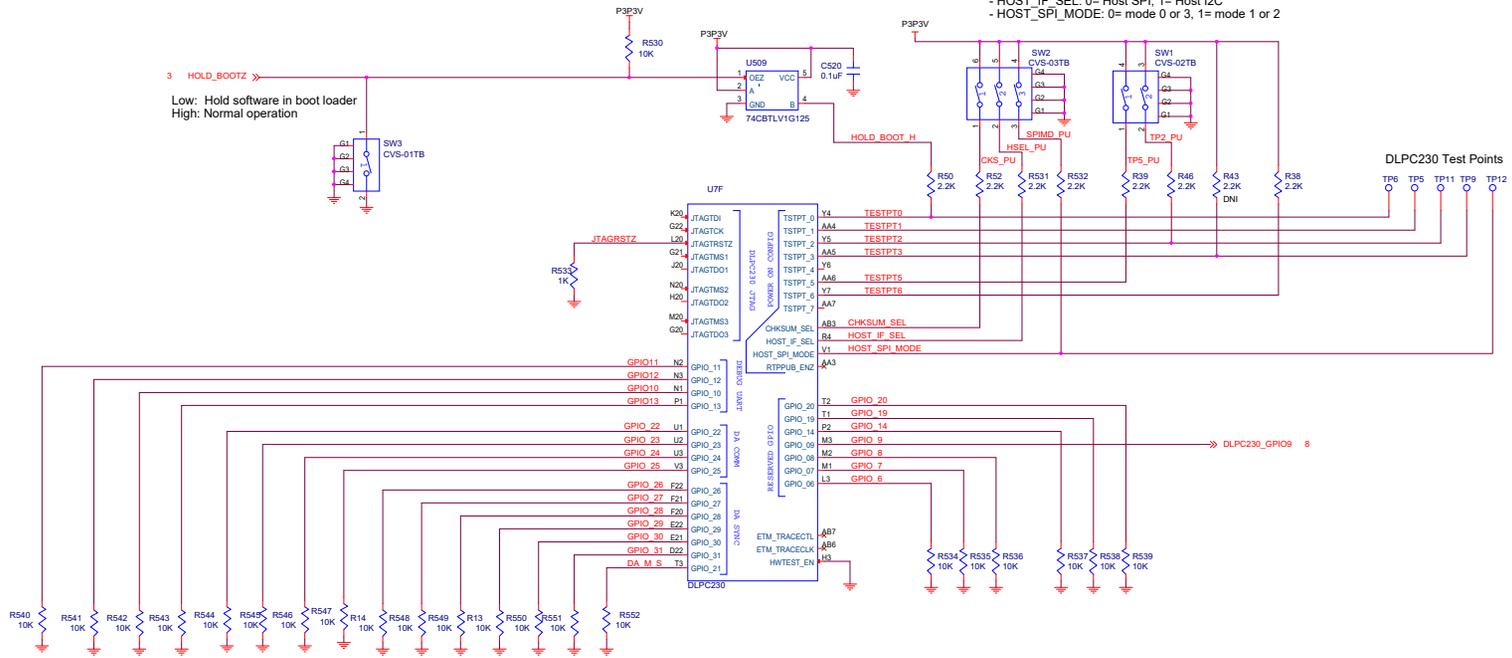


DMD INTERFACE

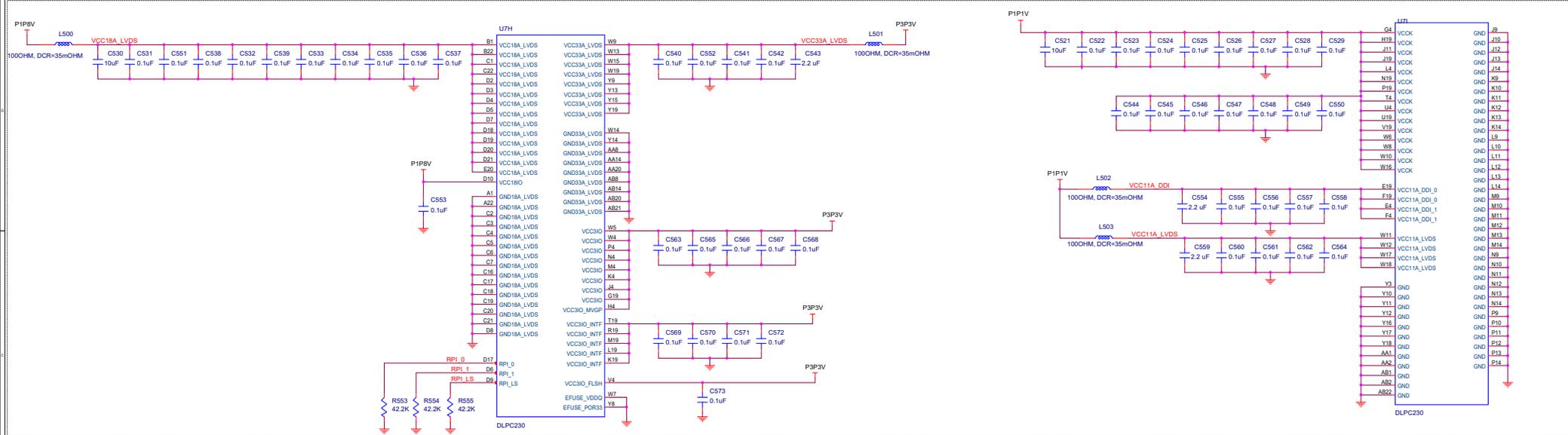
TP1	A8	ICCH
TP2	B8	ICCH
TP3	A9	ICCH
TP4	B9	ICCH
TP5	A10	ICCH
TP6	B10	ICCH
TP7	A11	VSSH
TP8	B11	VSSH
TP9	A12	VSSH
TP10	B12	VSSH
TP11	A13	VSSH
TP12	B13	VSSH
TP13	A14	VSSH
TP14	B14	VSSH
TP15	A15	VSSH
TP16	B15	VSSH
TP17	A16	VSSH
TP18	B16	VSSH
TP19	A17	VSSH
TP20	B17	VSSH
TP21	A18	VSSH
TP22	B18	VSSH
TP23	A19	VSSH
TP24	B19	VSSH
TP25	A20	VSSH
TP26	B20	VSSH
TP27	A21	VSSH
TP28	B21	VSSH
TP29	A22	VSSH
TP30	B22	VSSH
TP31	A23	VSSH
TP32	B23	VSSH
TP33	A24	VSSH
TP34	B24	VSSH
TP35	A25	VSSH
TP36	B25	VSSH
TP37	A26	VSSH
TP38	B26	VSSH
TP39	A27	VSSH
TP40	B27	VSSH
TP41	A28	VSSH
TP42	B28	VSSH
TP43	A29	VSSH
TP44	B29	VSSH
TP45	A30	VSSH
TP46	B30	VSSH
TP47	A31	VSSH
TP48	B31	VSSH
TP49	A32	VSSH
TP50	B32	VSSH
TP51	A33	VSSH
TP52	B33	VSSH
TP53	A34	VSSH
TP54	B34	VSSH
TP55	A35	VSSH
TP56	B35	VSSH
TP57	A36	VSSH
TP58	B36	VSSH
TP59	A37	VSSH
TP60	B37	VSSH
TP61	A38	VSSH
TP62	B38	VSSH
TP63	A39	VSSH
TP64	B39	VSSH
TP65	A40	VSSH
TP66	B40	VSSH
TP67	A41	VSSH
TP68	B41	VSSH
TP69	A42	VSSH
TP70	B42	VSSH
TP71	A43	VSSH
TP72	B43	VSSH
TP73	A44	VSSH
TP74	B44	VSSH
TP75	A45	VSSH
TP76	B45	VSSH
TP77	A46	VSSH
TP78	B46	VSSH
TP79	A47	VSSH
TP80	B47	VSSH
TP81	A48	VSSH
TP82	B48	VSSH
TP83	A49	VSSH
TP84	B49	VSSH
TP85	A50	VSSH
TP86	B50	VSSH
TP87	A51	VSSH
TP88	B51	VSSH
TP89	A52	VSSH
TP90	B52	VSSH
TP91	A53	VSSH
TP92	B53	VSSH
TP93	A54	VSSH
TP94	B54	VSSH
TP95	A55	VSSH
TP96	B55	VSSH
TP97	A56	VSSH
TP98	B56	VSSH
TP99	A57	VSSH
TP100	B57	VSSH
TP101	A58	VSSH
TP102	B58	VSSH
TP103	A59	VSSH
TP104	B59	VSSH
TP105	A60	VSSH
TP106	B60	VSSH
TP107	A61	VSSH
TP108	B61	VSSH
TP109	A62	VSSH
TP110	B62	VSSH
TP111	A63	VSSH
TP112	B63	VSSH
TP113	A64	VSSH
TP114	B64	VSSH
TP115	A65	VSSH
TP116	B65	VSSH
TP117	A66	VSSH
TP118	B66	VSSH
TP119	A67	VSSH
TP120	B67	VSSH
TP121	A68	VSSH
TP122	B68	VSSH
TP123	A69	VSSH
TP124	B69	VSSH
TP125	A70	VSSH
TP126	B70	VSSH
TP127	A71	VSSH
TP128	B71	VSSH
TP129	A72	VSSH
TP130	B72	VSSH
TP131	A73	VSSH
TP132	B73	VSSH
TP133	A74	VSSH
TP134	B74	VSSH
TP135	A75	VSSH
TP136	B75	VSSH
TP137	A76	VSSH
TP138	B76	VSSH
TP139	A77	VSSH
TP140	B77	VSSH
TP141	A78	VSSH
TP142	B78	VSSH
TP143	A79	VSSH
TP144	B79	VSSH
TP145	A80	VSSH
TP146	B80	VSSH
TP147	A81	VSSH
TP148	B81	VSSH
TP149	A82	VSSH
TP150	B82	VSSH
TP151	A83	VSSH
TP152	B83	VSSH
TP153	A84	VSSH
TP154	B84	VSSH
TP155	A85	VSSH
TP156	B85	VSSH
TP157	A86	VSSH
TP158	B86	VSSH
TP159	A87	VSSH
TP160	B87	VSSH
TP161	A88	VSSH
TP162	B88	VSSH
TP163	A89	VSSH
TP164	B89	VSSH
TP165	A90	VSSH
TP166	B90	VSSH
TP167	A91	VSSH
TP168	B91	VSSH
TP169	A92	VSSH
TP170	B92	VSSH
TP171	A93	VSSH
TP172	B93	VSSH
TP173	A94	VSSH
TP174	B94	VSSH
TP175	A95	VSSH
TP176	B95	VSSH
TP177	A96	VSSH
TP178	B96	VSSH
TP179	A97	VSSH
TP180	B97	VSSH
TP181	A98	VSSH
TP182	B98	VSSH
TP183	A99	VSSH
TP184	B99	VSSH
TP185	A100	VSSH
TP186	B100	VSSH

- TSTPT(7:0), CHKSUM_SEL, HOST_IF_SEL, HOST_SPI_SEL are inputs when RESETZ is low and have internal weak pulldown resistors. The states of the inputs are sampled after reset transitions from low to high to determine configuration options. Pins are then set as outputs.

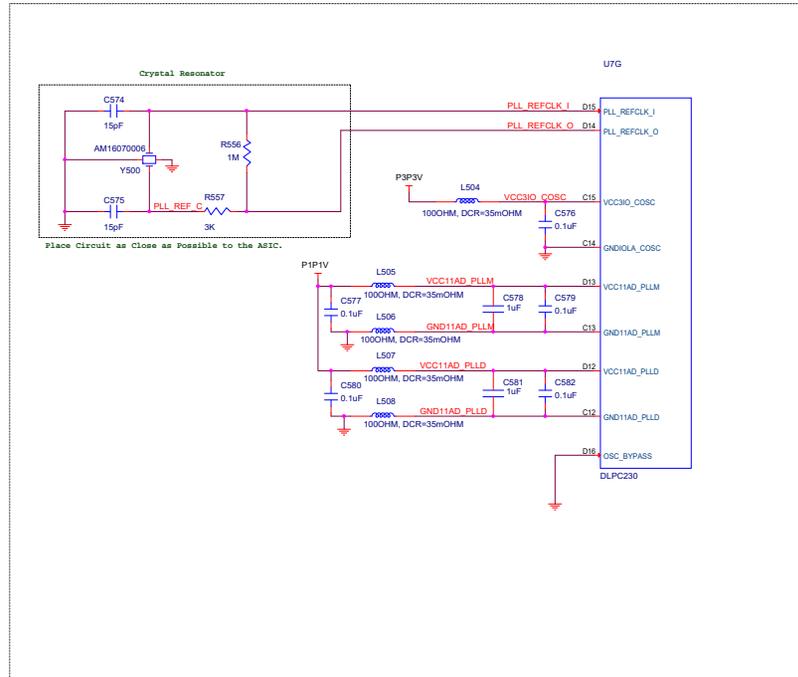
- CONFIGURATION OPTIONS
- TSTPT0 (STAY-IN-BOOT): 0= load main app, 1= stay in boot app
 - TSTPT1 (EXT-BOOT-EN): 0= internal boot (must be low)
 - TSTPT2 (I2C-ADDR-SEL): 0=0x36, 1=0x34
 - TSTPT3 (ALT-MADR-SEL): 0= load main app 1, 1= load main app 2
 - TSTPT4 (BOOT-SPI-MASTER-EN): 0= disabled (must be low)
 - TSTPT5 (Spread Spectrum Enable): 0= disabled, 1= enabled
 - TSTPT6 (Crystal Frequency): 0= reserved, 1= 16MHz (must be high)
 - CHKSUM_SEL: 0= 8 bit CRC, 1= 8 bit checksum
 - HOST_IF_SEL: 0= Host SPI, 1= Host I2C
 - HOST_SPI_MODE: 0= mode 0 or 3, 1= mode 1 or 2



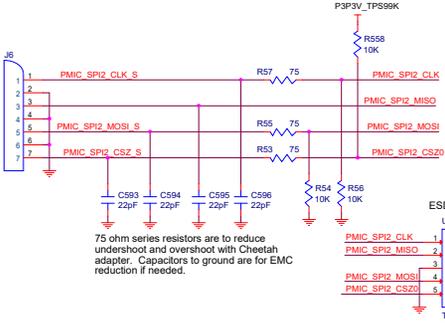
DLPC230 POWER



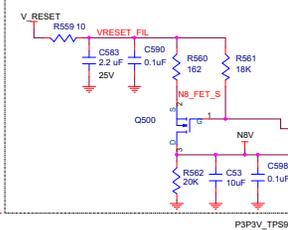
DLPC230 REFERENCE CLOCK INTERFACE



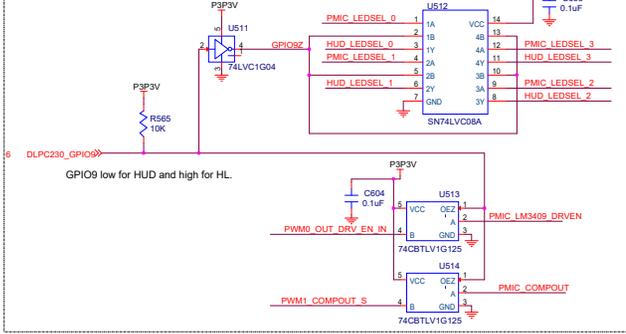
TPS99000 SPI DEBUG CONNECTOR



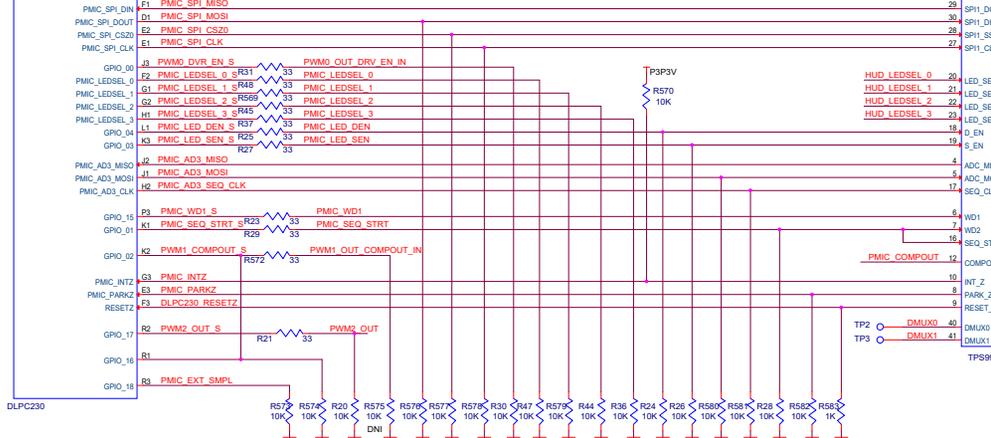
If photodiodes are not needed then negative 8V (NBV) circuit can be removed as long as negative 8V regulator is not enabled in software configuration. TPS99000 pins VIN_LDOT_M8 and VLDOT_M8 can be left unconnected.



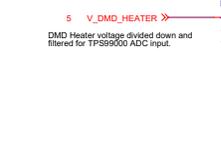
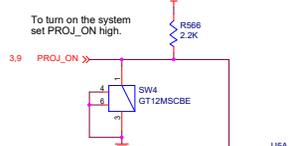
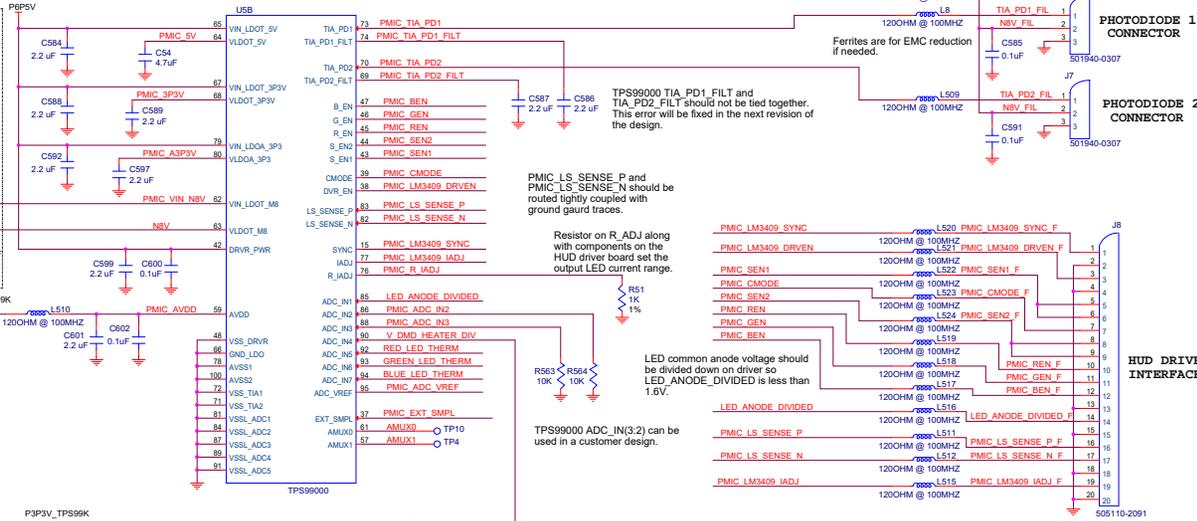
Circuitry in this box is to configure I/O for HL versus HUD operation. It is not needed for "HUD only" or "HL only" designs.



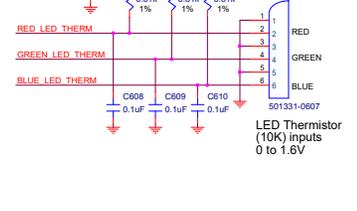
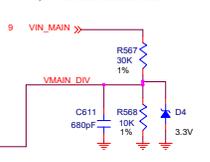
TPS99000 DLPC230 INTERFACE



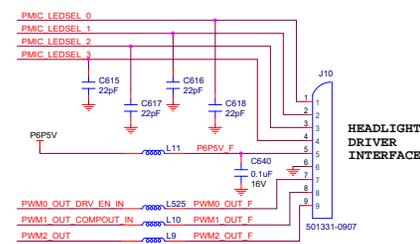
TPS99000 ANALOG INTERFACE



VMAIN shutdown threshold set to 5V (VMAIN_DIV = 1.25 when VBATT = 5V). 5.1us time constant filter.



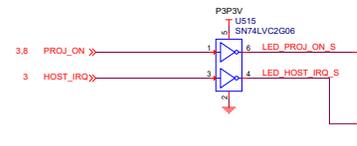
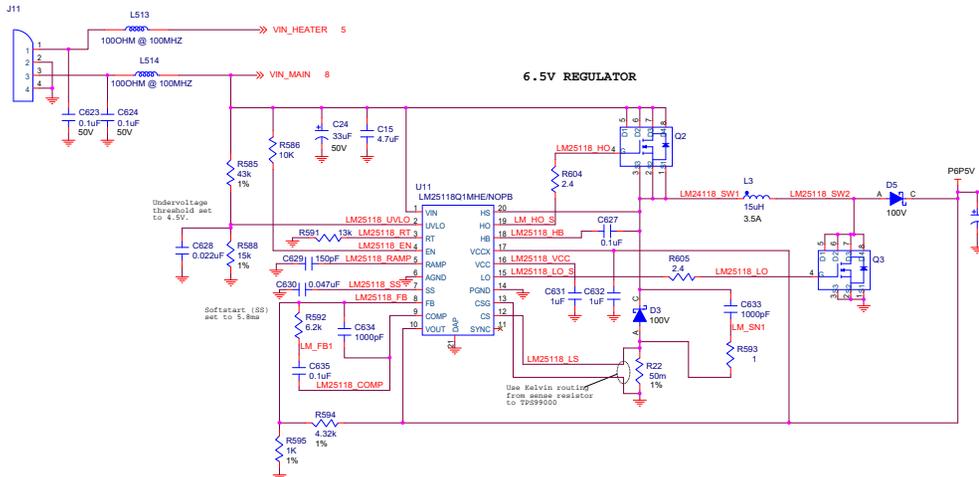
HEADLIGHT DRIVER INTERFACE



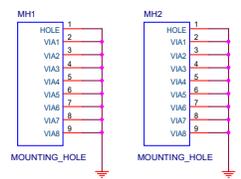
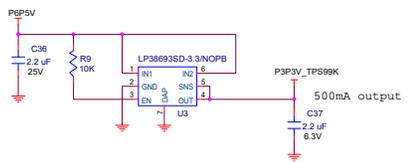
TPS99000 Interface

TEXAS INSTRUMENTS	REV: George Pavloussi 4/18/2017	DRWING NO: 2515618	REV: C
ISSUE DATE: -Issue Date-	SCALE:	SHEET 8 OF 9	

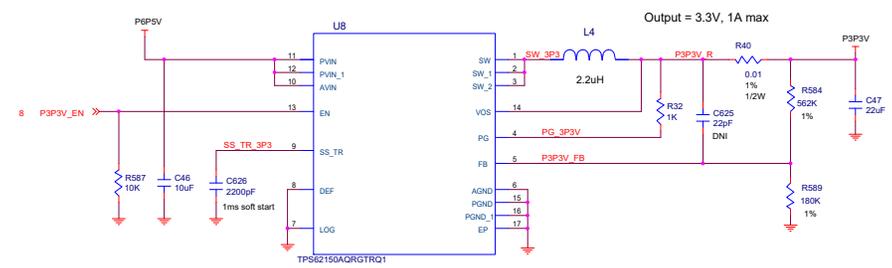
INPUT VOLTAGE FROM DRIVER



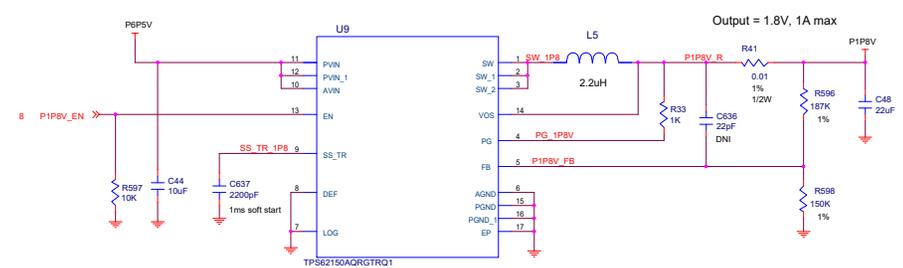
TPS99000 ANALOG 3.3V REGULATOR



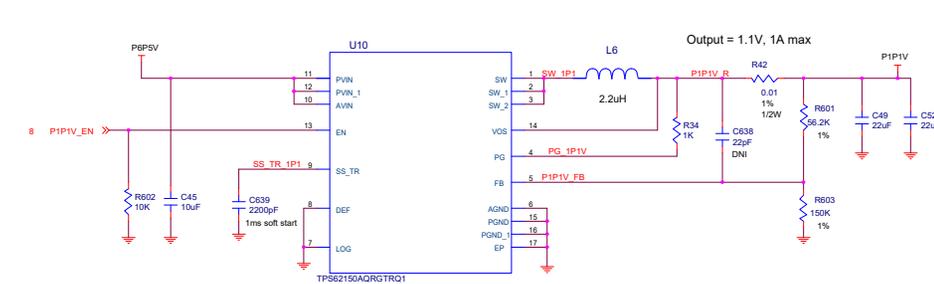
SYSTEM 3.3V REGULATOR



SYSTEM 1.8V REGULATOR



SYSTEM 1.1V REGULATOR



SYSTEM POWER