

NOTES, UNLESS OTHERWISE SPECIFIED:

- 1. The netname "P3P3V" represents connection to the +3.3V digital power plane.
- 2. The netname "P1P8V" represents connection to the +1.8V digital power plane.
- 3. The netname "P1P1V" represents connection to the +1.1V digital power plane.
- 4. The symbol ⚡ represents connection to the digital ground plane.
- 5. A "Z" suffix on a signal name indicates an active low signal.
- 6. A "_S" suffix on a signal name indicates a trace that is between a driver and a series termination resistor.
- 7. All components with designators "U", "D", "Y" and "Q" are electrostatic discharge sensitive.
- 8. The letters DNI near a part mean "do not install".

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REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
A	Initial Release		GP
B	Corrected wiring from DVI receiver to DLPC230. Changed DLPC230 pulldown on JTAGRSTZ to 1K. Changed C615-C618 to 22pF. Changed U511 to LCV1G04.		GP
C	Fixed TPS99000 connections for TIA_PD1_FILTER and TIA_PD2_FILTER. Added C642 to TPS99000 inductor/LS net. Connected PWM1_COMPOUT_S to DLPC230 GPIO16. Changed R575 to DNI. Changed connector, diode and transistor part number attribute to non-visible. Added PCB part.	3/22/2018	GP

Z_PCB1
PCB_DLP553X Formatter
DLP005
2515619



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		ENGR			
		SYST			
		PRJ			
				TITLE DLP553x EVM Formatter - DLP005	
2515620					
NEXT ASSY	USED ON				
APPLICATION		SW	Cadence Capture 16.6	D	DRAWING NO 2515618
				SCALE	SHEET 1 of 9
					REV C

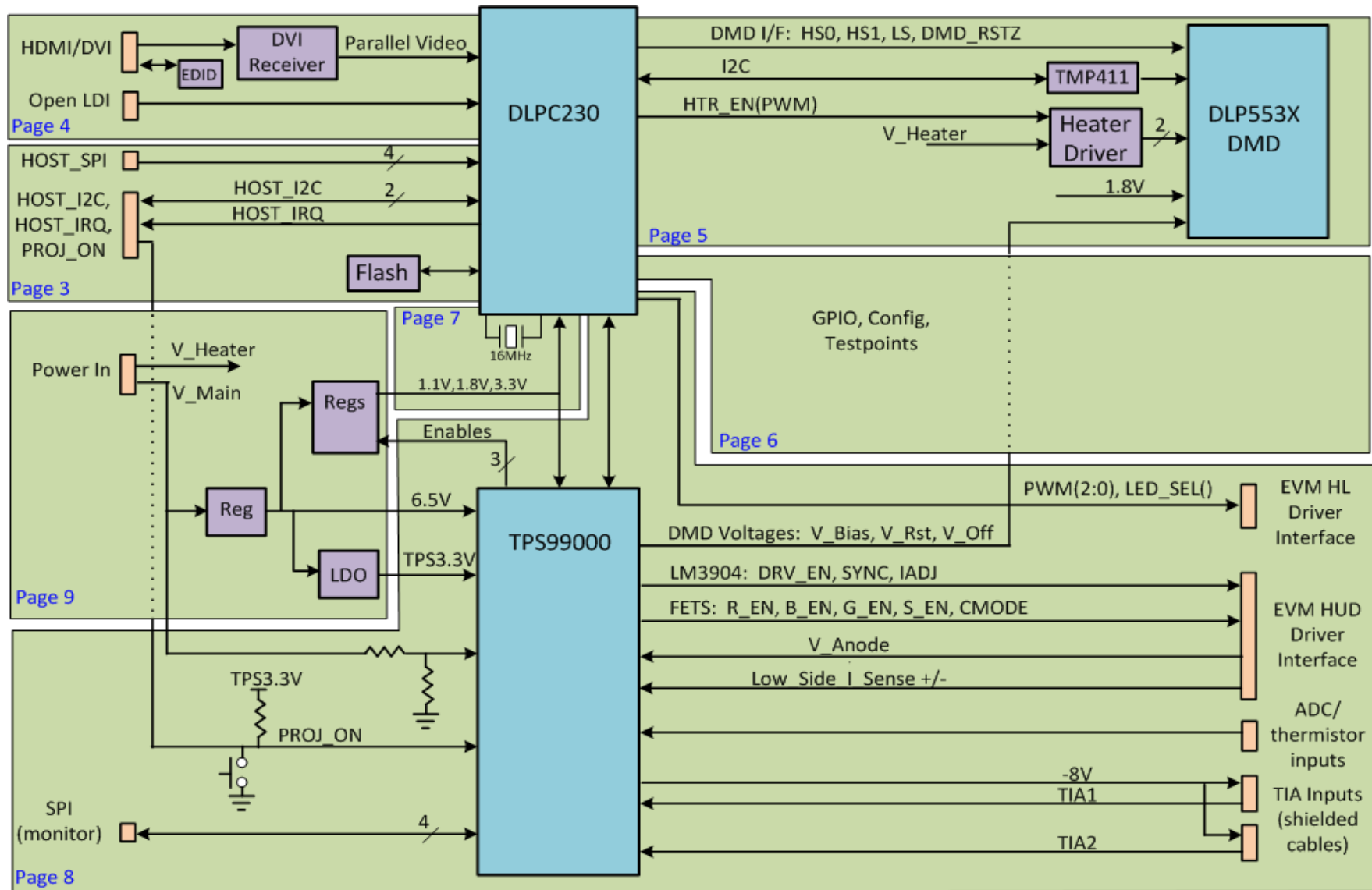


Diagram showing pin connections for U13 and U500:

- U13:**
 - IO1: HOST I2C SDA
 - IO2: HOST I2C SCL
 - GND: Ground
- U500:**
 - D1: HOST IRQ
 - D2: PROJ ON
 - D3: HOLD BOOTZ
 - D4: Ground
 - D10: Ground
 - D9: Ground
 - D8: Ground
 - D7: Ground
 - D6: Ground

HOST SPI CONNECTOR

The diagram illustrates the electrical connections for the HOST SPI interface. A 7-pin connector (J2) is shown on the left, with pins numbered 1 through 7. The connections are as follows:

- Pin 1:** HOST SPI CLK_S. This line is connected to a 75 ohm resistor (R501) and then to the P3P3V supply.
- Pin 2:** GND.
- Pin 3:** GND.
- Pin 4:** GND.
- Pin 5:** HOST SPI MOSI_S. This line is connected to a 75 ohm resistor (R502) and then to the P3P3V supply.
- Pin 6:** GND.
- Pin 7:** HOST SPI CSZ_S. This line is connected to a 75 ohm resistor (R503) and then to the P3P3V supply.

Additional components shown include:

- Four 22pF capacitors (C505, C506, C507, C508) connected to ground.
- Two 10K resistors (R504, R505) connected to the P3P3V supply.

75 ohm series resistors are to reduce undershoot and overshoot with Cheetah adapter. Capacitors to ground are for EMC reduction if needed.

U501

HOST SPI CLK S 1 D1 10

HOST SPI MOSI 2 D2 9

HOST SPI MISO S 3 GND1 GND2 8

HOST SPI CSZ S 4 D3 7

5 D4 6

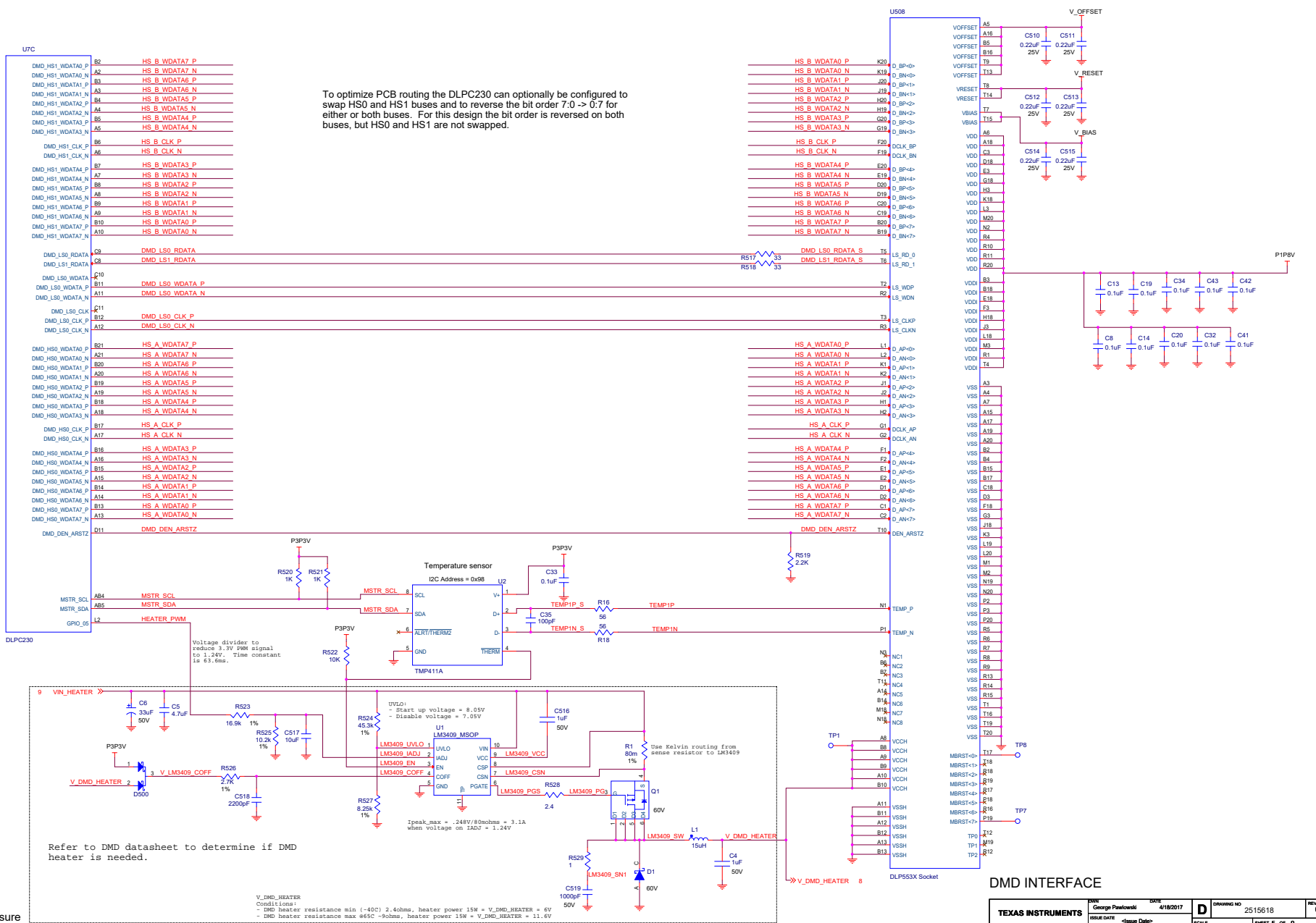
TPD4F05106

[illegible]

The Host IRQ signal is asserted to let the host know when an emergency shutdown has occurred within the DLPC230

DQ2 and DQ3 have smaller pullup resistors to ensure they are high after a quad operation before a new command starts. This is only necessary for parts with HOLDZ and WZ functionality.

The diagram shows the internal circuitry of the MX25L12839F QSPI flash memory. The chip is connected to a P3P3V supply and ground. Pullup resistors are connected to P3P3V: R508 (10K) to DQ2, R507 (10K) to DQ3, R506 (10K) to DQ4, R49 (10K) to DQ5, R505 (3.3K) to DQ6, and R35 (3.3K) to DQ7. A 0.1uF capacitor (C51) is connected between VCC and ground. The chip's pins are: A2 (NC/A2), A3 (NC/A3), A5 (NC/A5), B1 (NC/B1), NCB1 (NCB1), NCB5 (NCB5), C1 (NC/C1), C3 (NC/C3), NC03 (NC03), C5 (NC/C5), D1 (NC/D1), D3 (NC/D3), D5 (NC/D5), E1 (NC/E1), E3 (NC/E3), E5 (NC/E5), F1 (NC/F1), F3 (NC/F3), F5 (NC/F5), G1 (NC/G1), G3 (NC/G3), G5 (NC/G5), H1 (NC/H1), H3 (NC/H3), H5 (NC/H5), I1 (NC/I1), I3 (NC/I3), I5 (NC/I5), J1 (NC/J1), J3 (NC/J3), J5 (NC/J5), K1 (NC/K1), K3 (NC/K3), K5 (NC/K5), L1 (NC/L1), L3 (NC/L3), L5 (NC/L5), M1 (NC/M1), M3 (NC/M3), M5 (NC/M5), N1 (NC/N1), N3 (NC/N3), N5 (NC/N5), O1 (NC/O1), O3 (NC/O3), O5 (NC/O5), P1 (NC/P1), P3 (NC/P3), P5 (NC/P5), Q1 (NC/Q1), Q3 (NC/Q3), Q5 (NC/Q5), R1 (NC/R1), R3 (NC/R3), R5 (NC/R5), S1 (NC/S1), S3 (NC/S3), S5 (NC/S5), T1 (NC/T1), T3 (NC/T3), T5 (NC/T5), U1 (NC/U1), U3 (NC/U3), U5 (NC/U5), V1 (NC/V1), V3 (NC/V3), V5 (NC/V5), W1 (NC/W1), W3 (NC/W3), W5 (NC/W5), X1 (NC/X1), X3 (NC/X3), X5 (NC/X5), Y1 (NC/Y1), Y3 (NC/Y3), Y5 (NC/Y5), Z1 (NC/Z1), Z3 (NC/Z3), Z5 (NC/Z5).

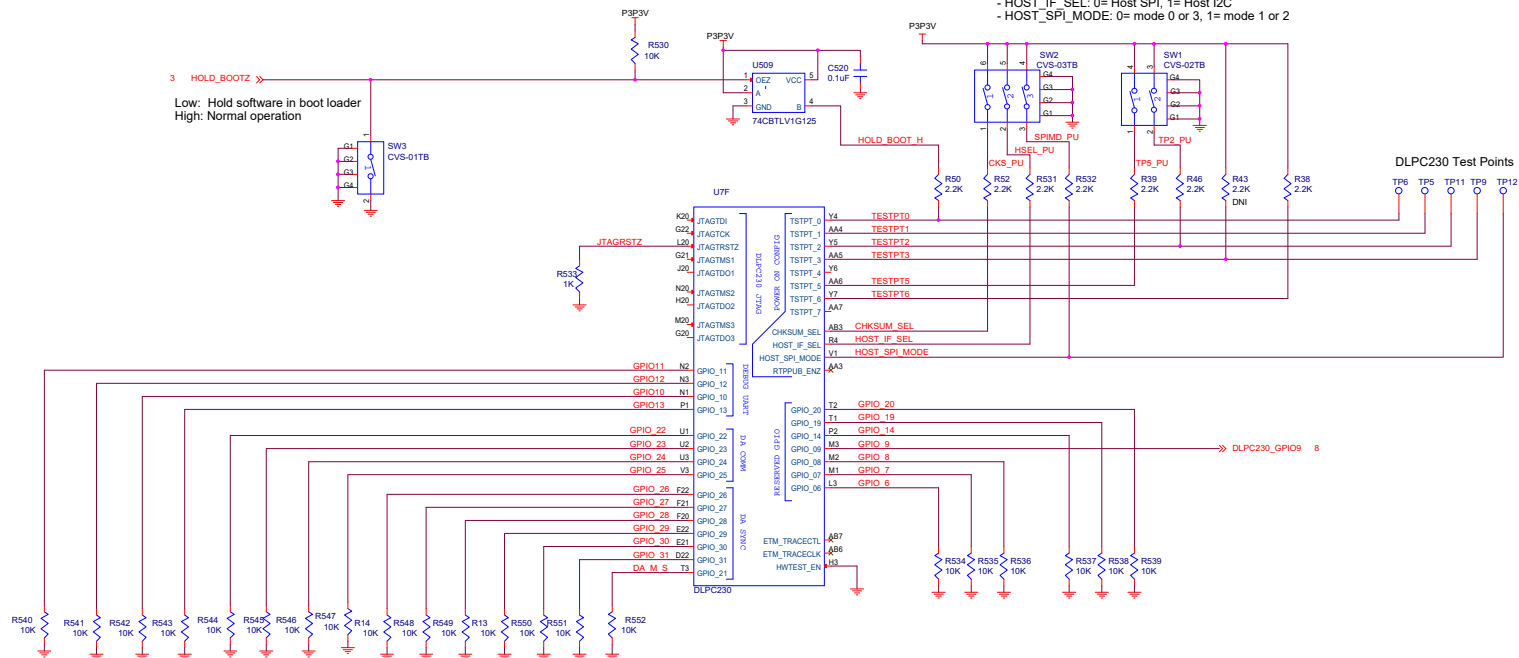


To optimize PCB routing the DLPC230 can optionally be configured to swap HS0 and HS1 buses and to reverse the bit order 7:0 -> 0:7 for either or both buses. For this design the bit order is reversed on both buses, but HS0 and HS1 are not swapped.

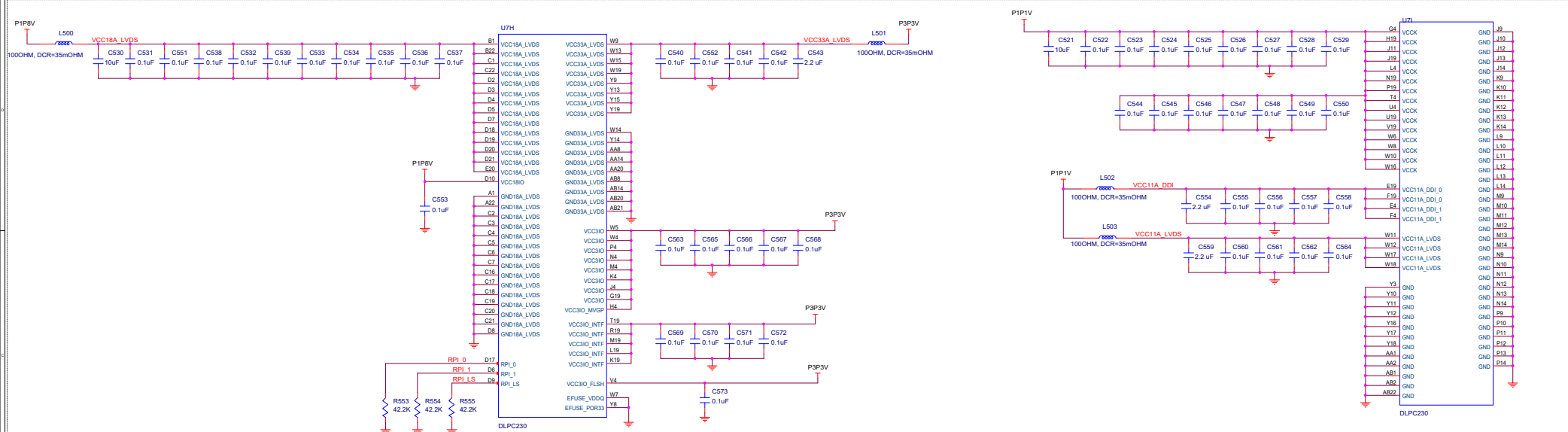
- TSTPT(7:0), CHKSUM_SEL, HOST_IF_SEL, HOST_SPI_SEL are inputs when RESETZ is low and have internal weak pulldown resistors. The states of the inputs are sampled after reset transitions from low to high to determine configuration options. Pins are then set as outputs.

CONFIGURATION OPTIONS

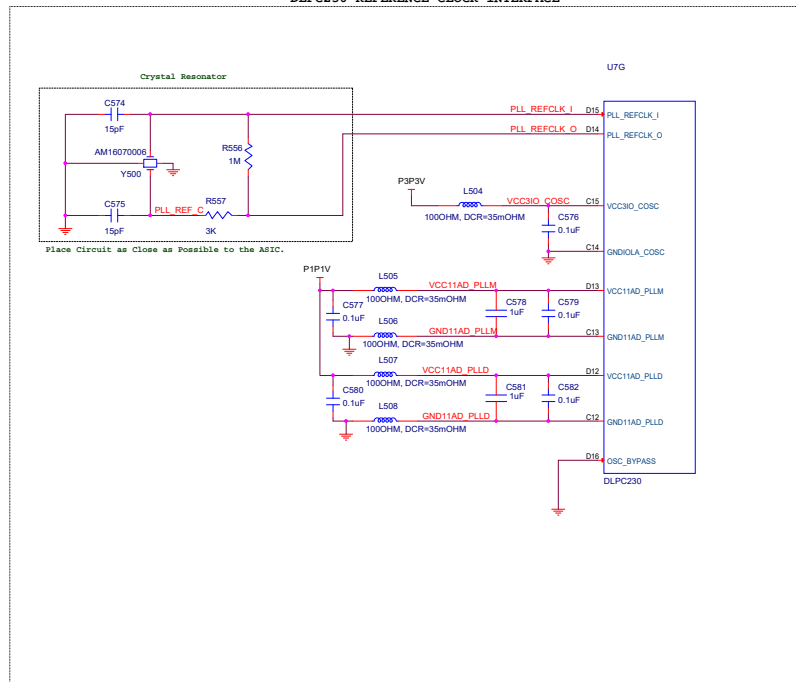
- TSTPT0 (STAY-IN-BOOT): 0= load main app, 1= stay in boot app
- TSTPT1 (EXT-BOOT-EN): 0= internal boot (must be low)
- TSTPT2 (I2C-ADDR-SEL): 0=0x36, 1=0x34
- TSTPT3 (ALT-MADR-SEL): 0= load main app 1, 1= load main app 2
- TSTPT4 (BOOT-SPI-MASTER-EN): 0= disabled (must be low)
- TSTPT5 (Spread Spectrum Enable): 0= disabled, 1= enabled
- TSTPT6 (Crystal Frequency): 0= reserved, 1= 16MHz (must be high)
- CHKSUM_SEL: 0= 8 bit CRC, 1= 8 bit checksum
- HOST_IF_SEL: 0= Host SPI, 1= Host I2C
- HOST_SPI_MODE: 0= mode 0 or 3, 1= mode 1 or 2



DLPC230 POWER



DLPC230 REFERENCE CLOCK INTERFACE



Undervoltage threshold set to 4.5V

Softstart (SS) set to 5.8ms

Use Kelvin routine for sense resistor to TP9P9000

[illegible]

Output = 1.8V, 1A max

The schematic diagram illustrates the P3P2V_TPS99K circuit. It features a P3P2V_TPS99K LED driver IC, which is an LP38893SD-3.3/NOPB. The circuit includes a 2.2 uF capacitor (C36) connected to the P3P2V input, a 10K resistor (R9) connected to the IN1 pin, and a 2.2 uF capacitor (C37) connected to the output. The output is labeled '500mA output'. The IC is an LP38893SD-3.3/NOPB. The diagram also shows two mounting hole patterns, MH1 and MH2, with dimensions in inches and millimeters.

[illegible]