

AM263x CC AUTO  
PROC153E1

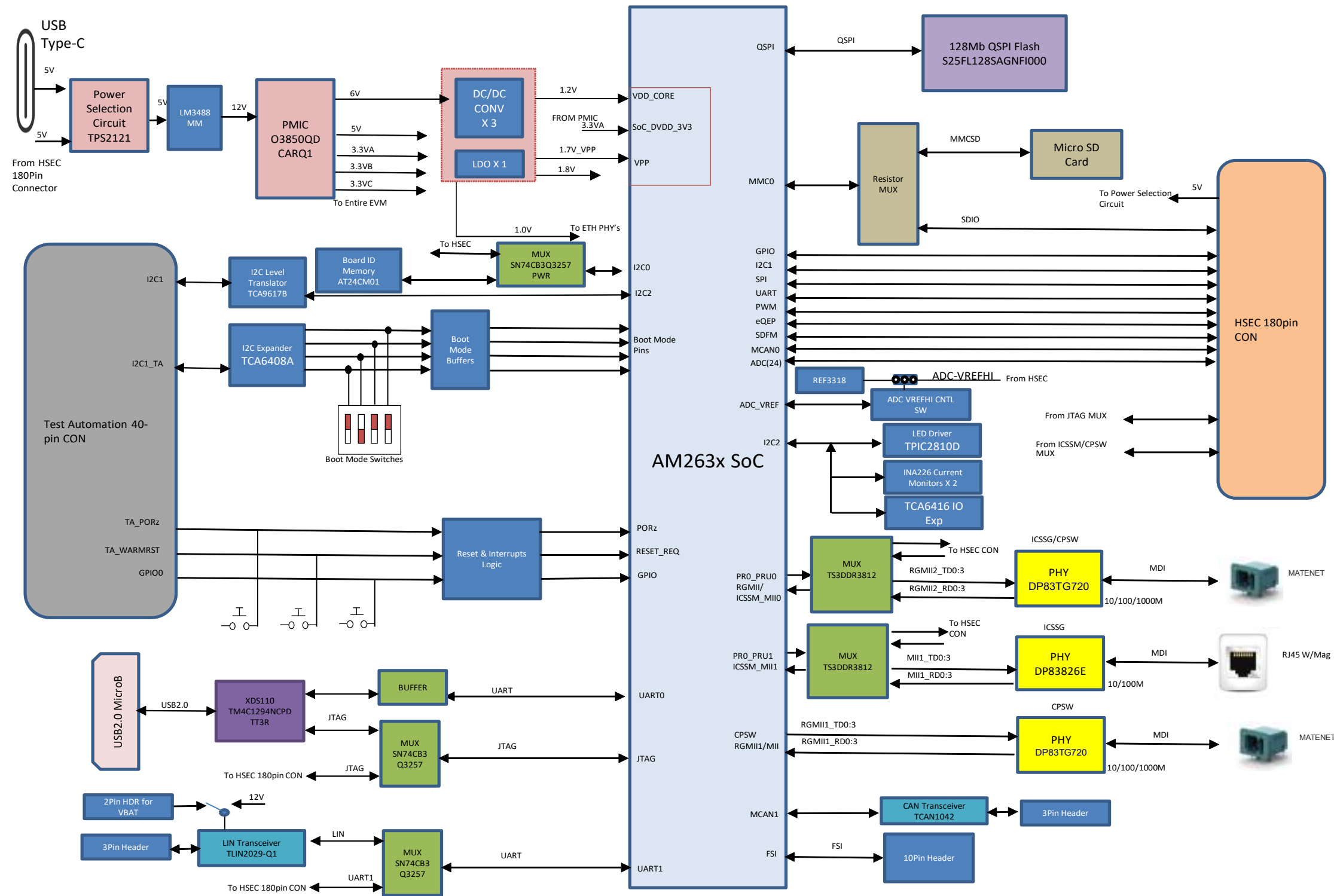
TABLE OF CONTENTS

PAGE	CONTENTS
01	TABLE OF CONTENTS
02	REVISION HISTORY
03	SYSTEM BLOCK DIAGRAM
04	POWER FLOW DIAGRAM
05	POWER SEQUENCING
06	I2C TREE
07	SOC GPIO_MAPPING_TABLE
08	SOC-QSPI INTERFACE
09	SOC-MMC0 INTERFACE
10	SOC-IO INTERFACES
11	SOC-JTAG, RESET and CLK
12	SOC-CPSW RGMII1/MII1 Ethernet
13	SOC-PRU0 ICSSM RGMII/MII, CPSW RGMII2/MII2 Ethernet
14	SOC-PRU1 ICSSM RGMII/MII Ethernet
15	SOC-ADC INTERFACE
16	SOC-POWER and GND
17	RESET SWITCHES
18	CLOCKS AND CURRENT MONS
19	XDS110 DEBUGGER
20	TEST AUTOMATION HEADER
21	BOOTMODE BUFFER AND SWITCH
22	LED DRIVER
23	POWER INPUT
24	PMIC
25	POWER SUPPLY #1
26	ETHERNET POWERS
27	HSEC CONNECTOR
28	CC EVM NOTES, HW and LABELS

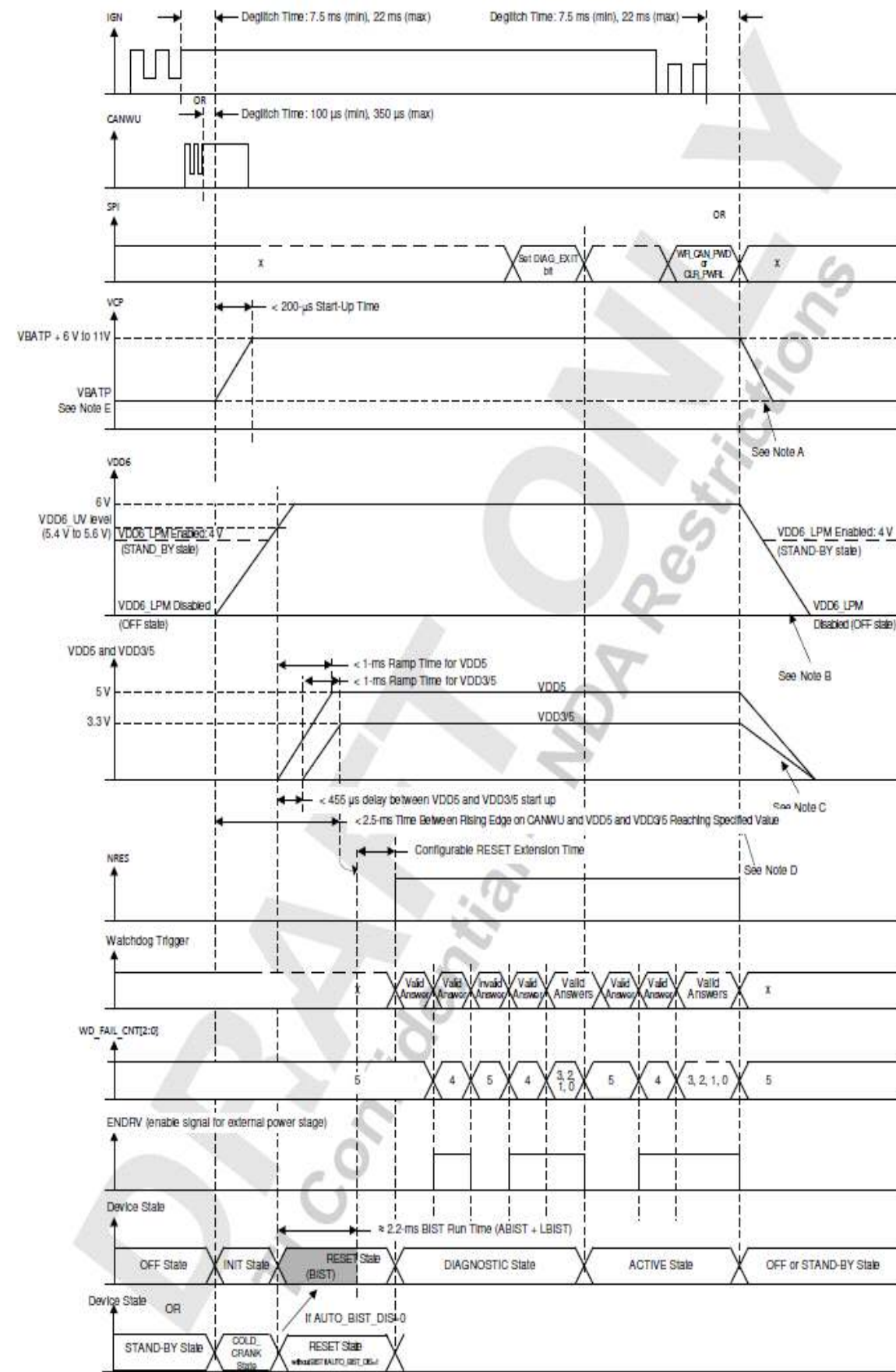
REVISION HISTORY

REV #	DATE	DESCRIPTION OF CHANGES	AUTHOR	REVIEWED BY	APPROVED BY
E1	04 APR 2022	Drafted from E2	Mistral Design Team		
	09 MAY 2022	Updated TI comments about power section	Mistral Design Team		
	22 JUL 2022	Updated TI comments about power section	Mistral Design Team		
	03 AUG 2022	Updated U66 Part to TPS75801	Mistral Design Team		
	14 OCT 2022	Updated RESET section as per TI comments	Mistral Design Team		
	18 NOV 2022	Updated TI comments	Mistral Design Team		
	05 DEC 2022	Updated TI comments and Changed SOC refdes to U1	Mistral Design Team		
	10 MAR 2023	Updated Block diagram	Mistral Design Team		

## SYSTEM BLOCK DIAGRAM



POWER SEQUENCE



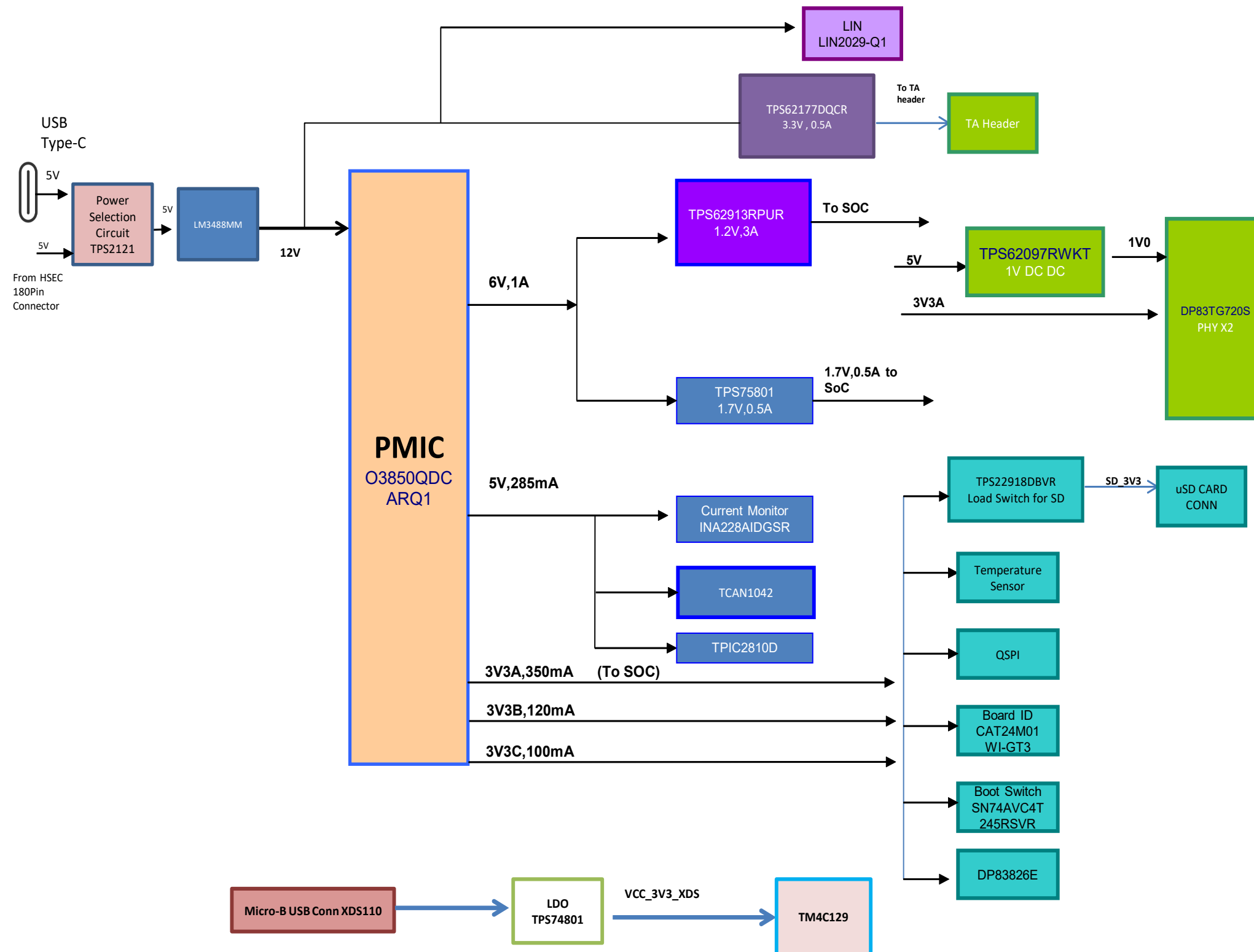
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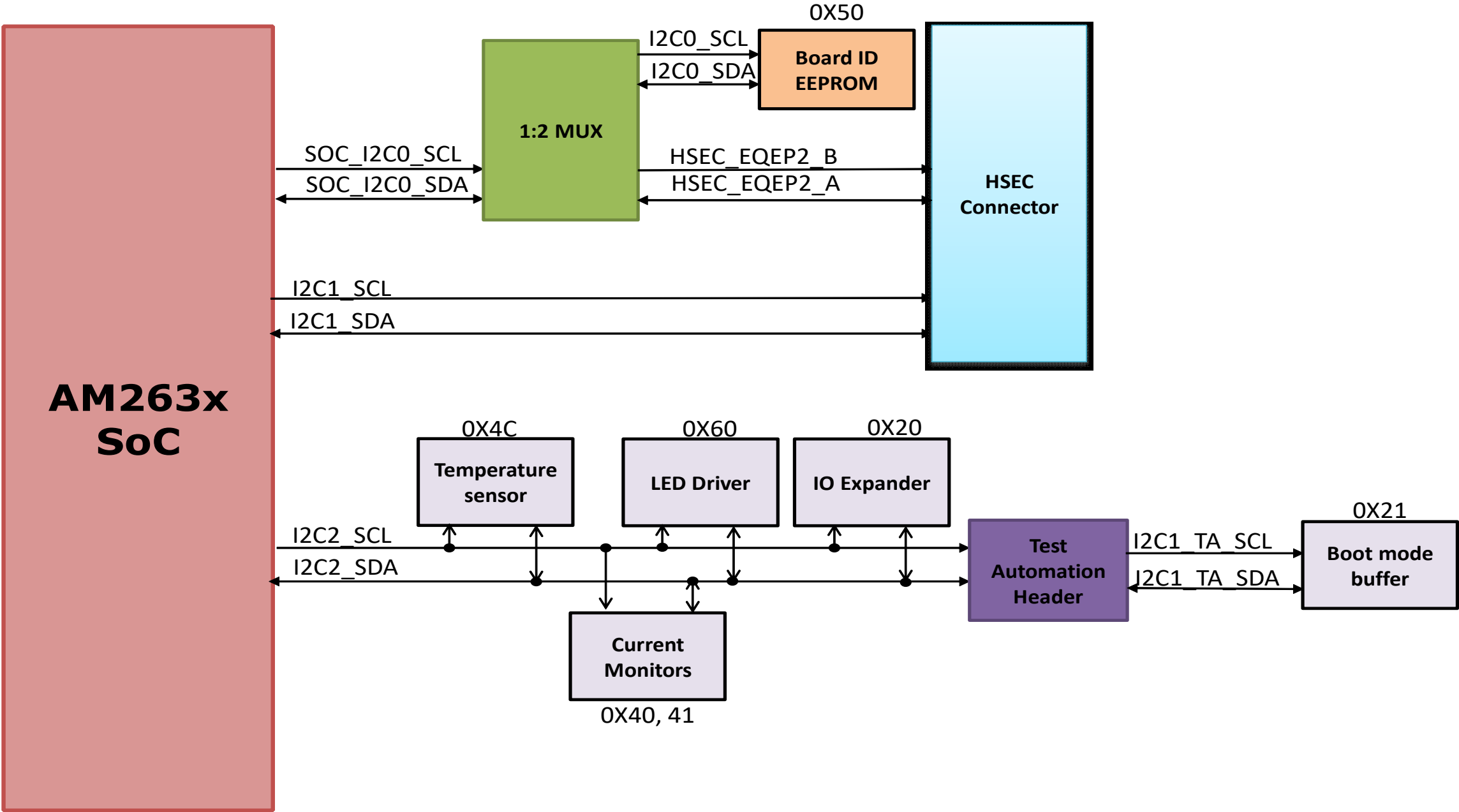
REVISION HISTORY

Size	Variant Name = PROC153 001	Rev
C		E1
Date:	Monday, December 05, 2022	Sheet 4 of 28

## POWER FLOW DIAGRAM



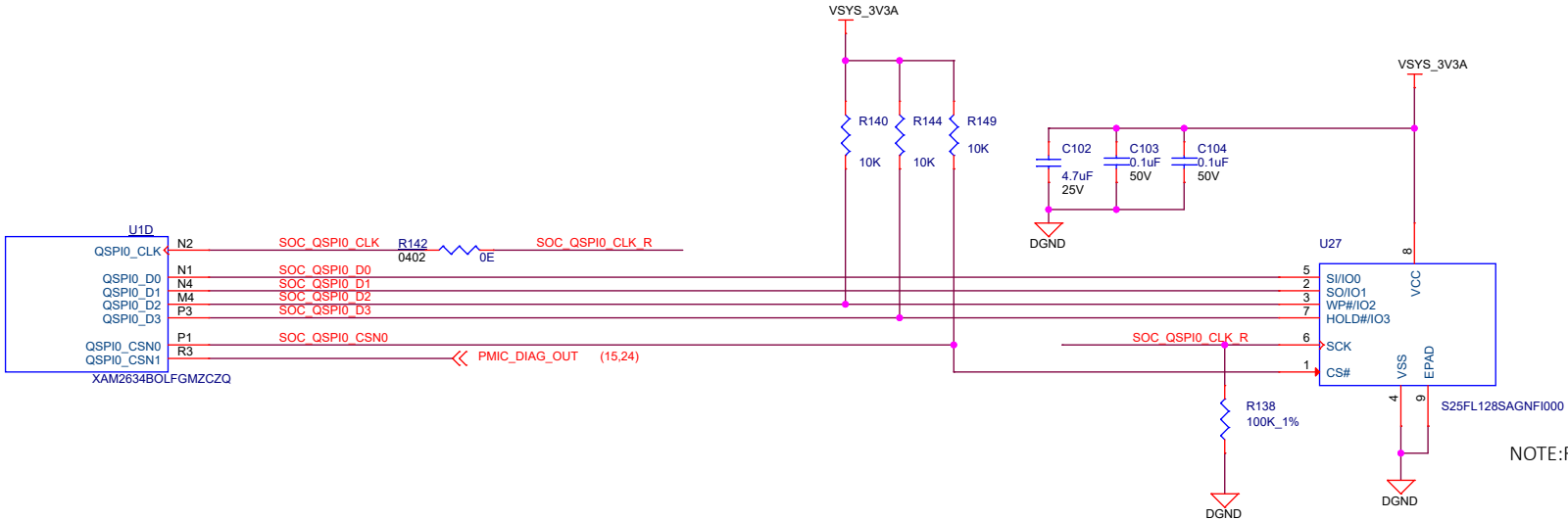
I2C TREE DIAGRAM



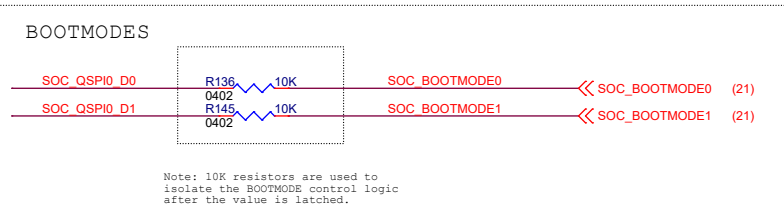
GPIO MAPPING TABLE

SI No.	GPIO DESCRIPTION	GPIO	Pin Name	FUNCTIONALITY	Net Name	ACTIVE STATE
1	Interupt To SoC	GPIO21	LIN2_RXD	Interrupt	SOC_INTn	LOW
2	Interupt To DP83826E	GPIO66	EPWM12_A	Interrupt	ICSSM2_PWDN/INTn	LOW
3	Interupt To DP83869_01	GPIO67	EPWM11_B	Interrupt	RGMII1_INT	LOW
4	Interupt To DP83869_02	GPIO68	EPWM12_B	Interrupt	ICSSM1_INT	LOW
5	User Defined LED	GPIO20	LIN2_TXD	GPIO	USER_LED0	PREFERABLE
6	PMIC DIAG OUT to SOC	GPIO1	QSPI0_CSn1	GPIO	PMIC_DIAG_OUT	LOW
IO Expander 01						
7	Standby input to CAN tranciever		P00	GPIO	MCAN1_STB	High
8	Enable control to clock buffer		P01	Enable	CLK_BUF_EN	High
9	Select line for ICSSM Mux 1		P02	Mux Selection	ICSSM1_MUX_SEL	PREFERABLE
10	Select line for ICSSM Mux 2		P03	Mux Selection	ICSSM2_MUX_SEL	PREFERABLE
11	Reset input to DT_01		P04	Reset	GPIO_RGMII1_RST	LOW
12	Reset input to DP83869_02		P05	Reset	GPIO_ICSSM1_RST	LOW
13	Reset input to DP83826E		P06	Reset	GPIO_ICSSM2_RST	LOW
14	Enable control to SD load switch		P07	Load SW Enable	GPIO_uSD_PWR_EN	High
15	User Defined LED		P10	GPIO	USER_LED1	PREFERABLE
16	Select line for I2C0 MUX		P11	Mux Selection	I2C0_MUX_SEL	PREFERABLE
17	Select line for SPI1 MUX		P12	Mux Selection	SPI1_MUX_SEL	PREFERABLE
18	Enable control to 1.7V LDO		P13	LDO Enable	VPP_LDO_EN	PREFERABLE
19	Select line for MDIO/MDC MUX		P14	Mux Selection	MDIO/MDC_MUX_SEL	PREFERABLE
20	Select line for LIN/UART MUX		P15	Mux Selection	LIN_MUX_SEL	PREFERABLE
21	Select line for ADC MUX		P16	Mux Selection	ADC1_MUX_SEL	PREFERABLE
22	Select line for ADC MUX		P17	Mux Selection	ADC2_MUX_SEL	PREFERABLE

# SOC- QSPI Interface

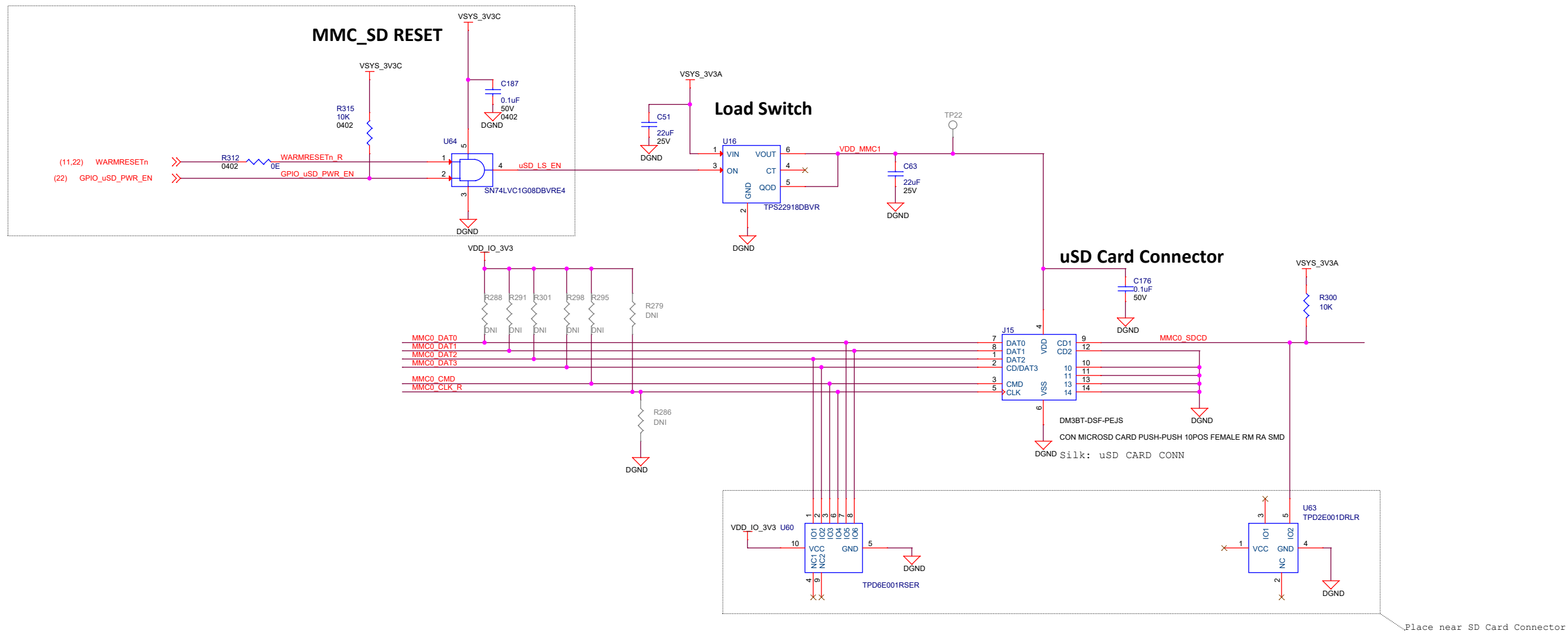
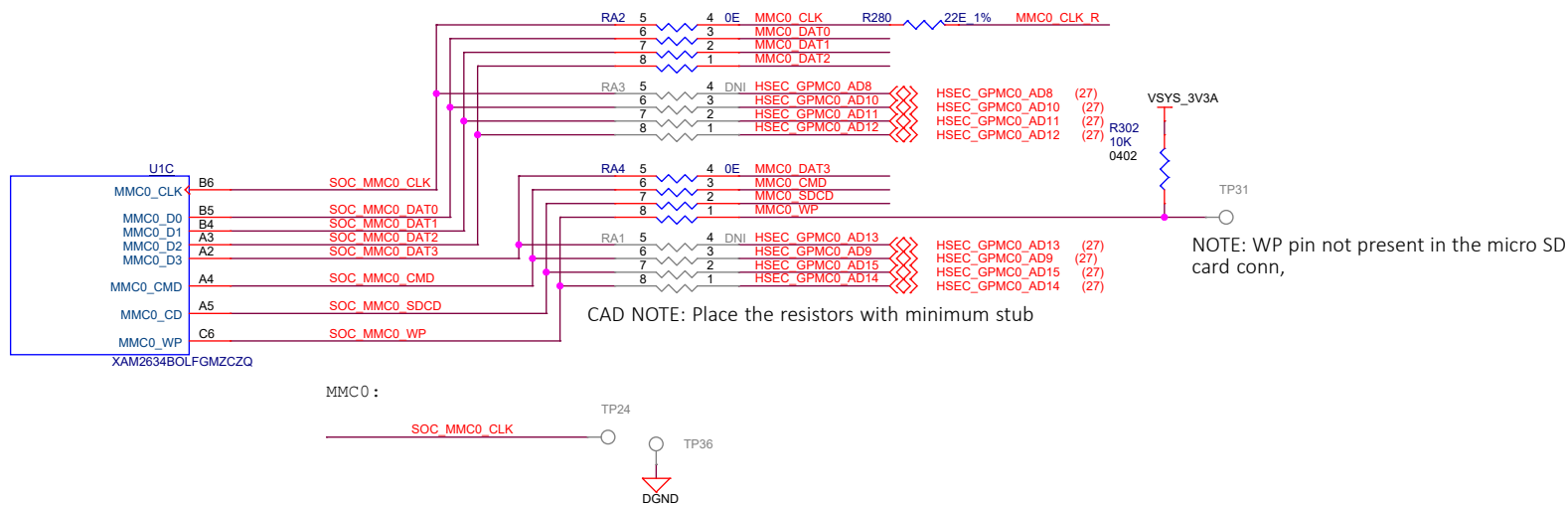


NOTE:RST pin is not present in WSON





# SOC- MMC0 Interface



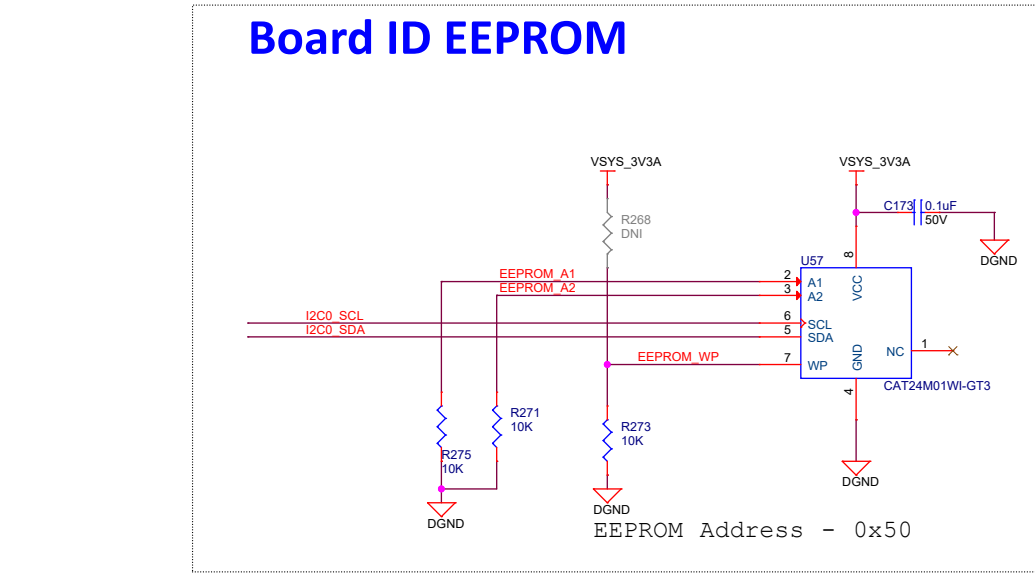
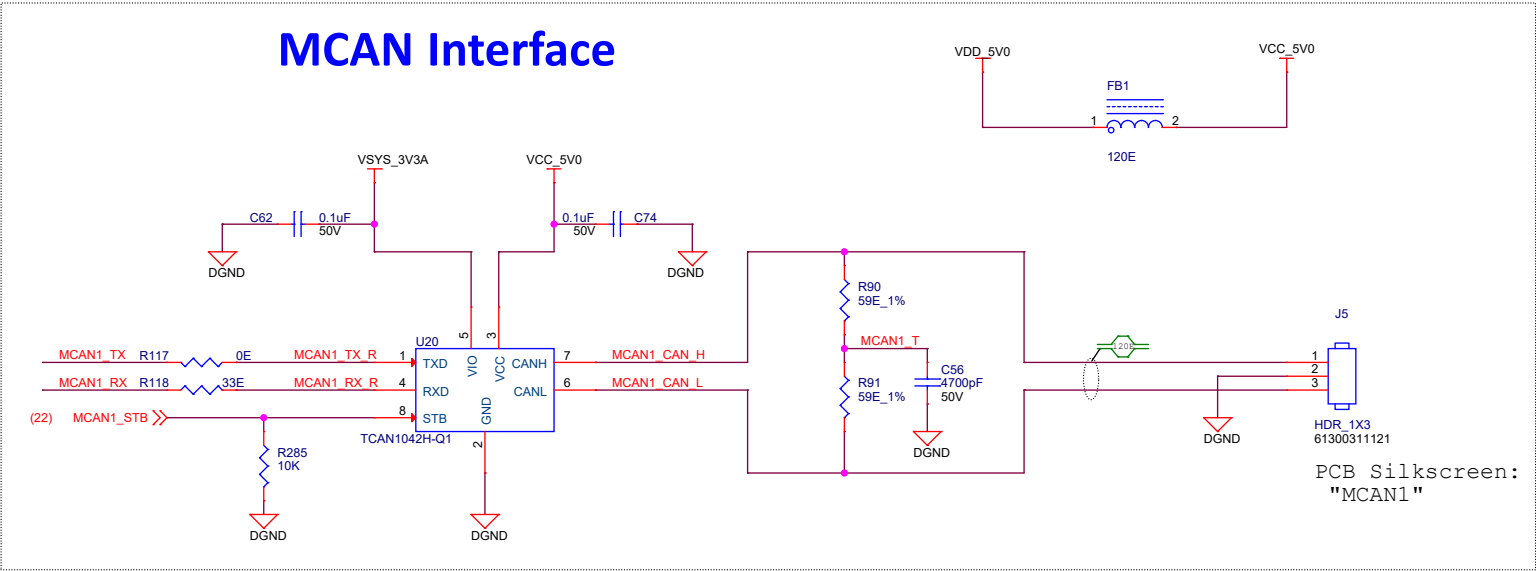
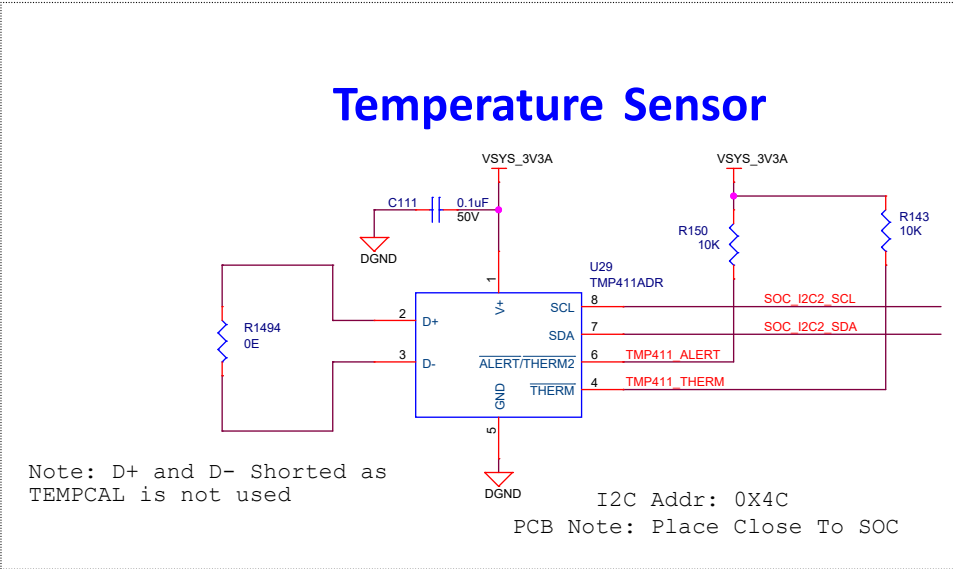
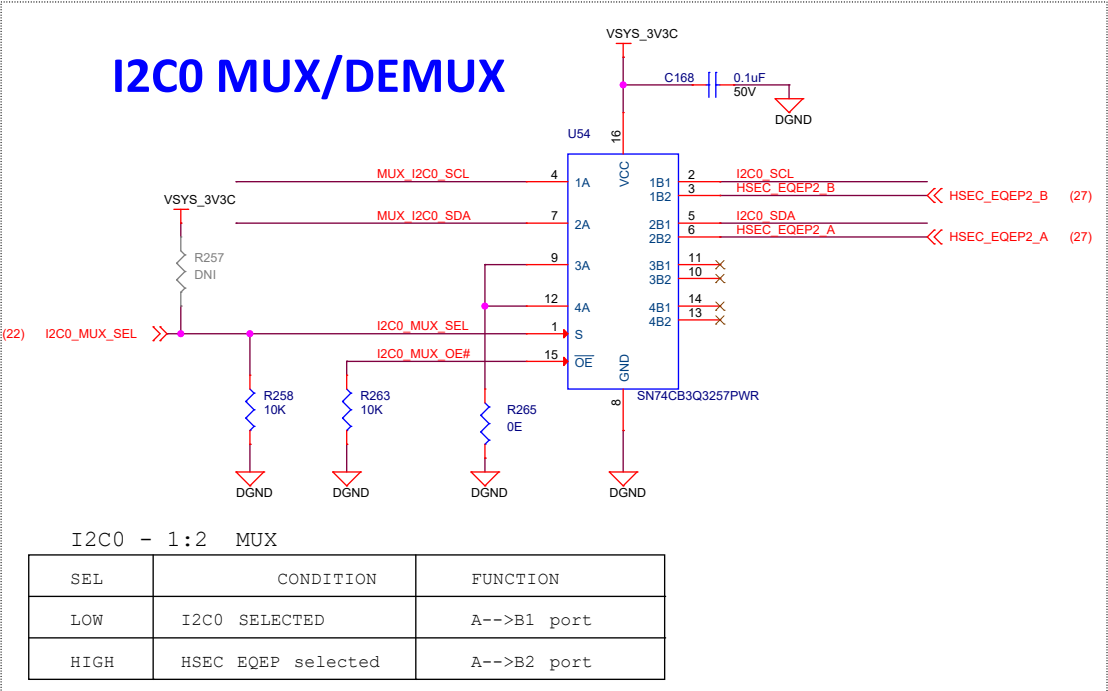
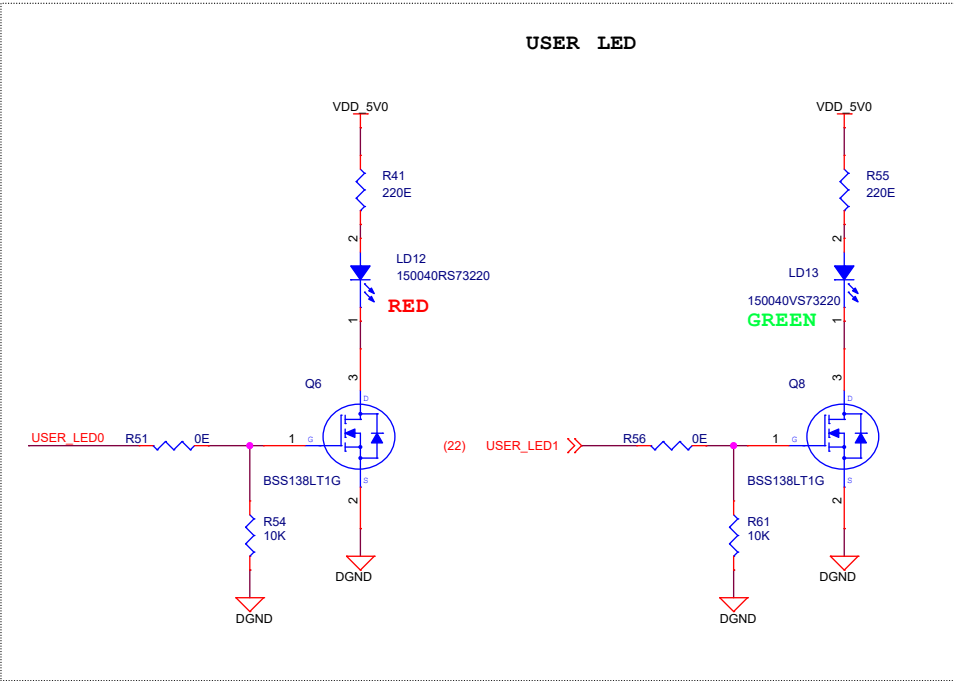
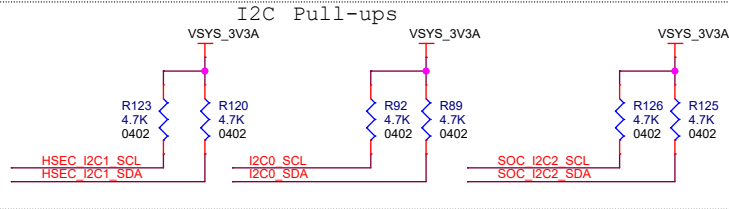
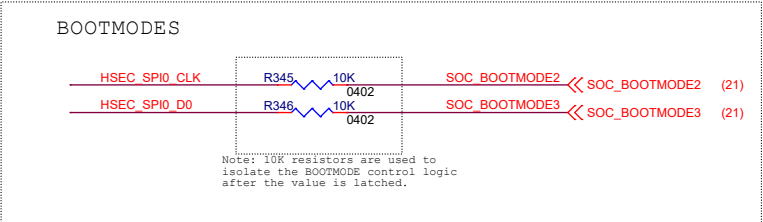
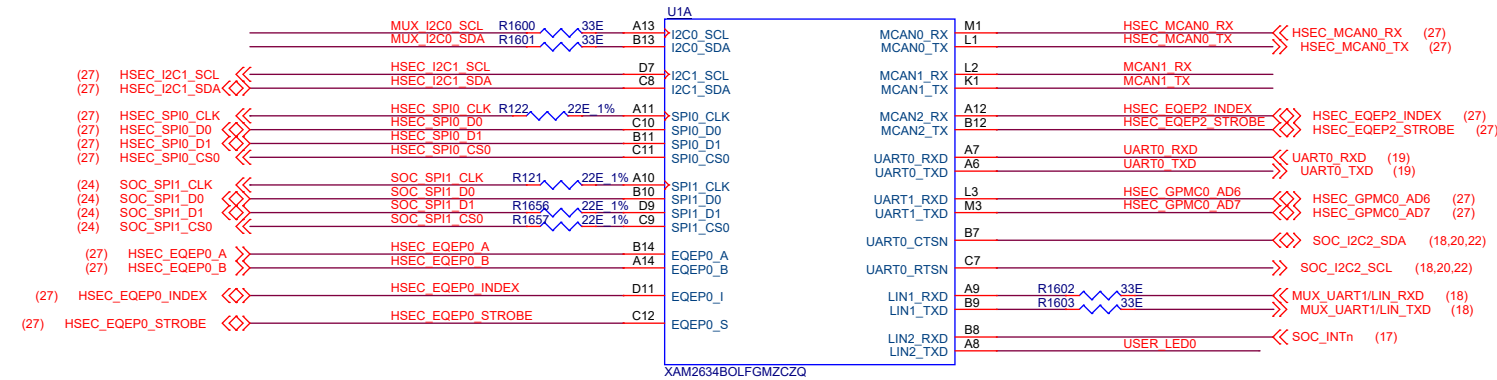
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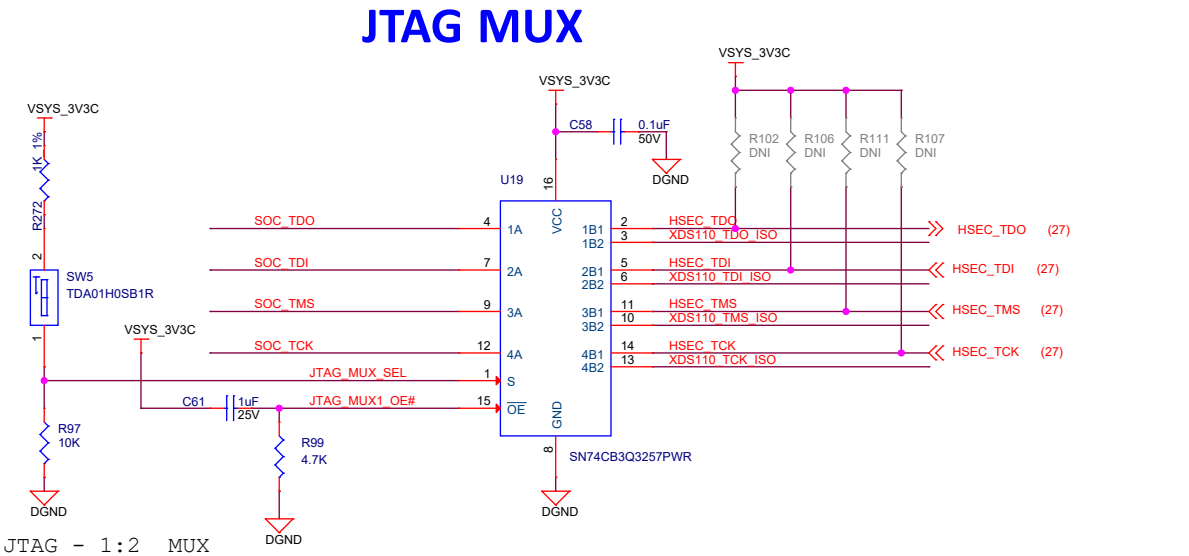
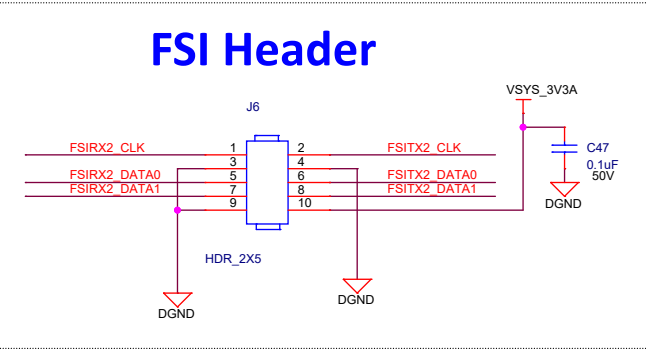
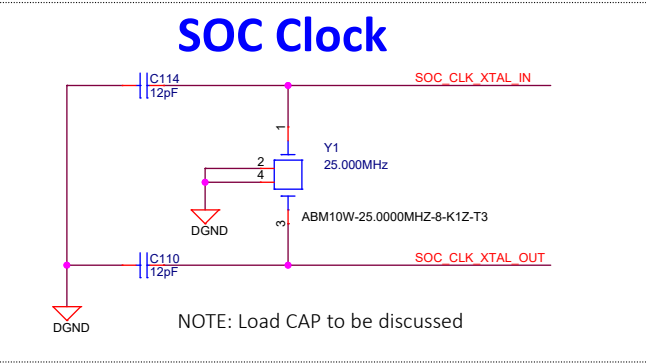
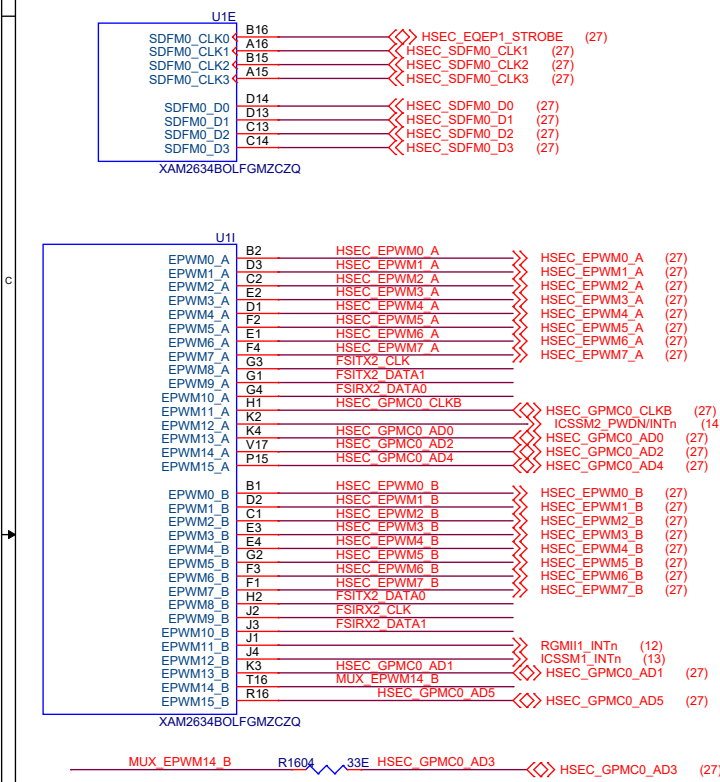
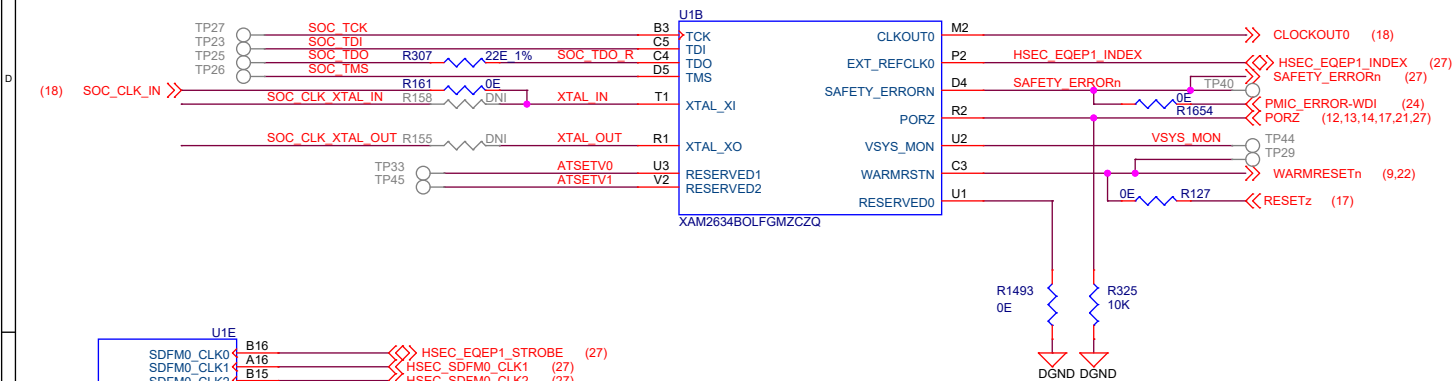
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Size	Rev
C	E1
Variant Name = PROC153 001	
Date: Monday, December 05, 2022	Sheet 9 of 28

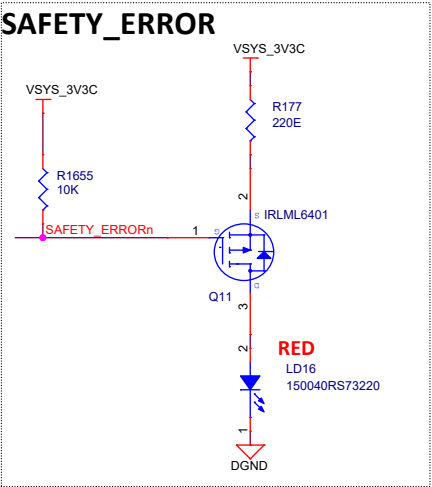
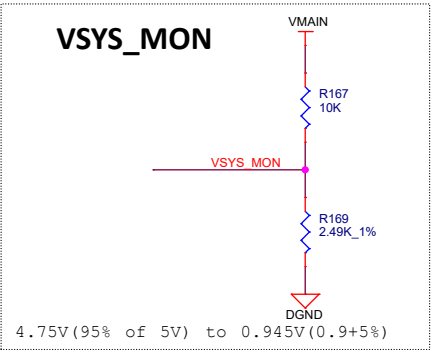
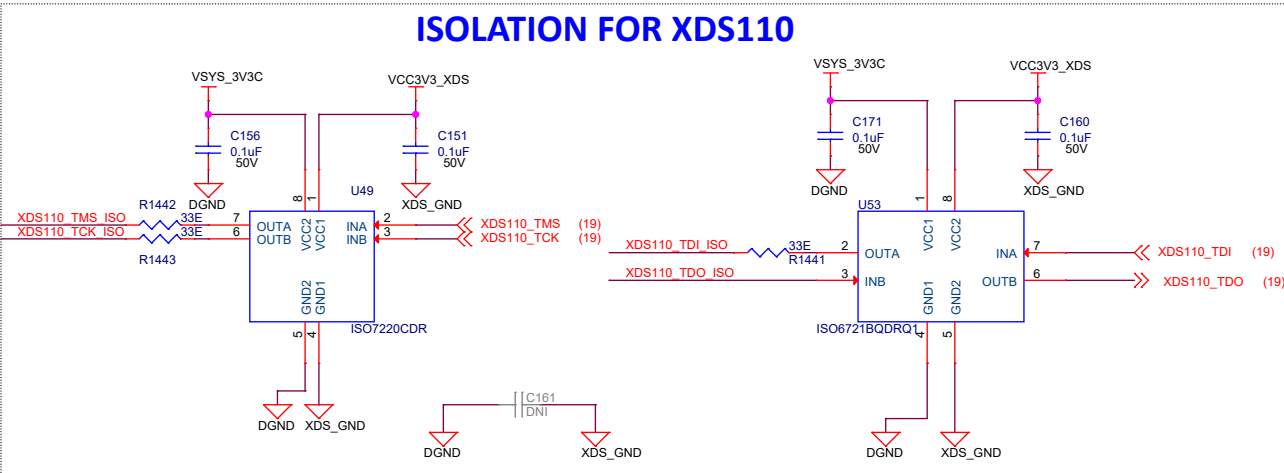
SOC-IO Interfaces



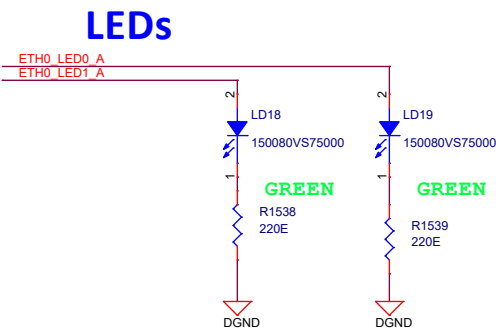
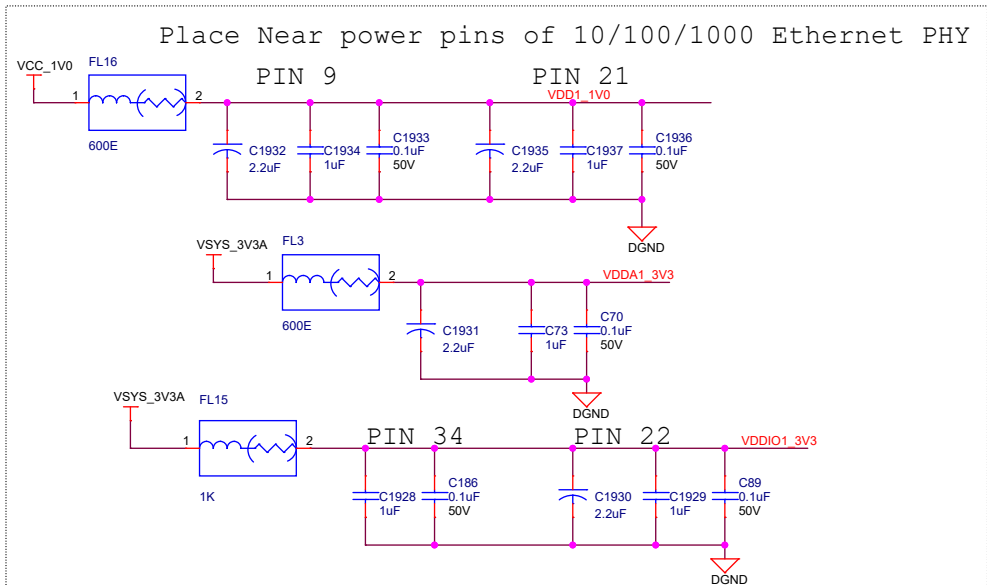
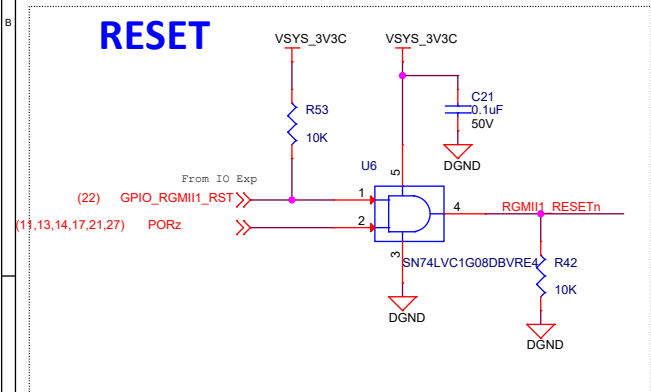
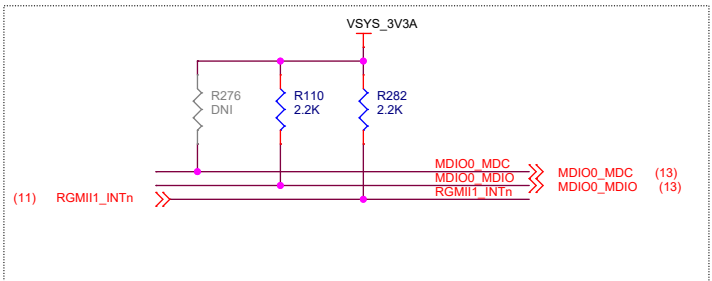
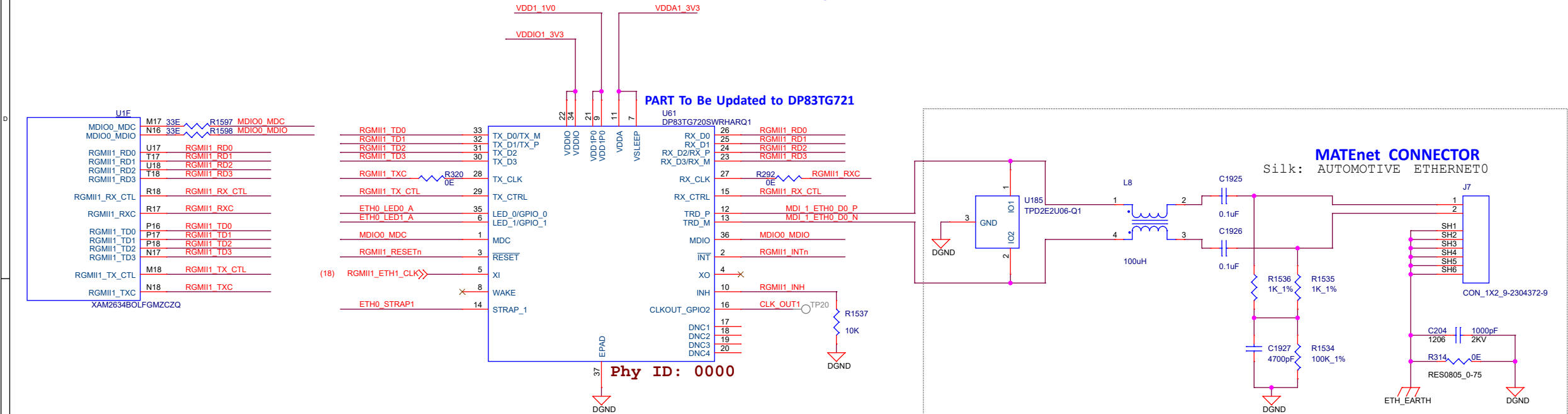
SOC JTAG, RESET and CLKS



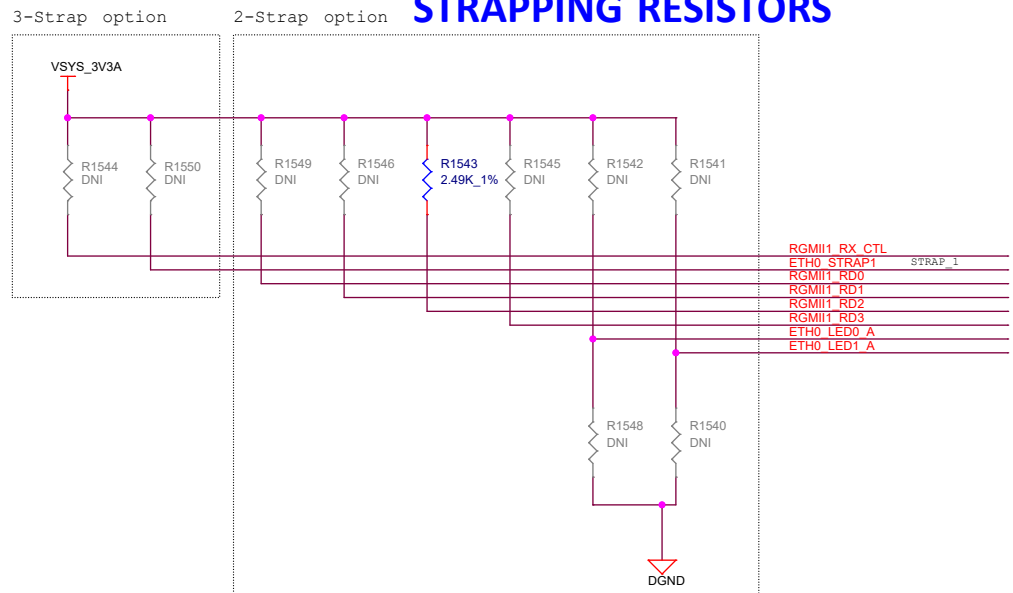
SW1.1	CONDITION	FUNCTION
LOW	HSEC EMU selected	A-->B1 port [ON Board EMU]
HIGH	XDS110 selected	A-->B2 port [EXTERNAL EMU]



# CPSW RGMII1/MII1 Ethernet



## STRAPPING RESISTORS



PHY ADDRESS = 00000  
MS = 0 Slave,AUTO = 0 Autonomous  
RGMII (Align Mode)

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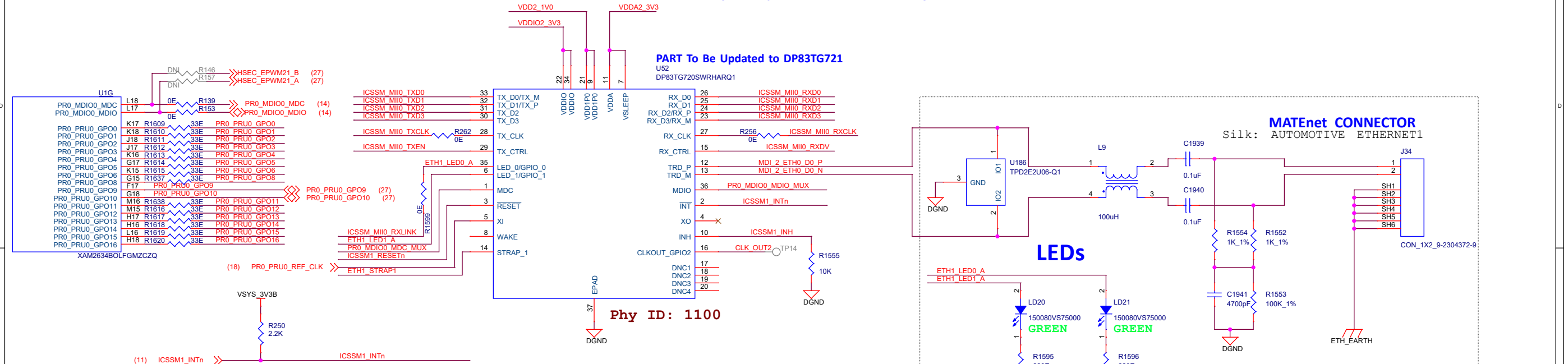
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C Variant Name = PROC153 001

Date: Monday, December 05, 2022

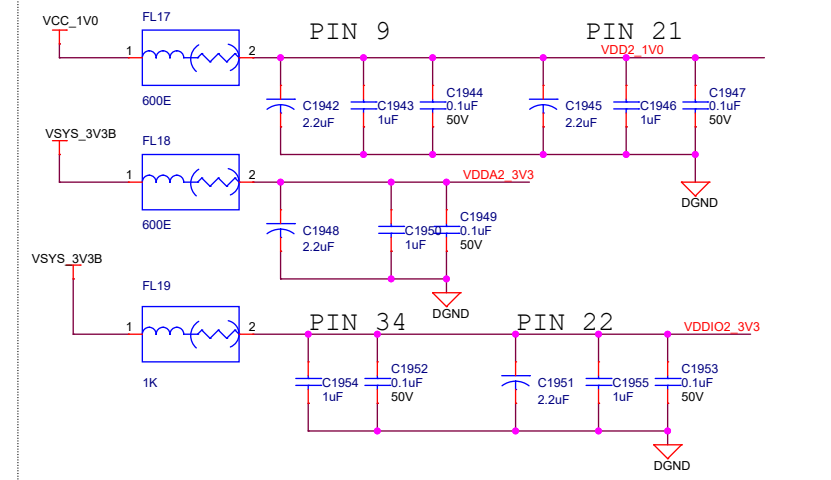
Sheet 12 of 28

Rev  
E1

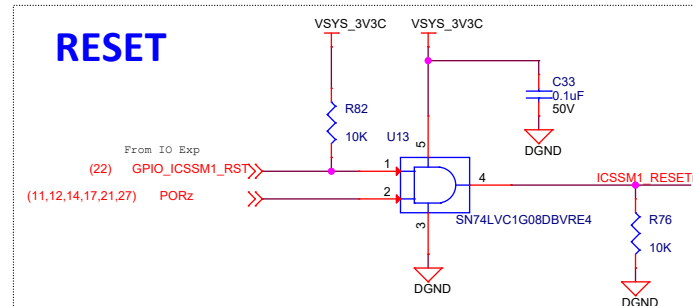
# PRU0 ICSSM RGMII/MII, CPSW RGMII2/MII2 Ethernet



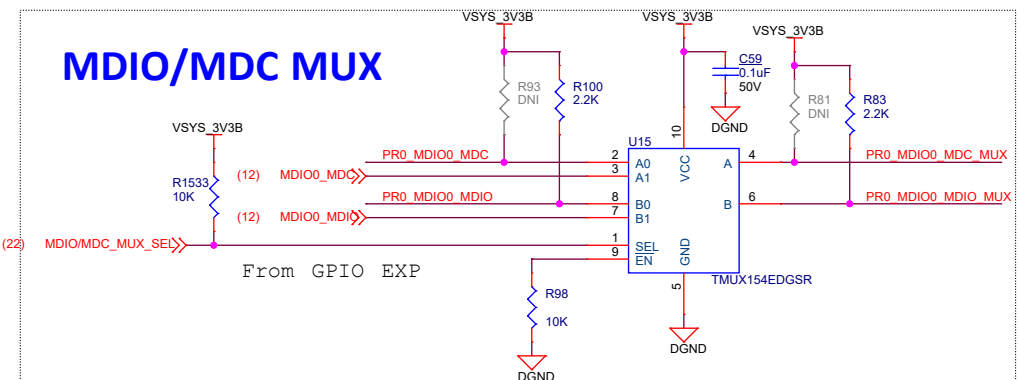
Place Near power pins of 10/100/1000 Ethernet PHY



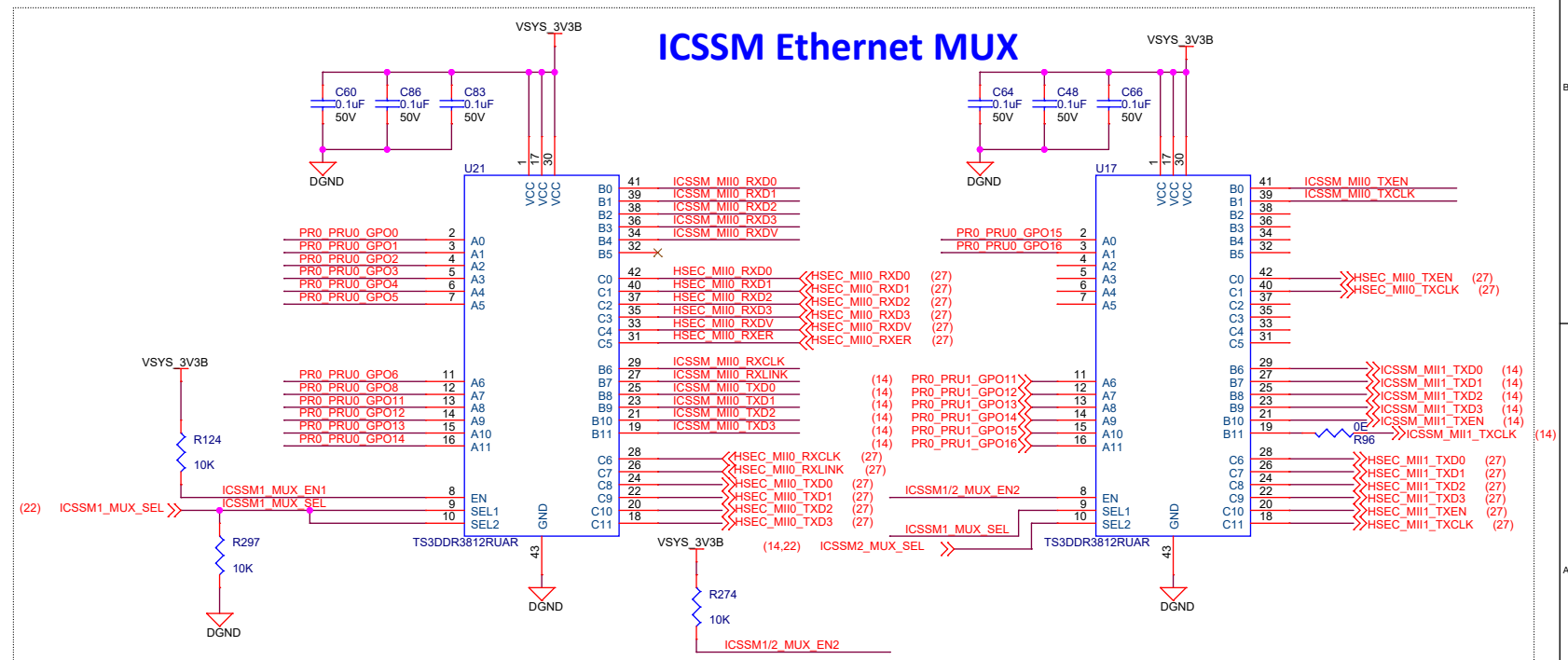
## RESET



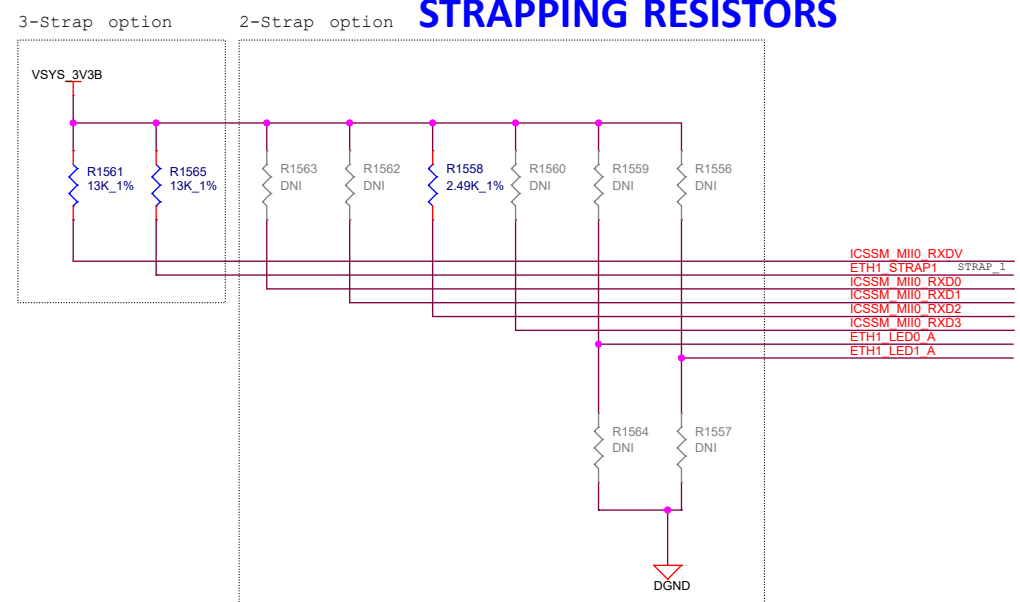
## MDIO/MDC MUX



## ICSSM Ethernet MUX



## STRAPPING RESISTORS



PHY ADDRESS = 01100  
MS = 0 Slave,AUTO = 0 Autonomous  
RGMII (Align Mode)

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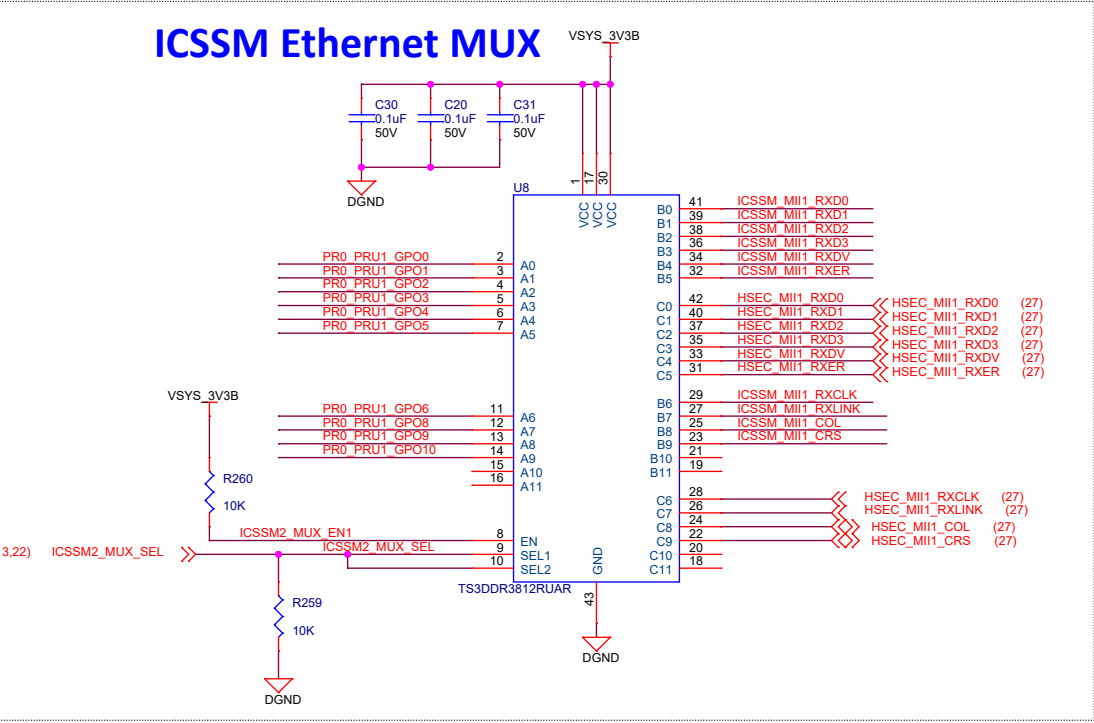
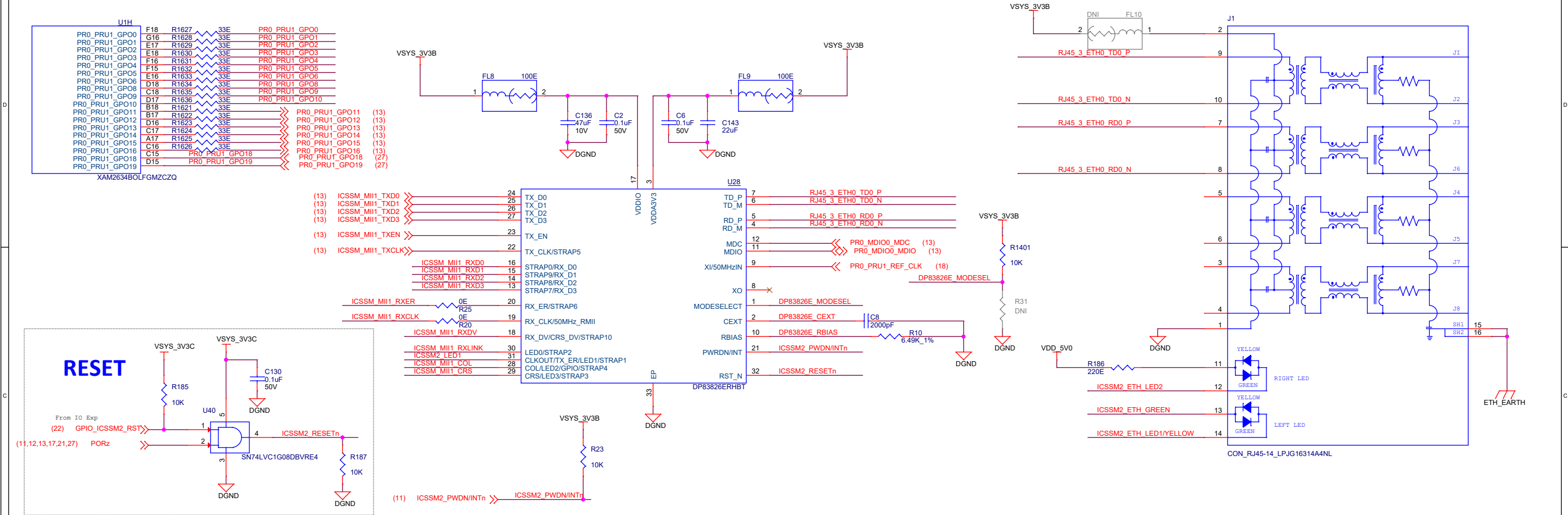


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C		E1
Date:	Monday, December 05, 2022	Sheet 13 of 28

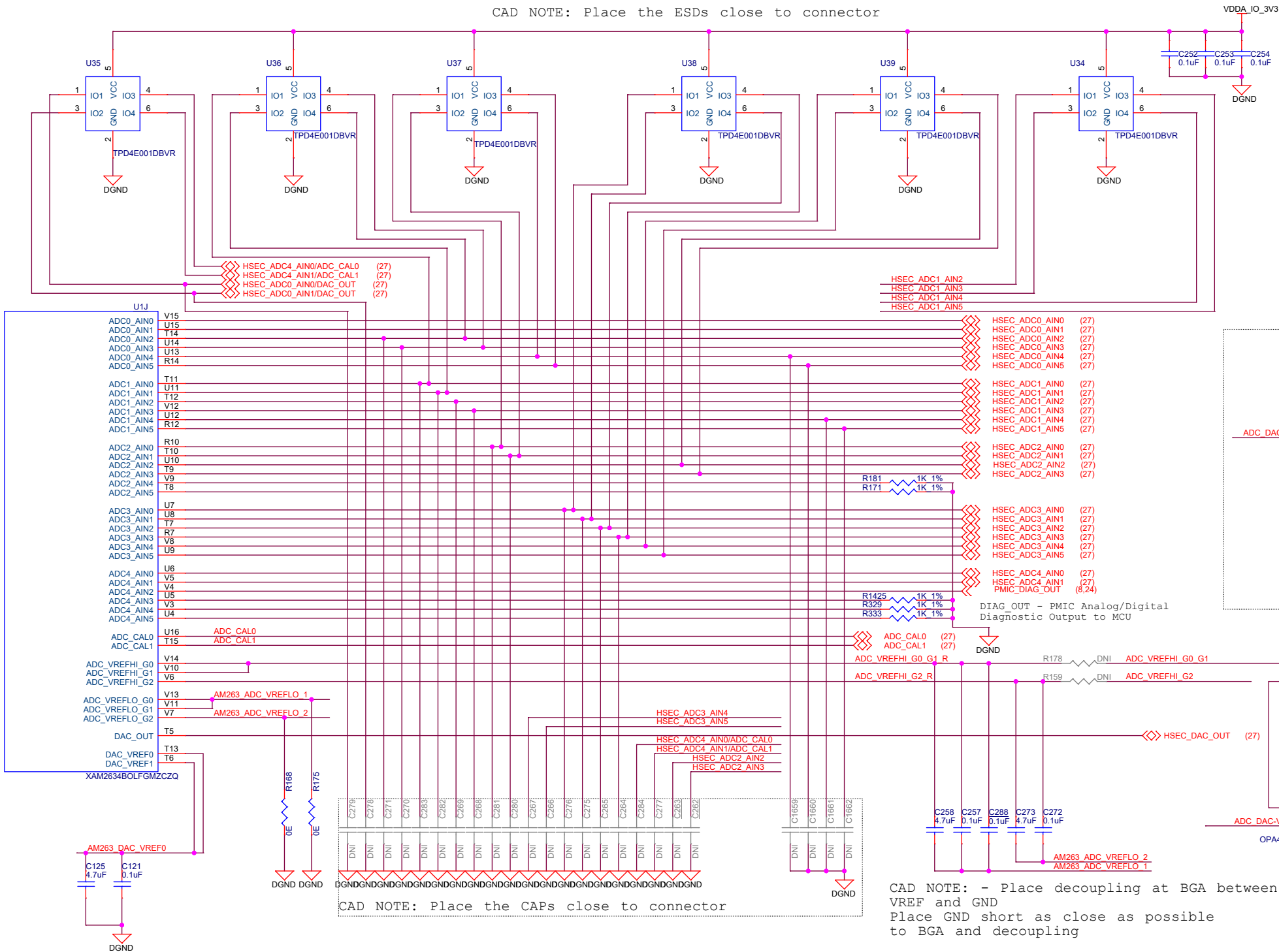


PRU1 ICSSM RGMII/MII Ethernet



# ADC and DAC Interfaces

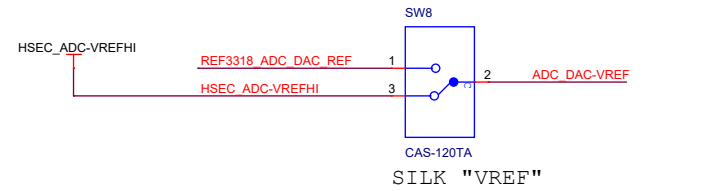
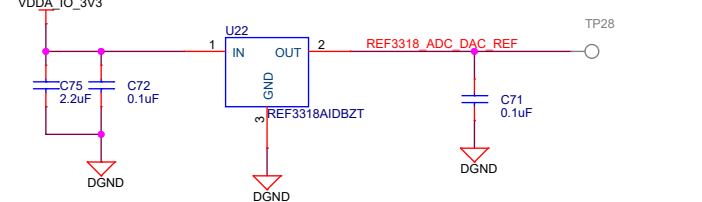
CAD NOTE: Place the ESDs close to connector



CAD NOTE: Place the CAPs close to connector

CAD NOTE: - Place decoupling at BGA between VREF and GND  
Place GND short as close as possible to BGA and decoupling

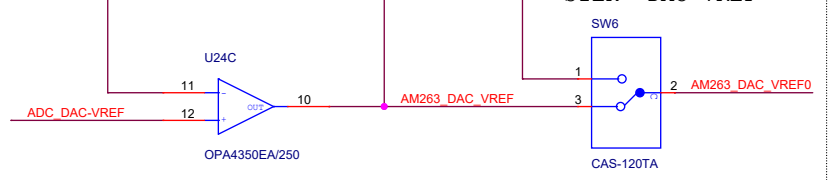
## REF Voltage Generation



### REF VOLTAGE SELECTION

SW POSITION	SUPPLY SELECTION
PIN 1-2	ON BOARD REF IS SELECTED
PIN 2-3	HSEC SUPPLY IS SELECTED

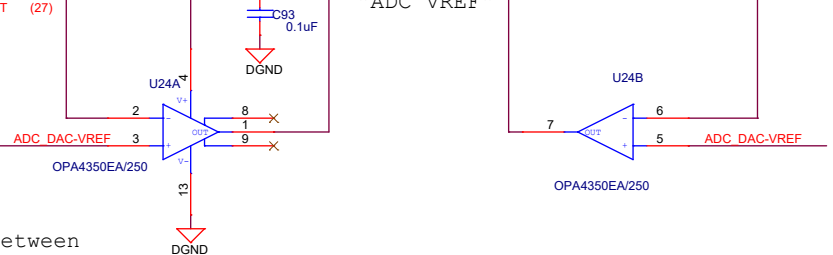
## SILK "DAC VREF"



### DAC REF VOLTAGE SELECTION

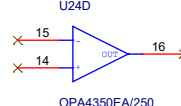
SW POSITION	SUPPLY SELECTION
PIN 1-2	Allows AM263x on-die LDO reference (Routed n PCB)
PIN 2-3	selects output of VREF switch

## SILK "ADC VREF"



### ADC REF VOLTAGE SELECTION

SW POSITION	SUPPLY SELECTION
PIN 1-2	OPEN - Allows AM263x on-die LDO reference (routed on-die)
PIN 2-3	selects output of VREF switch
PIN 4-5	OPEN - Allows AM263x on-die LDO reference (routed on-die)
PIN 5-6	selects output of VREF switch



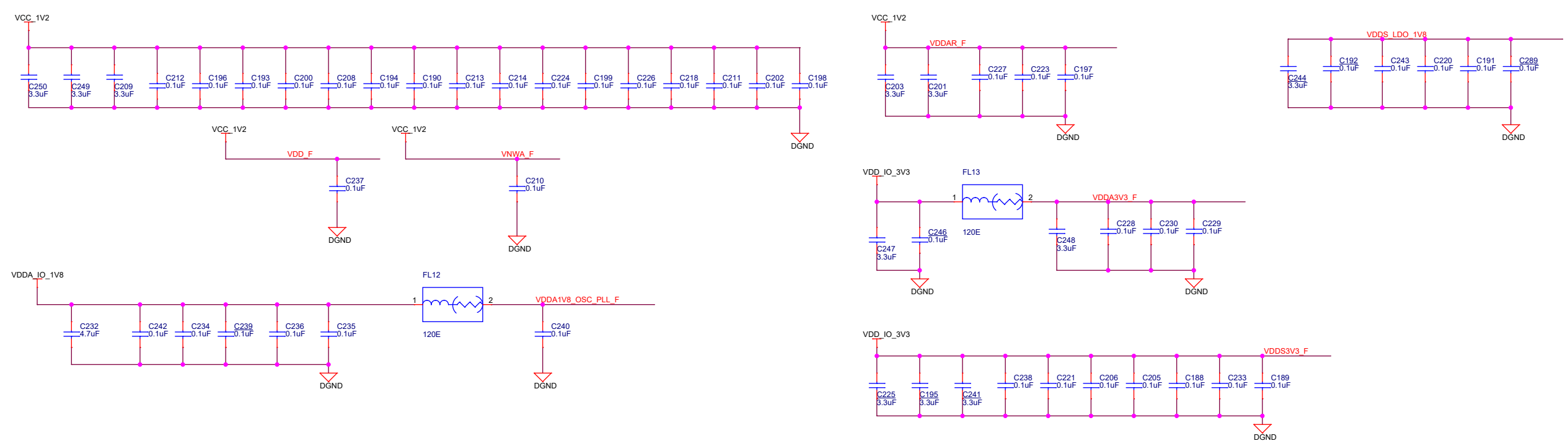
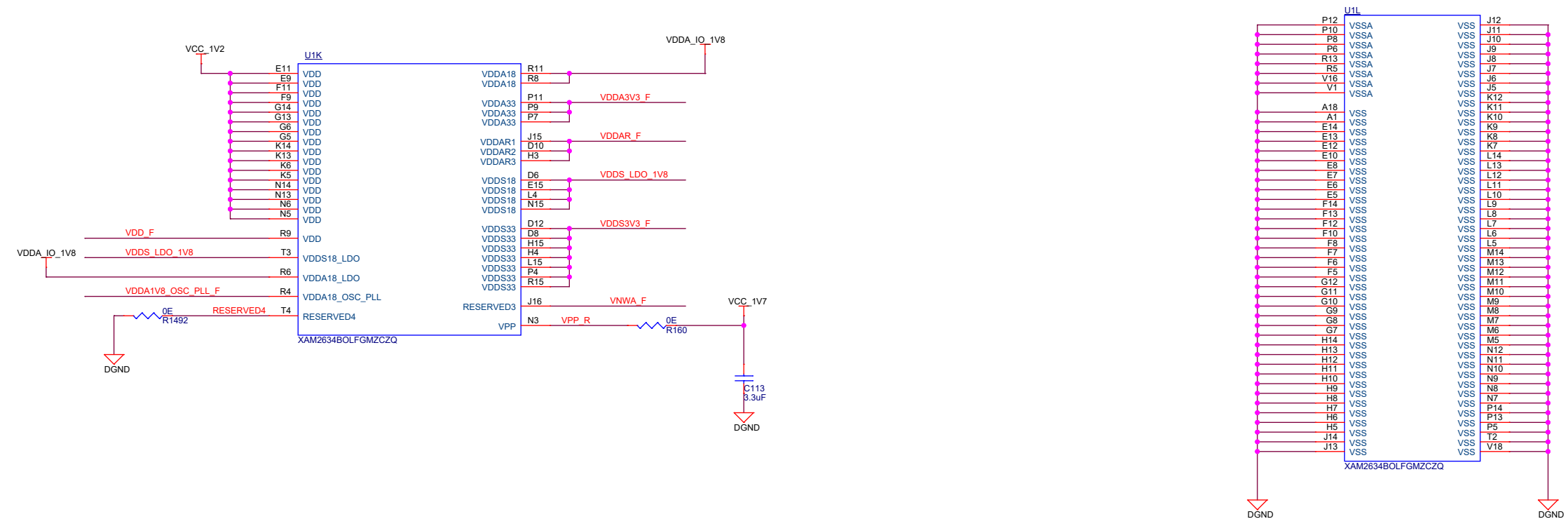
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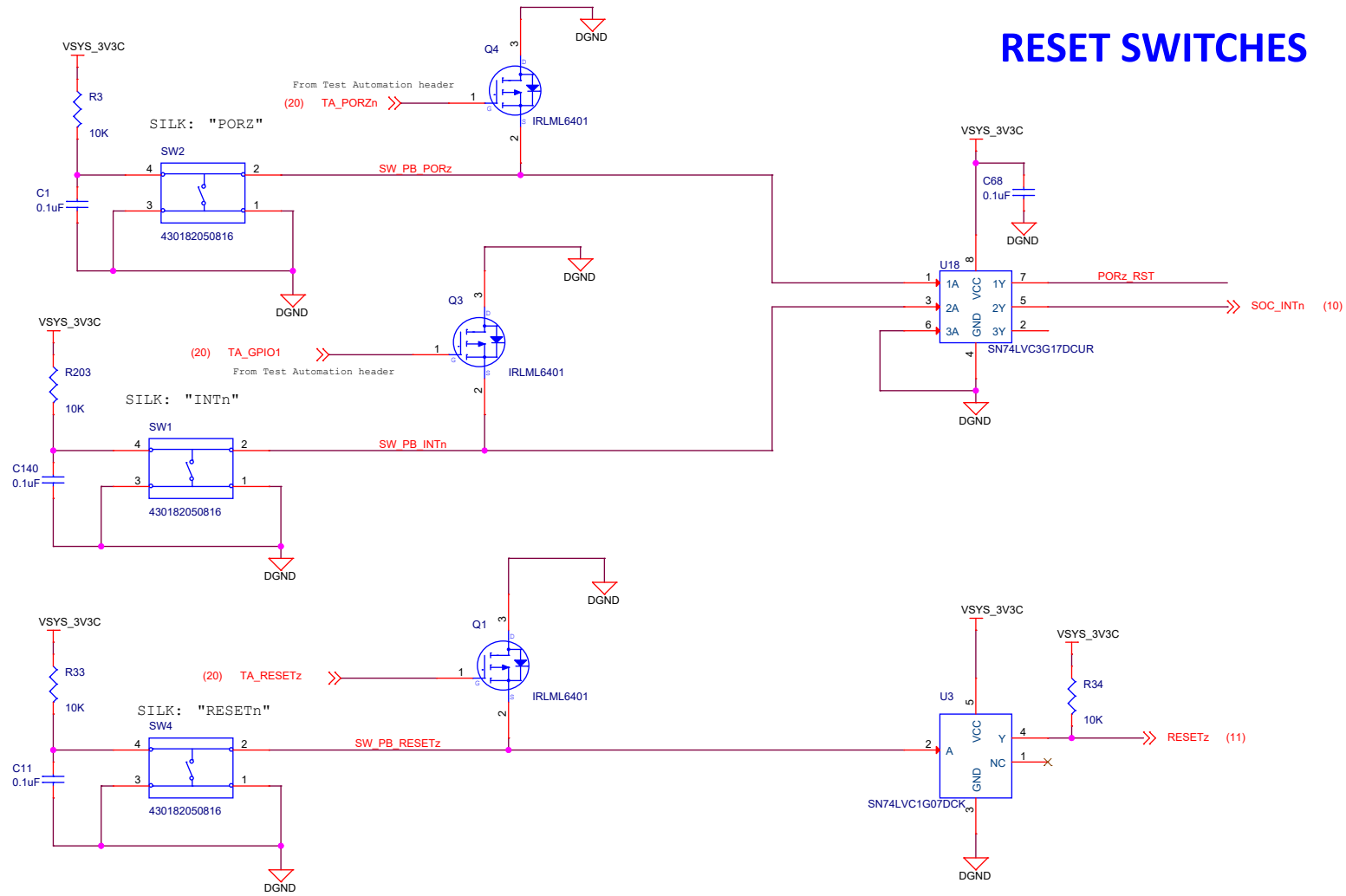
Size	Variant Name = PROC153 001	Rev
C		E1
Date:	Monday, December 05, 2022	Sheet 15 of 28

SOC-POWER and GND

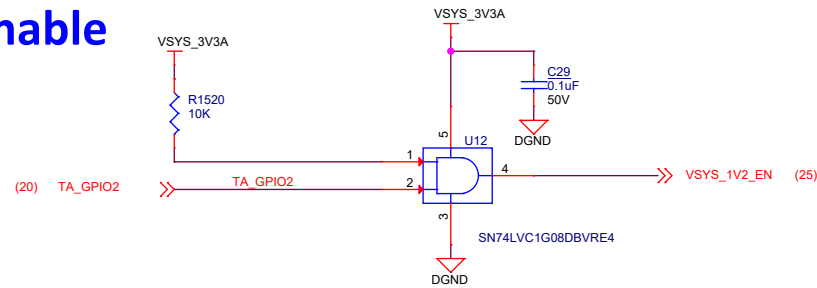




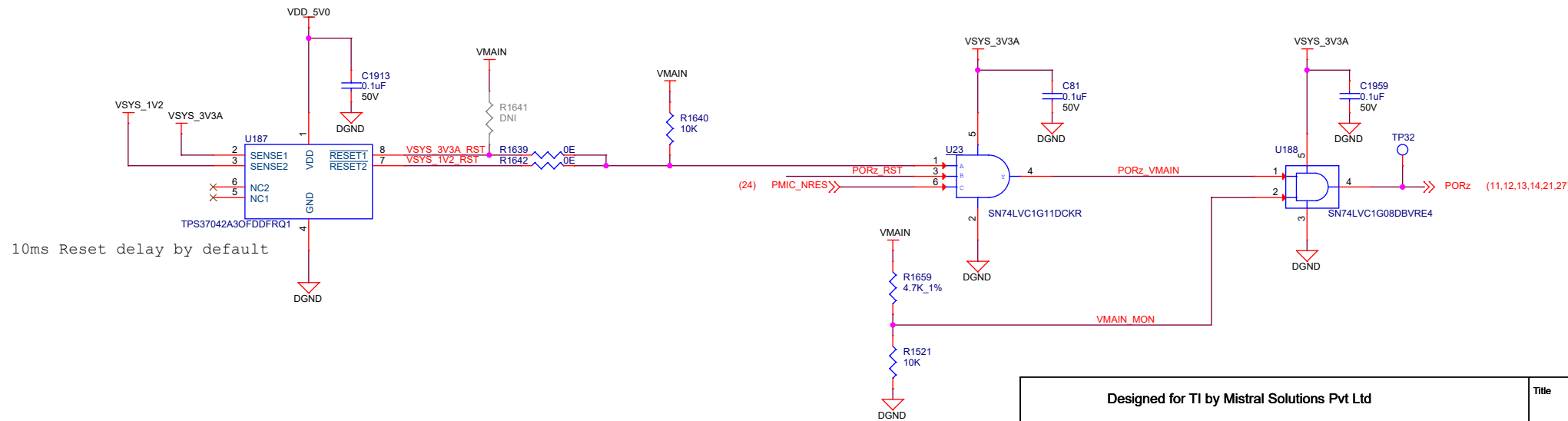
## RESET SWITCHES



## 1.2V Enable



## PORz



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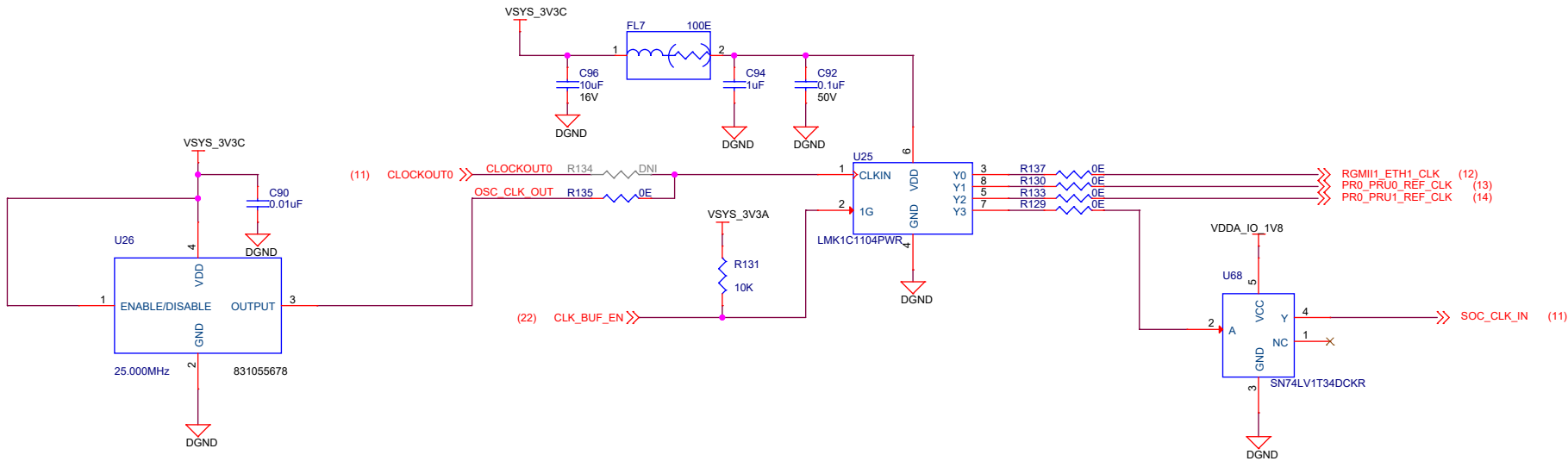
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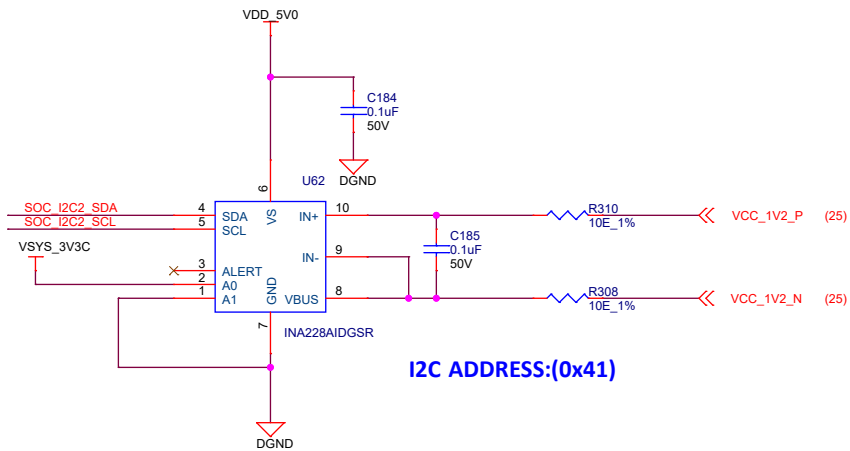
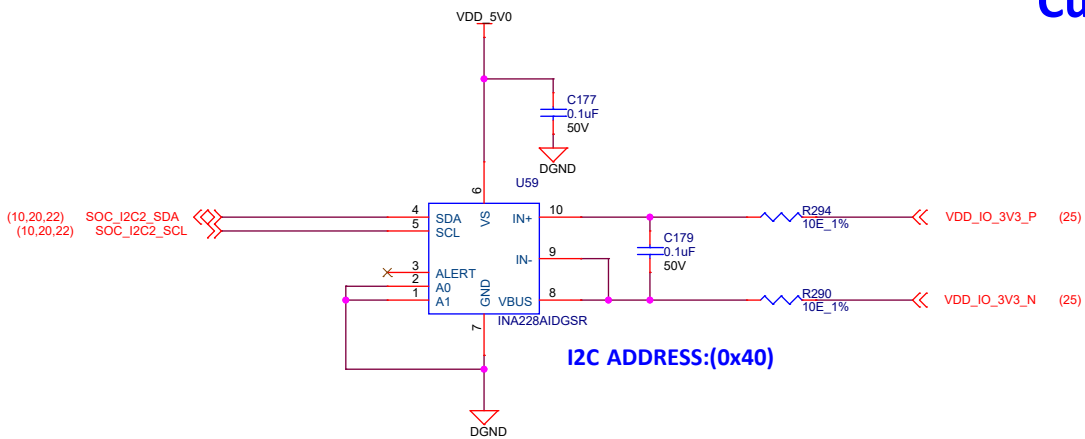
Sheet 17 of 28

Rev E1

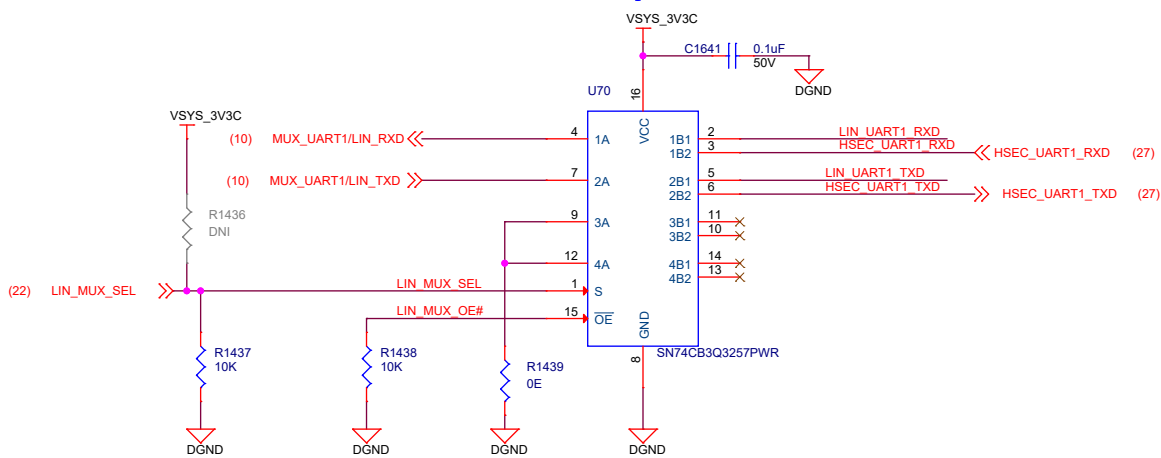
CLOCKS



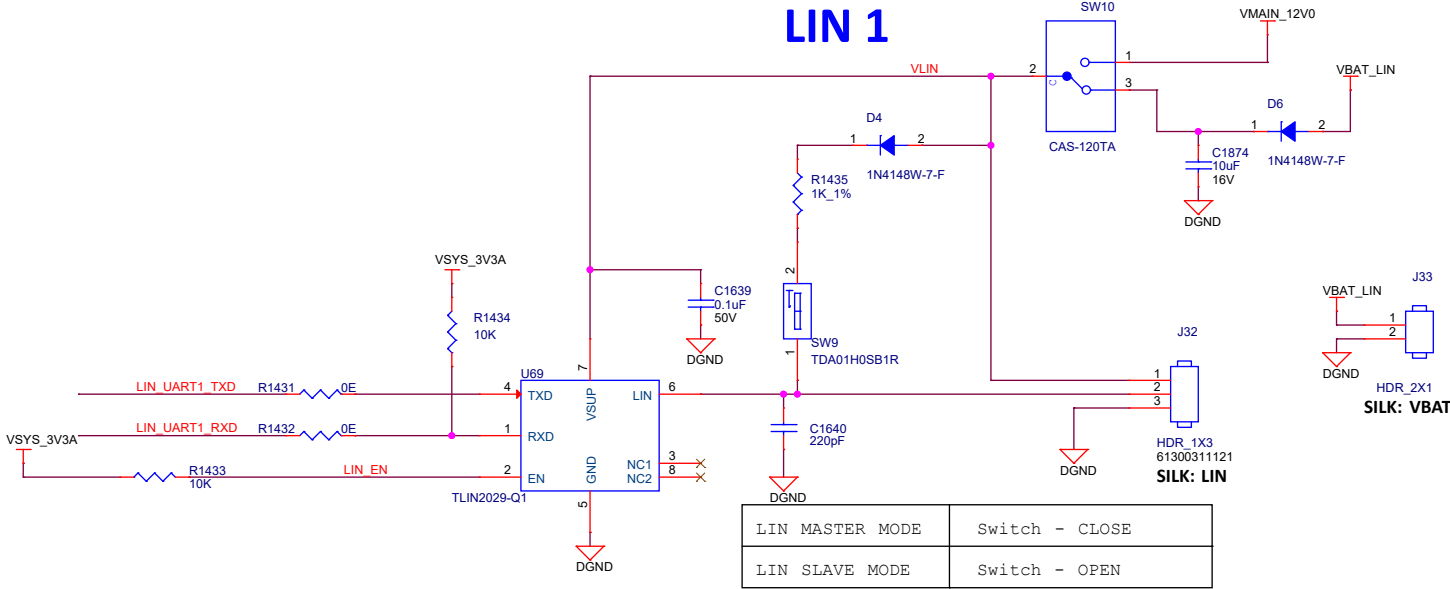
Current Monitors



LIN MUX/DEMUX



LIN 1



I2C0 - 1:2 MUX

SEL	CONDITION	FUNCTION
LOW	LIN SELECTED	A-->B1 port
HIGH	HSEC UART selected	A-->B2 port

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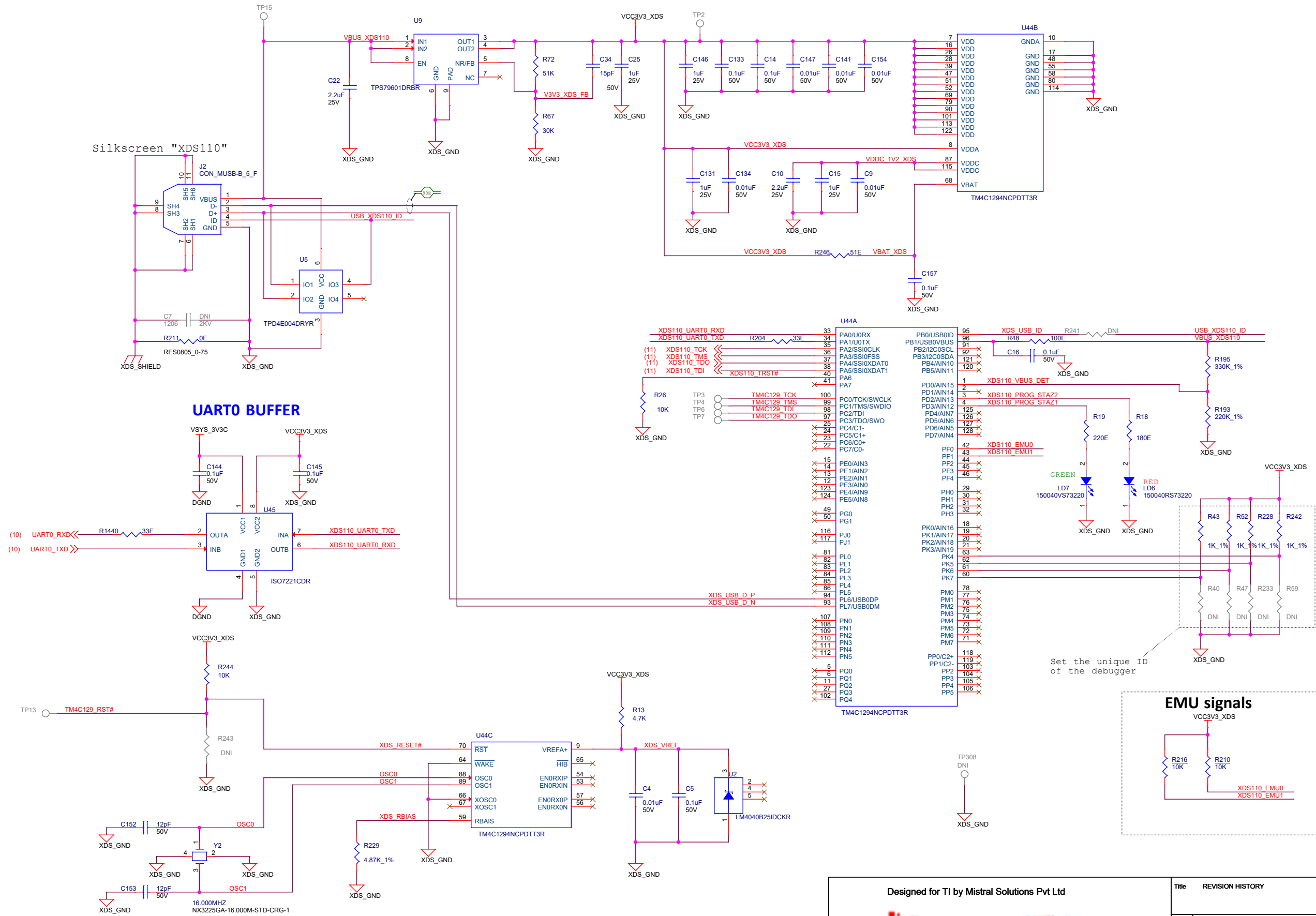
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Size	Variant Name = PROC153 001	Rev
C		E1

Date: Monday, December 05, 2022

Sheet 18 of 28

# XDS110 DEBUGGER



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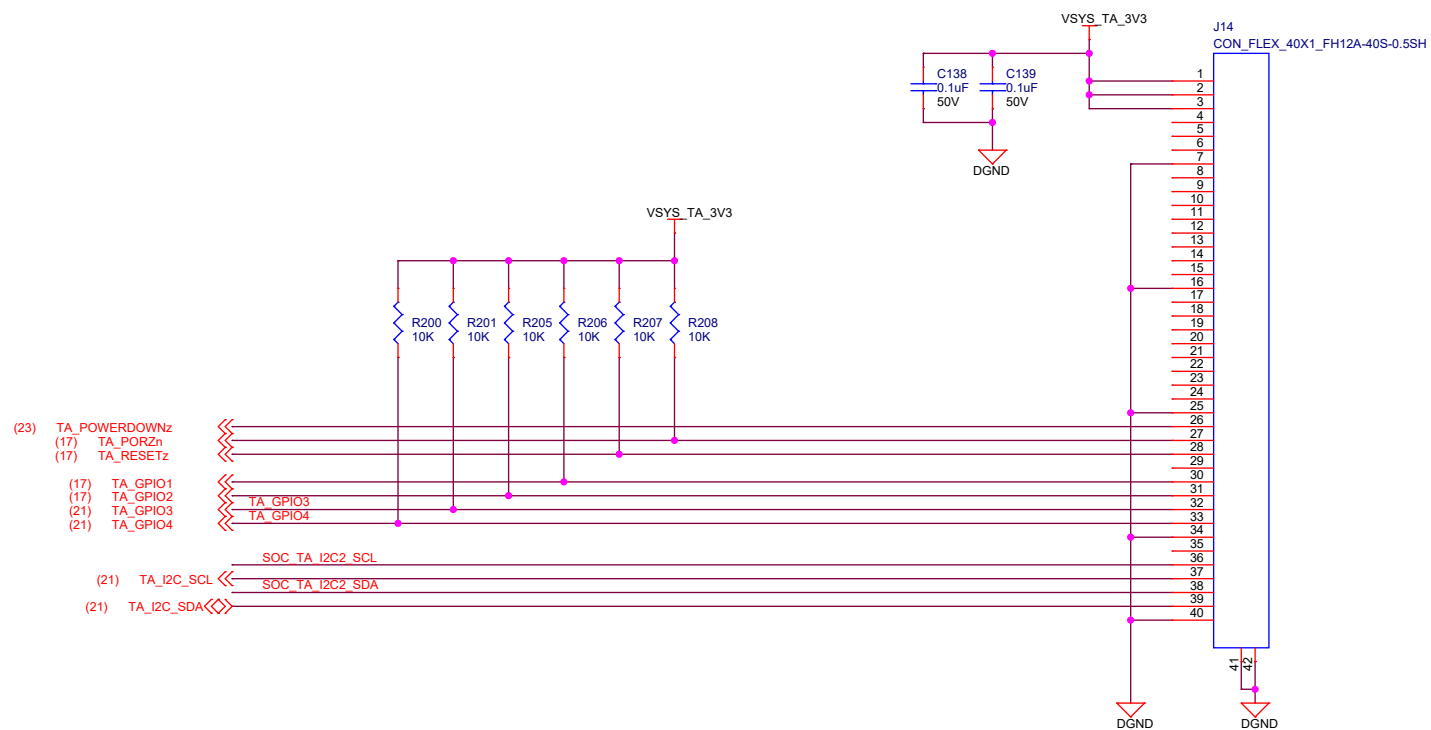


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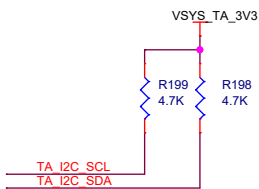
Size			Rev
C	Variant Name = PROC153 001		E1
Date:	Monday, December 05, 2022	Sheet	19 of 28

TEST AUTOMATION HEADER

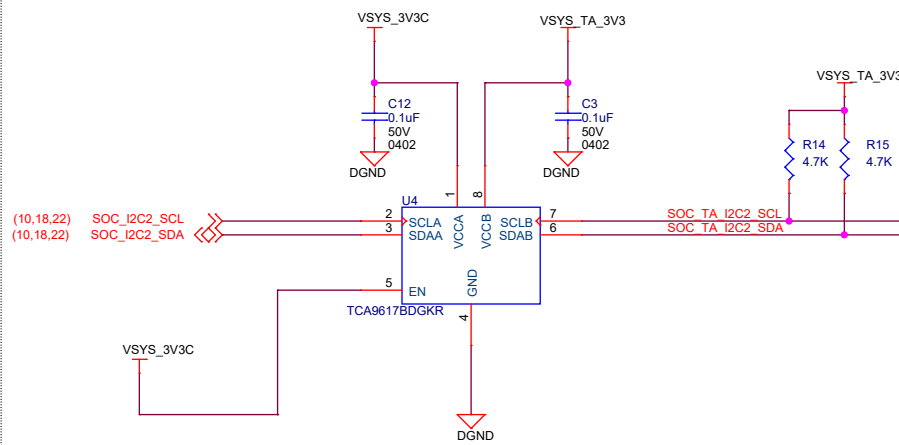
AUTOMATION INTERFACE  
Cable : Parlex-050R40-76B, .5mm 3"



I2C Pull Ups



I2C BUFFER



TEST AUTOMATION GPIO MAPPING

SIGNAL NAME	DESCRIPTION	Direction WRT CTRL	Internal/ External PU/PD states
TA_POWERDOWN	Used to Power down the system	OUTPUT	External Pullup
TA_PORZn	Used to Reset the SoC PORz	OUTPUT	External Pullup
TA_RESETz	SoC Warmreset	OUTPUT	External Pullup
TA_GPIO1	Interrupt to SOC	OUTPUT	External Pullup
TA_GPIO2	Used to Enable or Disable 1.2V Regulator	OUTPUT	External Pullup
TA_GPIO3	Used to Enable the BOOTMODE Buffer	OUTPUT	External Pullup
TA_GPIO4	Used Reset Bootmode IO Exp	OUTPUT	External Pullup

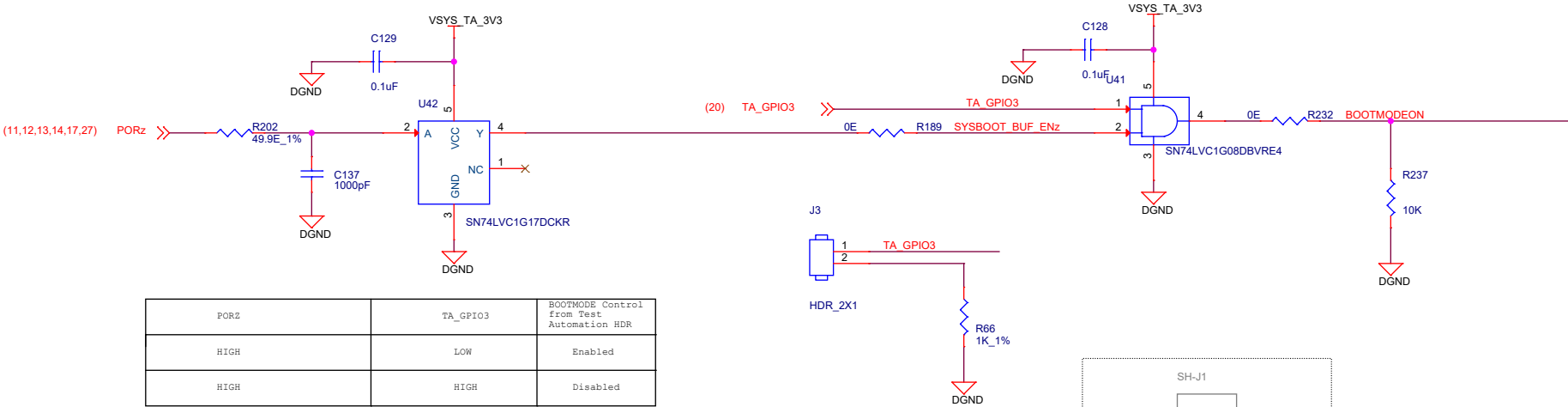
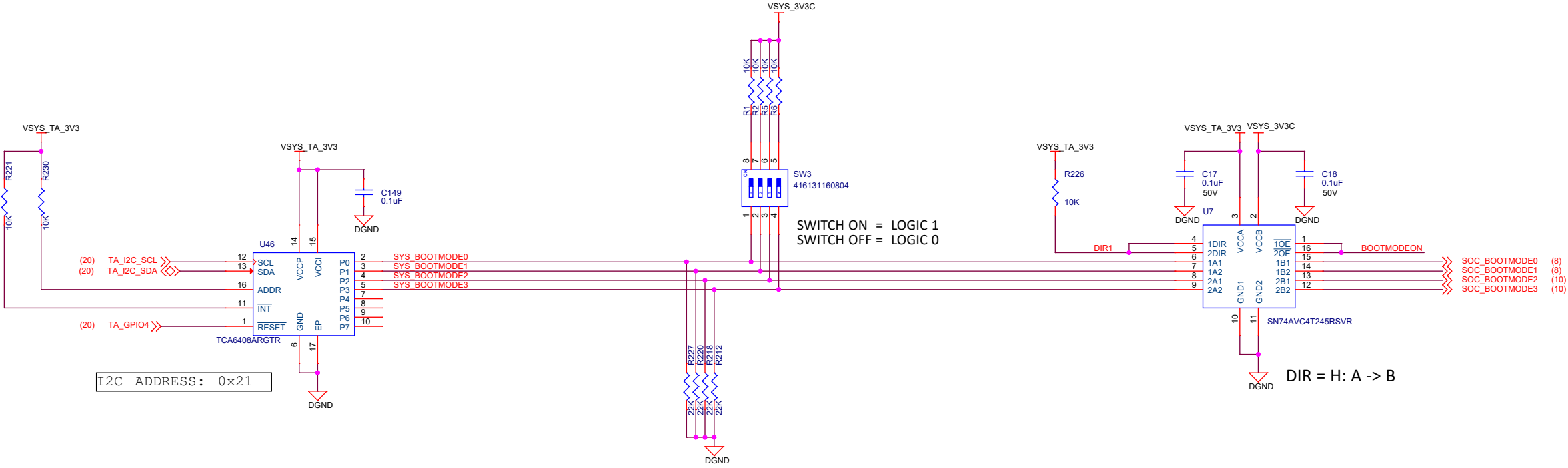
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Size	Variant Name = PROC153 001	Rev
C		E1
Date:	Monday, December 05, 2022	Sheet 20 of 28

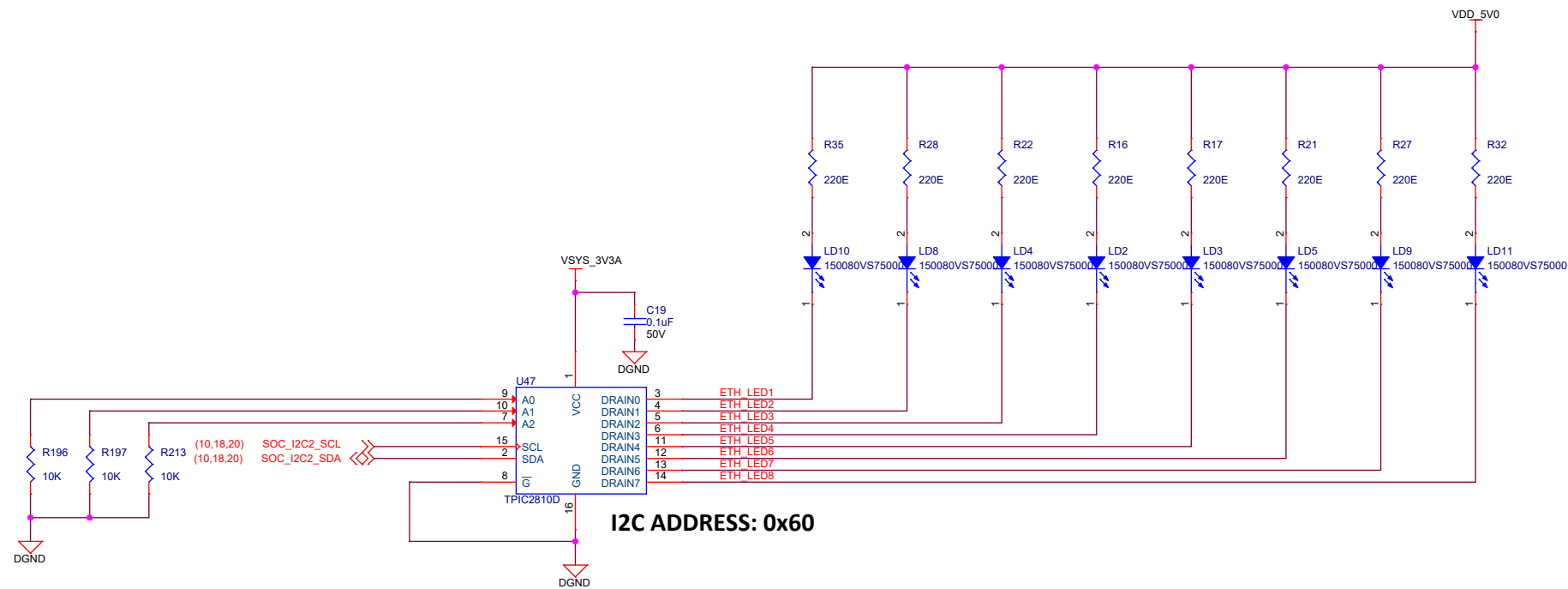
BOOTMODE BUFFER AND SWITCH



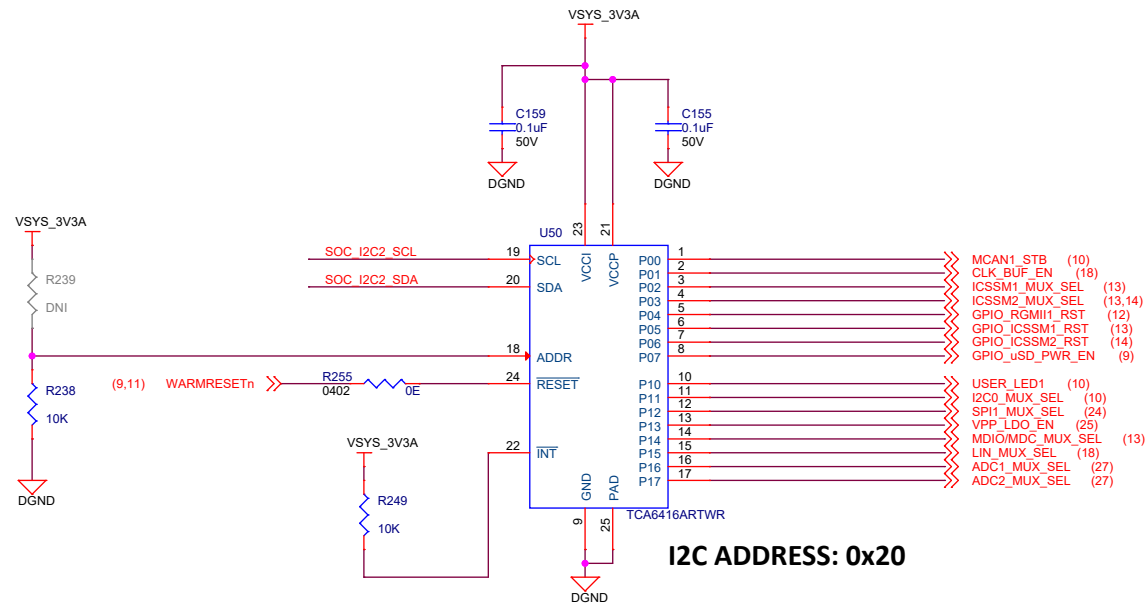
PORz	TA_GPIO3	BOOTMODE Control from Test Automation HDR
HIGH	LOW	Enabled
HIGH	HIGH	Disabled

SH-J1  
DNI  
SH-J1 Shall be mounted to enable the bootmode buffer

# LED Driver



# IO Expander



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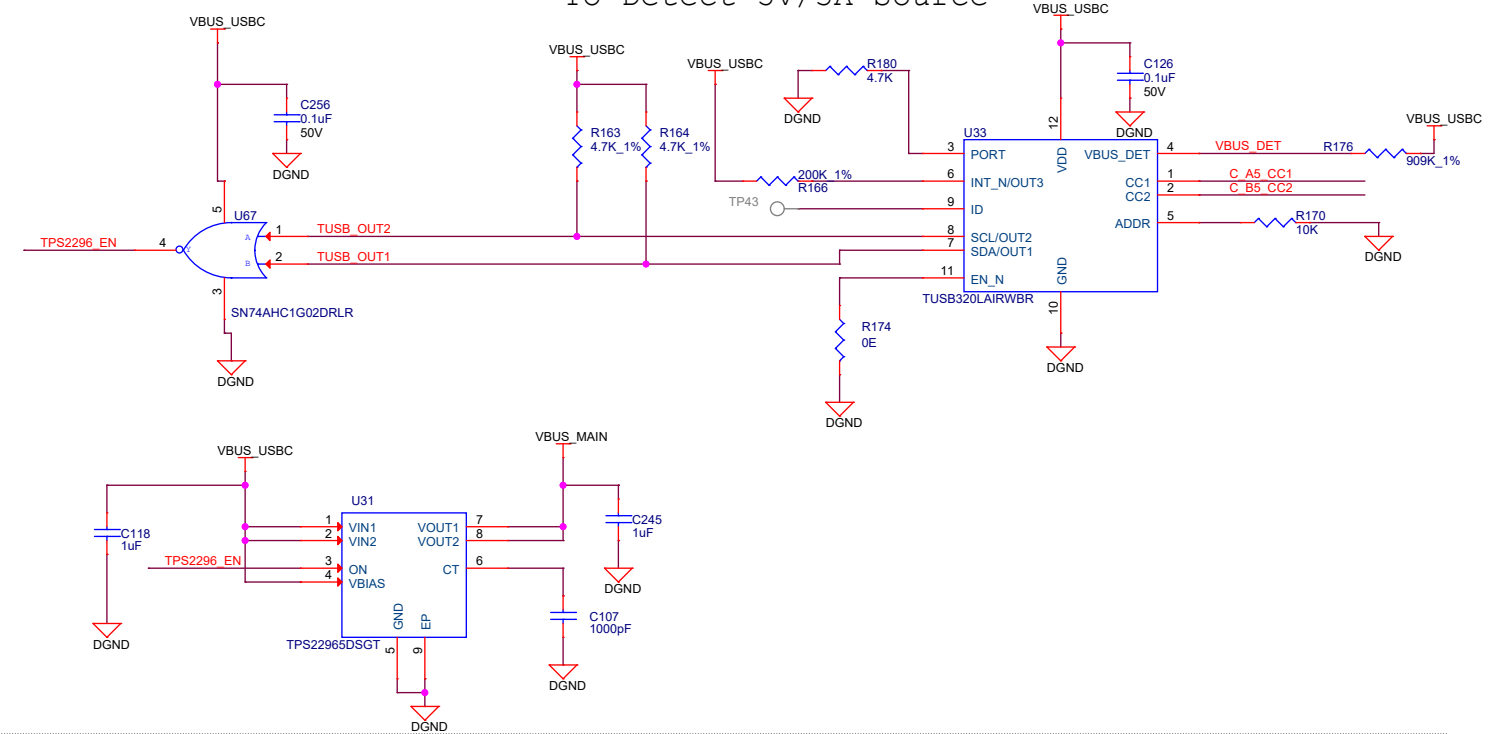
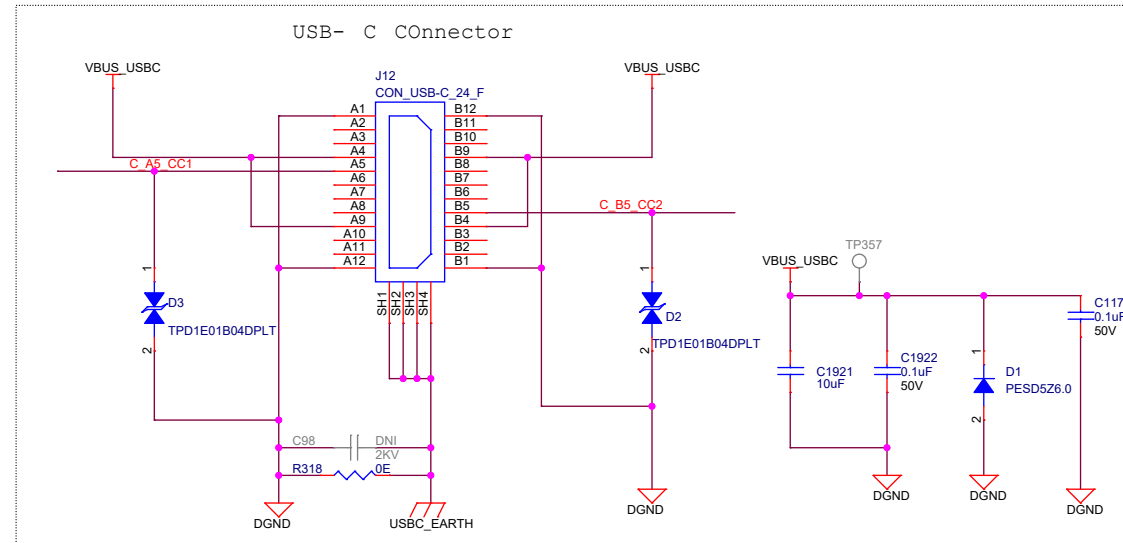


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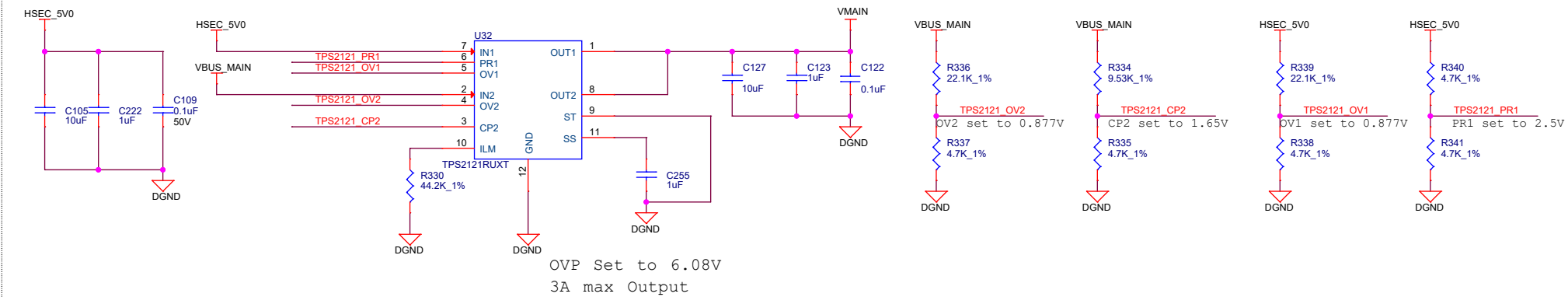
Size	Variant Name = PROC153 001	Rev
C		E1
Date:	Monday, December 05, 2022	Sheet 22 of 28

## USB-C Power

Configured as UFP MODE  
To Detect 5V/3A Source



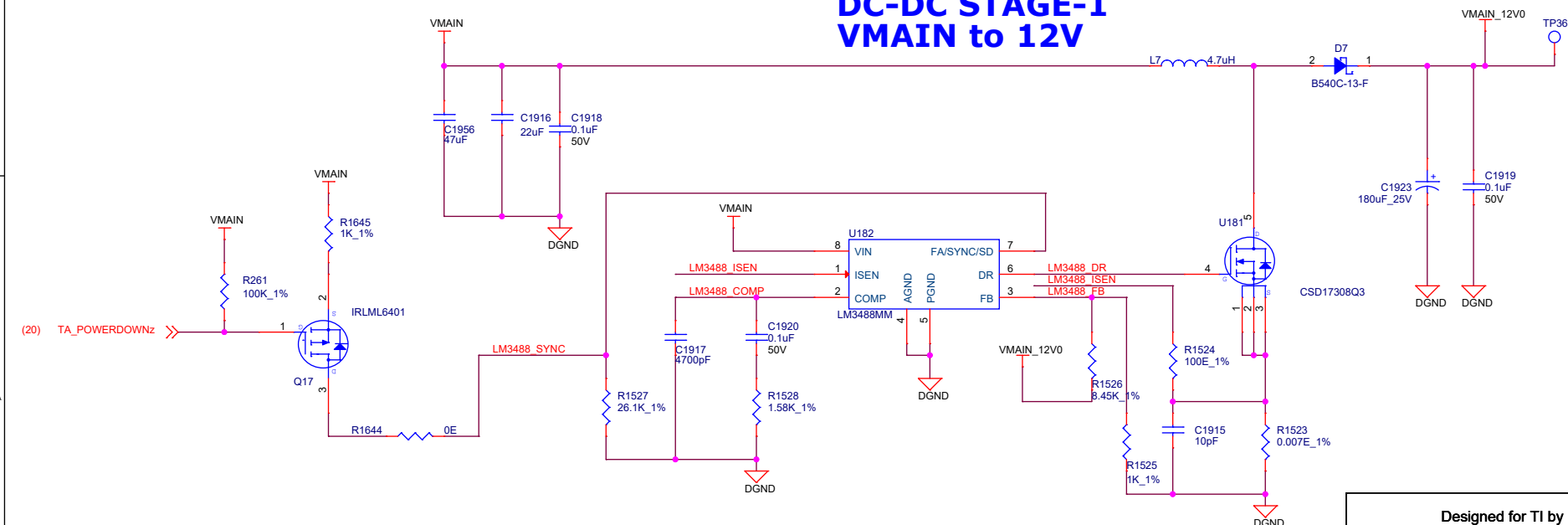
## Power MUX



	XCOMP	OUTPUT
V	PR1 > CP2	HSEC_5V0
	PR1 = < CP2	VBUS_MAIN

Designed as per reference sch

## DC-DC STAGE-1 VMAIN to 12V



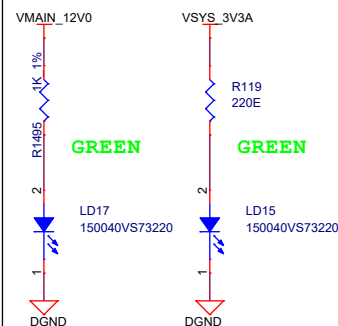
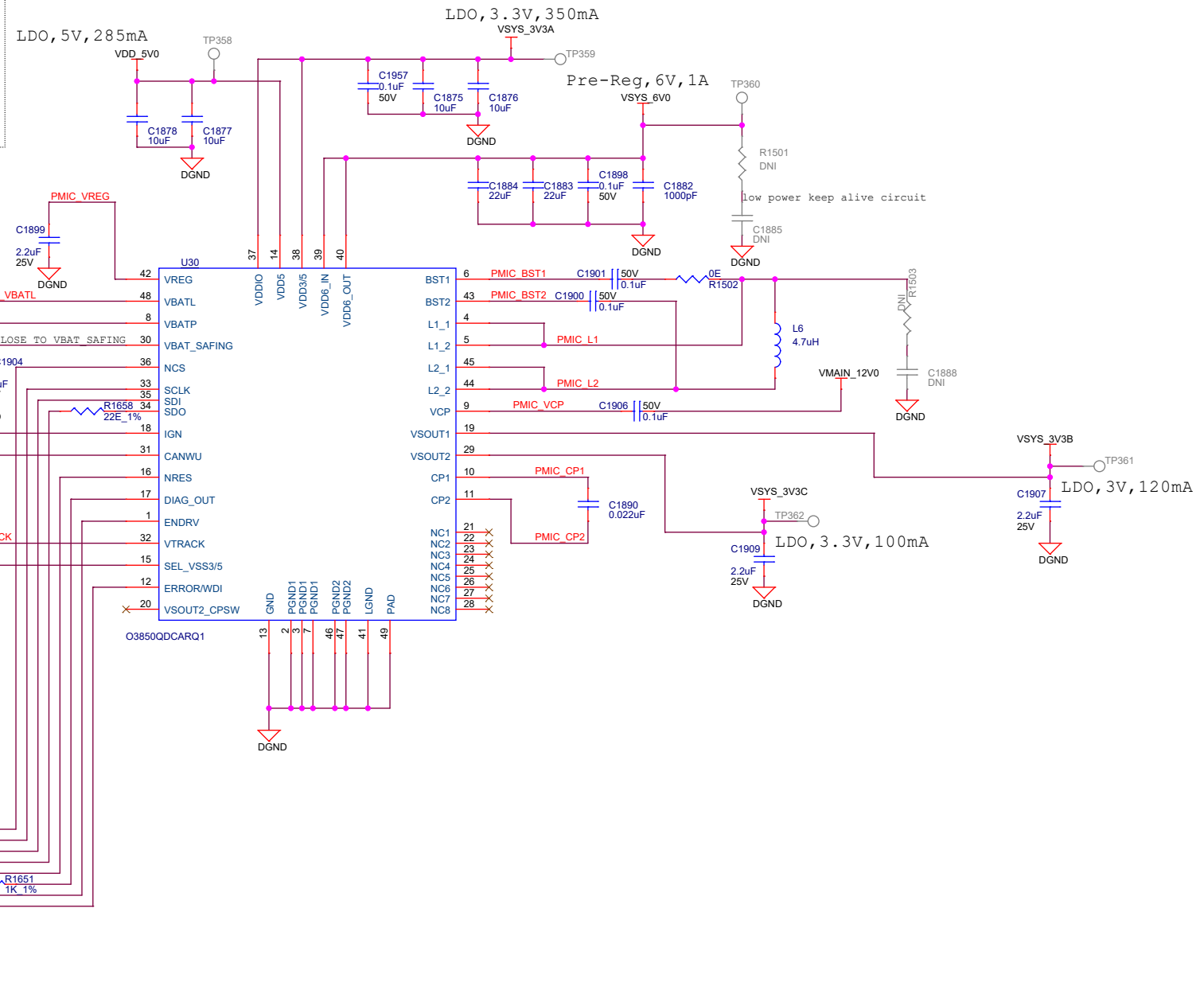
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Title	REVISION HISTORY
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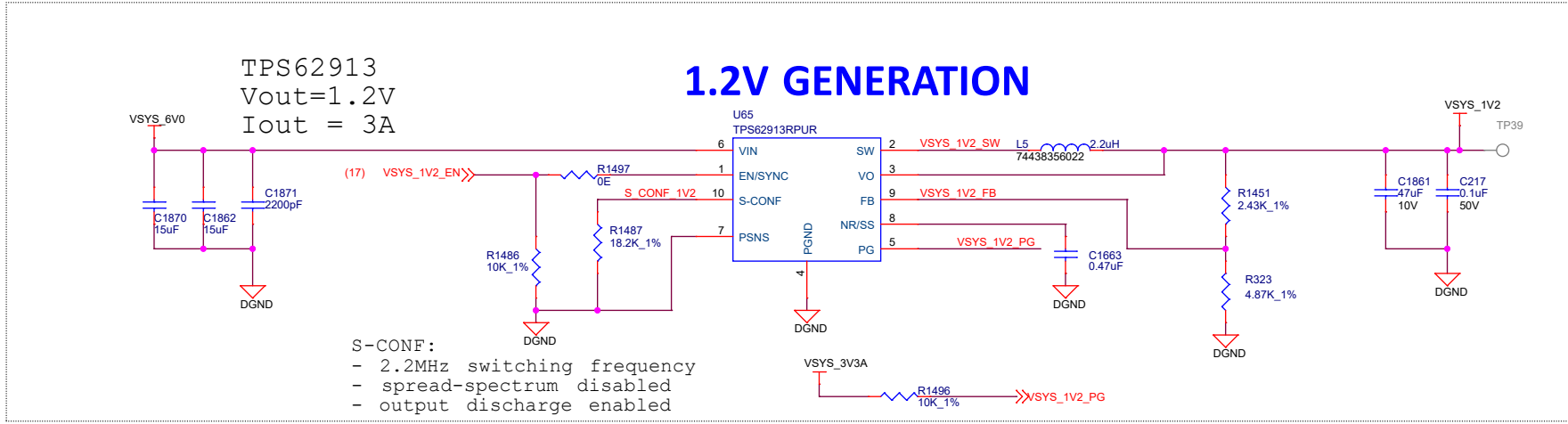
Size	Variant Name = PROC153 001	
C		
Date:	Monday, December 05, 2022	Sheet 23 of 28

## MAIN Power and PMIC

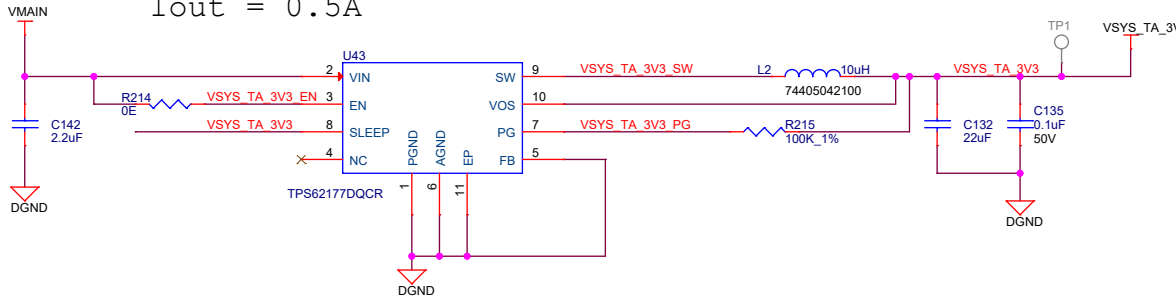




## Power Supply #1



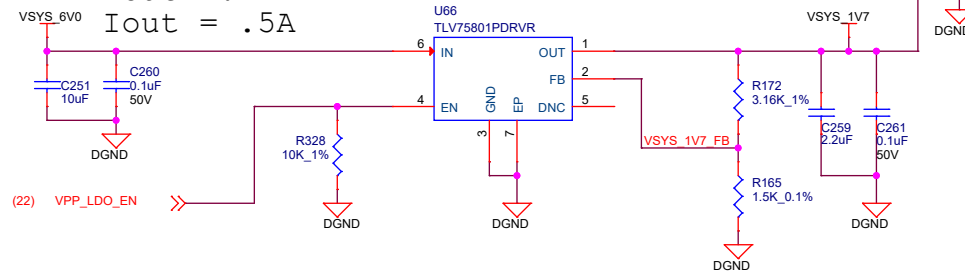
## Test Automation Header Supply

TPS62177 3.3V BUCK REGULATOR  
Vout = 3.3V  
Iout = 0.5A

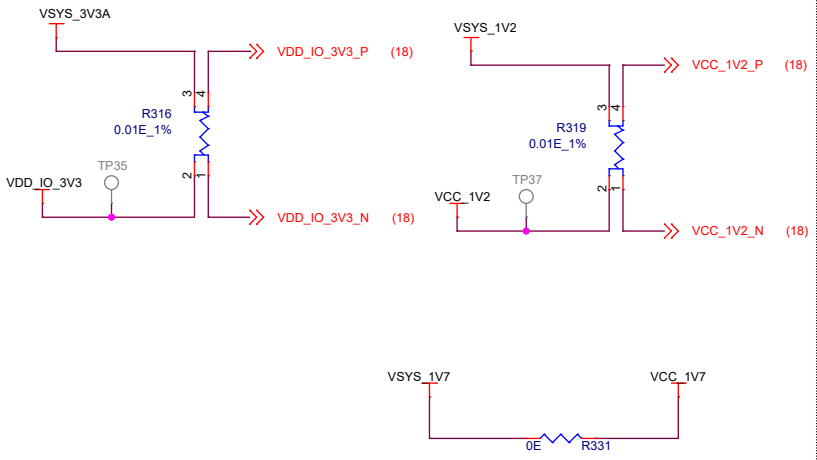
## 1.7V VPP Generation

Place testpoints with  
100mils spacing to  
insert external jumper

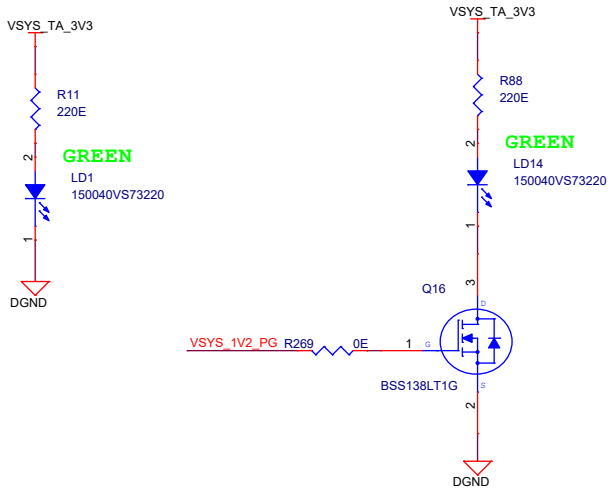
TLV75801  
Vout=1.7V  
Iout = .5A



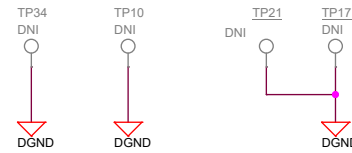
## Voltage In-Line Resistors



## Power LED



### Ground Test Points



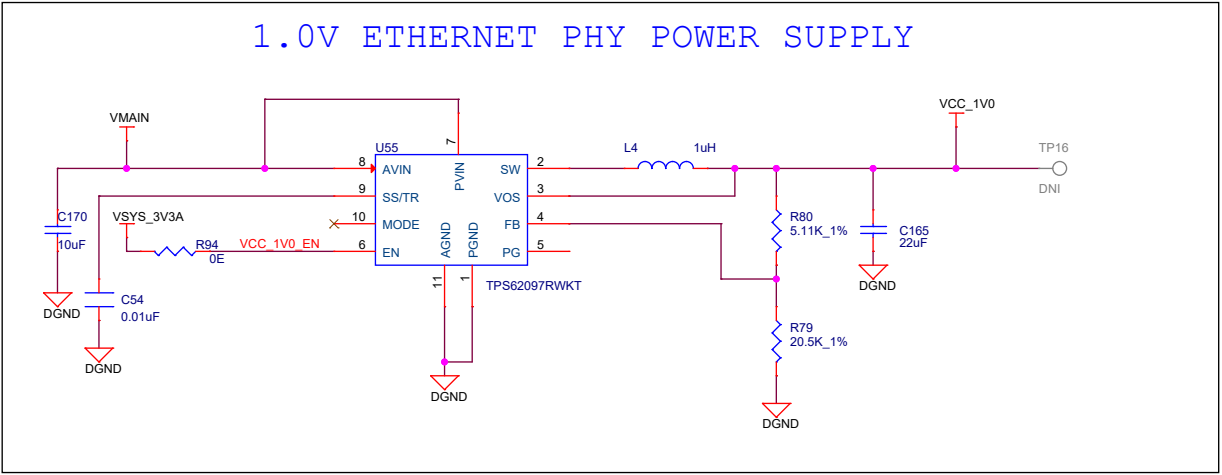
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Title	REVISION HISTORY
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Size	Variant Name = PROC153 001	Rev
C		E1
Date:	Monday, December 05, 2022	Sheet 25 of 28

Ethernet Powers



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Title REVISION HISTORY

Size  
C Variant Name = PROC153 001

Rev  
E1

Date: Monday, December 05, 2022 Sheet 26 of 28



# EVM Development & Evaluation test circuitry

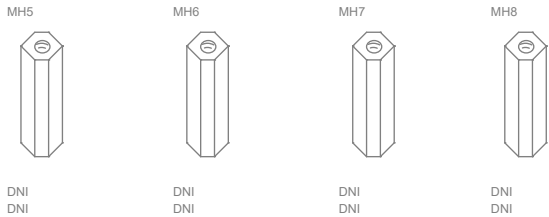
## (TI EVM Only)

### NOTES, HW & LABELS

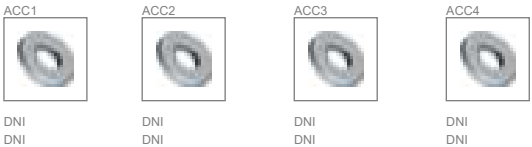
#### ASSEMBLY NOTES

1. All MSL components should be baked as per JEDEC standard.
2. PCB should be baked at 120 degree for 8 hours.
3. Board assembly must comply with workmanship standards. IPC-A-610 Class 2, unless otherwise specified.
4. These assemblies are ESD sensitive, ESD precautions shall be observed.
5. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
6. Provide serial numbers to the assembled boards for identification.
7. The assembled board are wrapped in ESD Covers(individual) and packed securely before shipment.

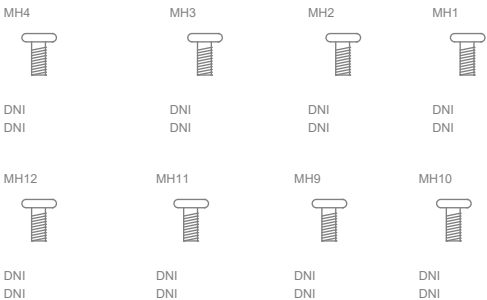
#### STANDOFFS



#### WASHER's



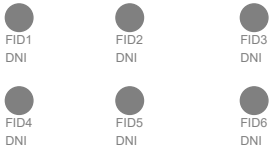
#### SCREWS



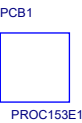
#### RUBBER FEET



#### FIDUCIALS



#### BARE PCB



#### LABELS

##### Board Serial No.



##### Assembly Revision.

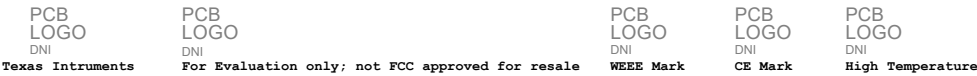


##### EVM Orderable No.



Orderable Part Numbers	
Variant	Label Text
001	TMDSCNCD263AUTO

#### LOGOs



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Title REVISION HISTORY

Size	Variant Name = PROC153 001		Rev
C			E1
Date:	Monday, December 05, 2022	Sheet 28 of 28	