AM263x CC AUTO

PROC153E2

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Title REVISION HISTORY

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REVISION HISTORY

REV #	DATE	DESCRIPTION OF CHANGES	AUTHOR	REVIEWED BY	APPROVED BY
E1	04 APR 2022	Drafted from E2	Mistral Design Team		
	09 MAY 2022	Updated TI comments about power section	Mistral Design Team		
	22 JUL 2022	Updated TI comments about power section	Mistral Design Team		
	03 AUG 2022	Updated U66 Part to TPS75801	Mistral Design Team		
	14 OCT 2022	Updated RESET section as per TI comments	Mistral Design Team		
	18 NOV 2022	Updated TI comments	Mistral Design Team		
	05 DEC 2022	Updated TI comments and Changed SOC refdes to U1	Mistral Design Team		
E2	02 MAY 2023	Changed the supply from VSYS3V3_C to VSYS3V3_A for some sections as per the TI comments	Mistral Design Team		
	23 MAY 2023	Changed the location of Q17 from boost converter to PMIC Ignition pin and added 47uF for VMAIN supply	Mistral Design Team		

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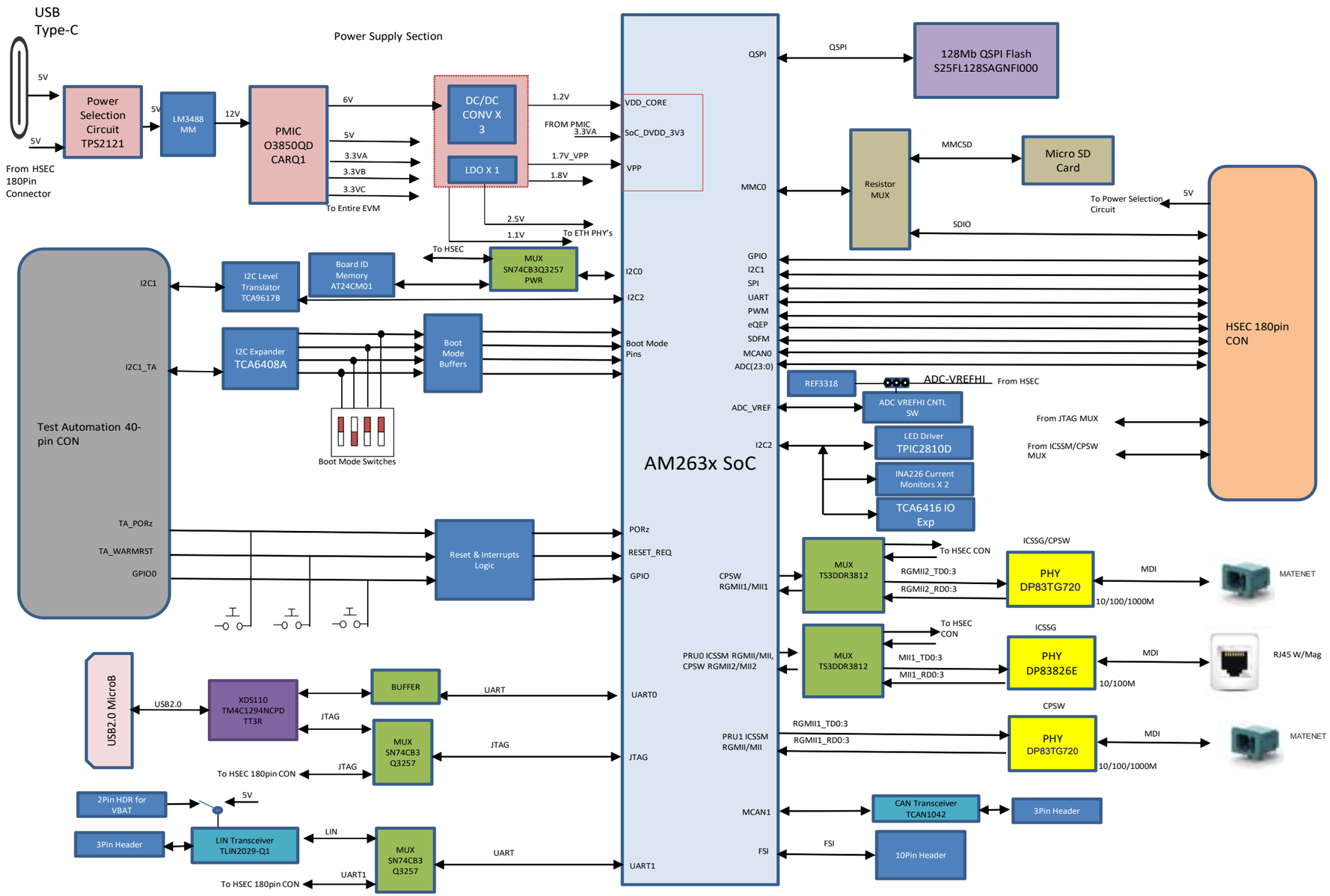
SYSTEM BLOCK DIAGRAM



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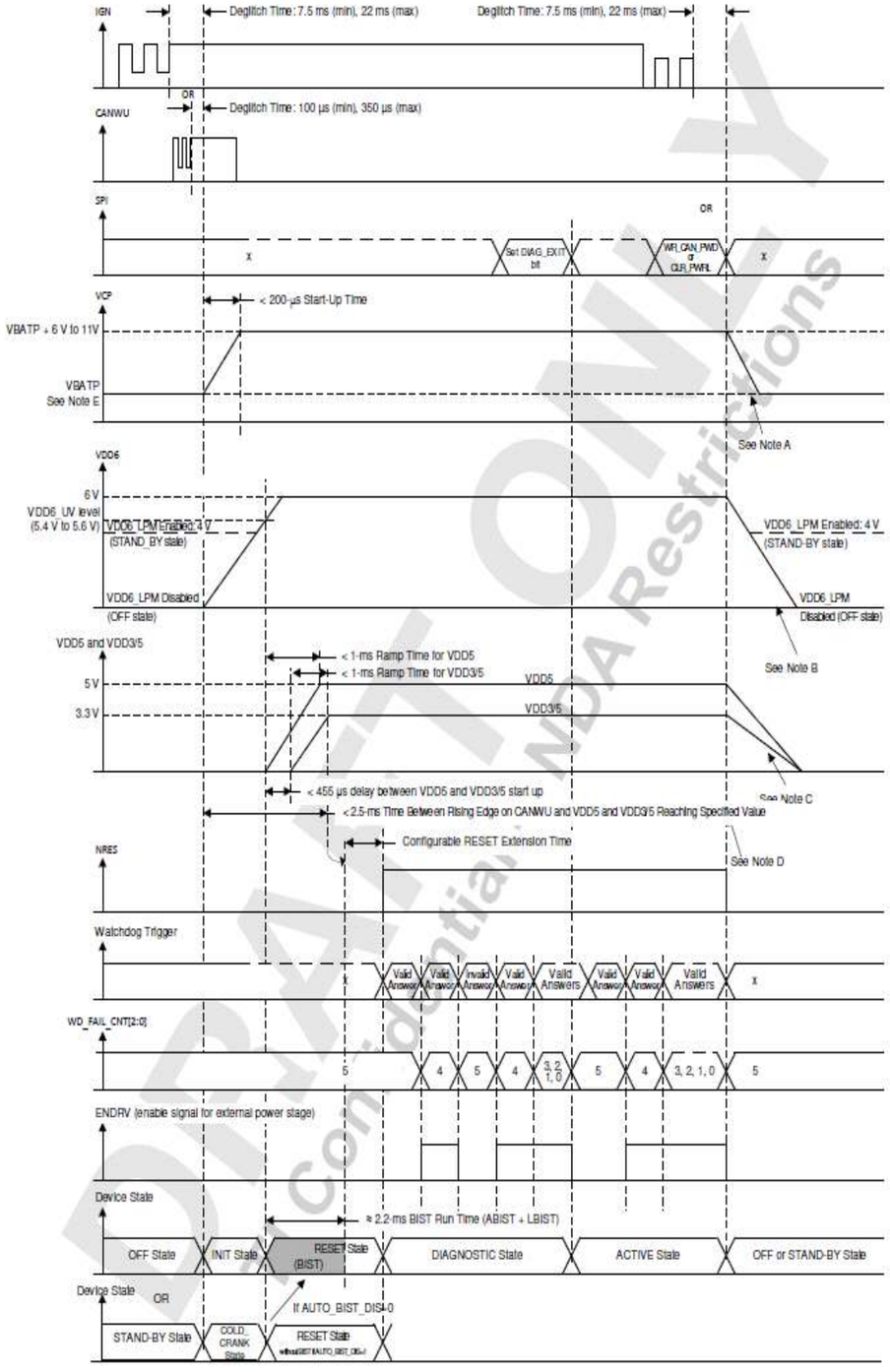
POWER SEQUENCE



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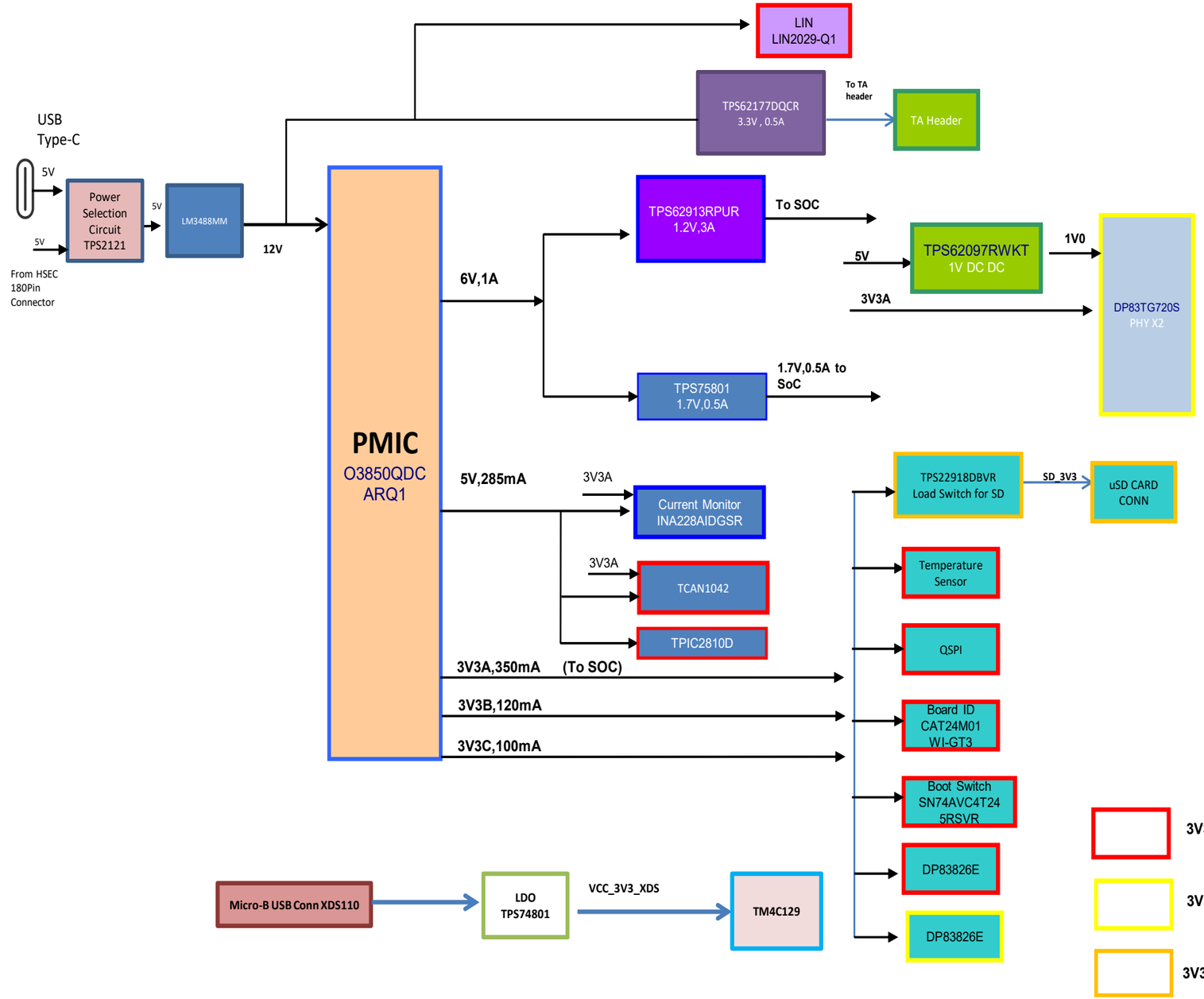
POWER FLOW DIAGRAM



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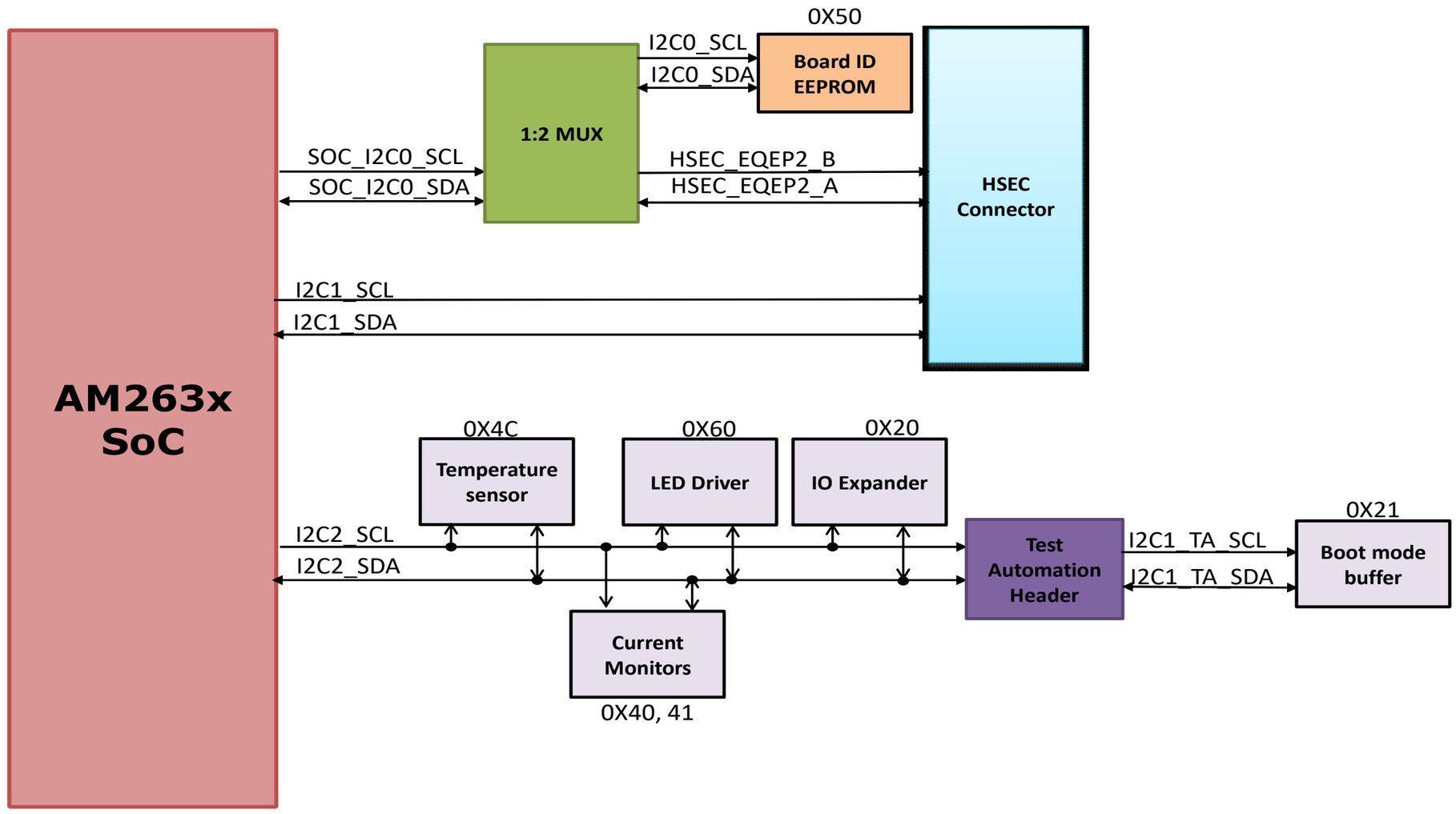
I2C TREE DIAGRAM



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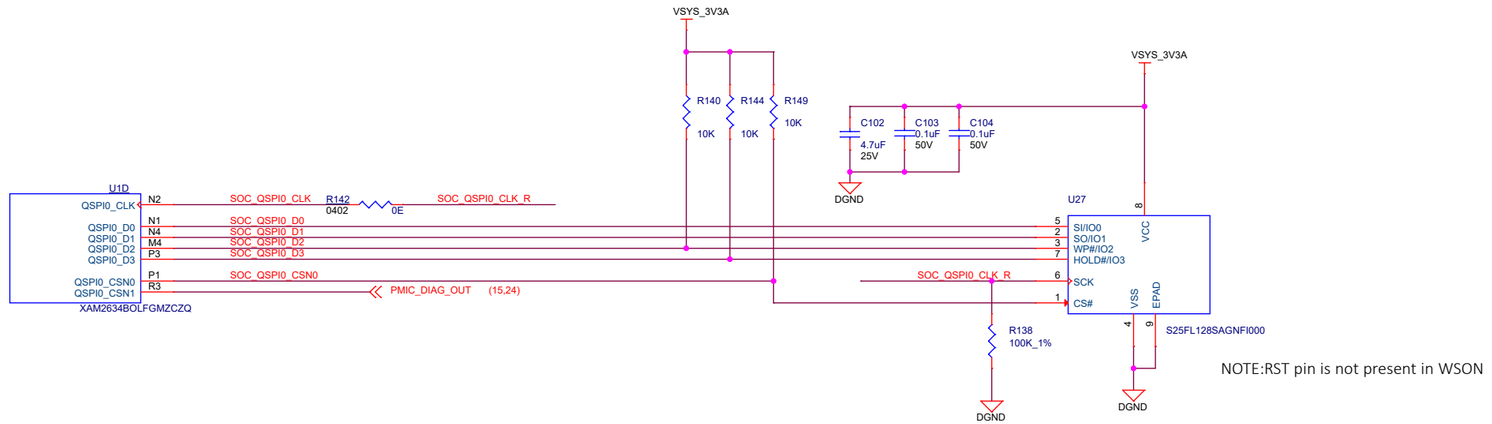
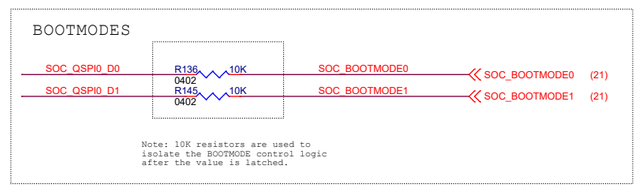
GPIO MAPPING TABLE

Sl No.	GPIO DESCRIPTION	GPIO	Pin Name	FUNCTIONALITY	Net Name	ACTIVE STATE
1	Interupt To SoC	GPIO21	LIN2_RXD	Interrupt	SOC_INTn	LOW
2	Interupt To DP83826E	GPIO66	EPWM12_A	Interrupt	ICSSM2_PWDN/INTn	LOW
3	Interupt To DP83869_01	GPIO67	EPWM11_B	Interrupt	RGMII1_INT	LOW
4	Interupt To DP83869_02	GPIO68	EPWM12_B	Interrupt	ICSSM1_INT	LOW
5	User Defined LED	GPIO20	LIN2_TXD	GPIO	USER_LED0	PREFERABLE
6	PMIC DIAG OUT to SOC	GPIO1	QSPI0_CSn1	GPIO	PMIC_DIAG_OUT	LOW
IO Expander 01						
7	Standby input to CAN tranciever		P00	GPIO	MCAN1_STB	High
8	Enable control to clock buffer		P01	Enable	CLK_BUF_EN	High
9	Select line for ICSSM Mux 1		P02	Mux Selection	ICSSM1_MUX_SEL	PREFERABLE
10	Select line for ICSSM Mux 2		P03	Mux Selection	ICSSM2_MUX_SEL	PREFERABLE
11	Reset input to DT_01		P04	Reset	GPIO_RGMII1_RST	LOW
12	Reset input to DP83869_02		P05	Reset	GPIO_ICSSM1_RST	LOW
13	Reset input to DP83826E		P06	Reset	GPIO_ICSSM2_RST	LOW
14	Enable control to SD load switch		P07	Load SW Enable	GPIO_uSD_PWR_EN	High
15	User Defined LED		P10	GPIO	USER_LED1	PREFERABLE
16	Select line for I2C0 MUX		P11	Mux Selection	I2C0_MUX_SEL	PREFERABLE
17	Select line for SPI1 MUX		P12	Mux Selection	SPI1_MUX_SEL	PREFERABLE
18	Enable control to 1.7V LDO		P13	LDO Enable	VPP_LDO_EN	PREFERABLE
19	Select line for MDIO/MDC MUX		P14	Mux Selection	MDIO/MDC_MUX_SEL	PREFERABLE
20	Select line for LIN/UART MUX		P15	Mux Selection	LIN_MUX_SEL	PREFERABLE
21	Select line for ADC MUX		P16	Mux Selection	ADC1_MUX_SEL	PREFERABLE
22	Select line for ADC MUX		P17	Mux Selection	ADC2_MUX_SEL	PREFERABLE

SOC- QSPI Interface





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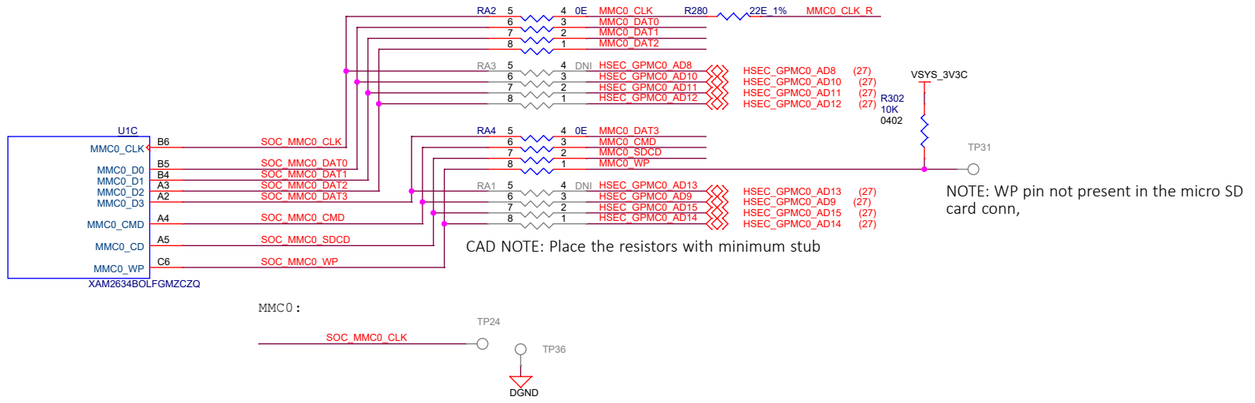
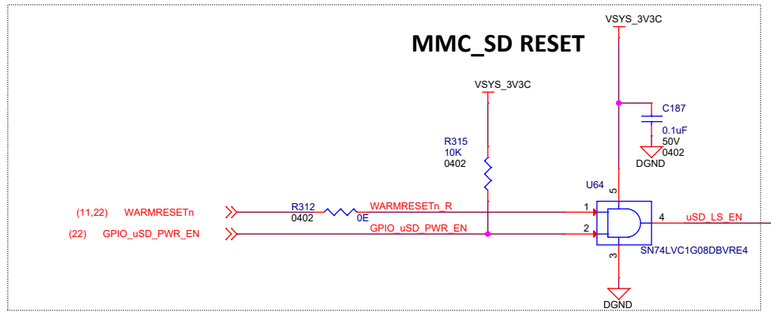
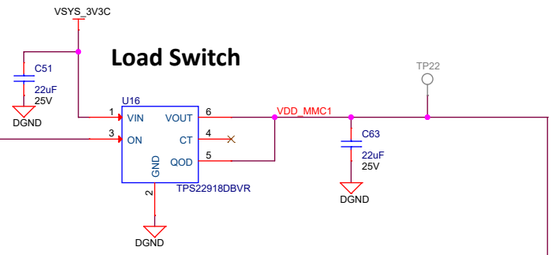
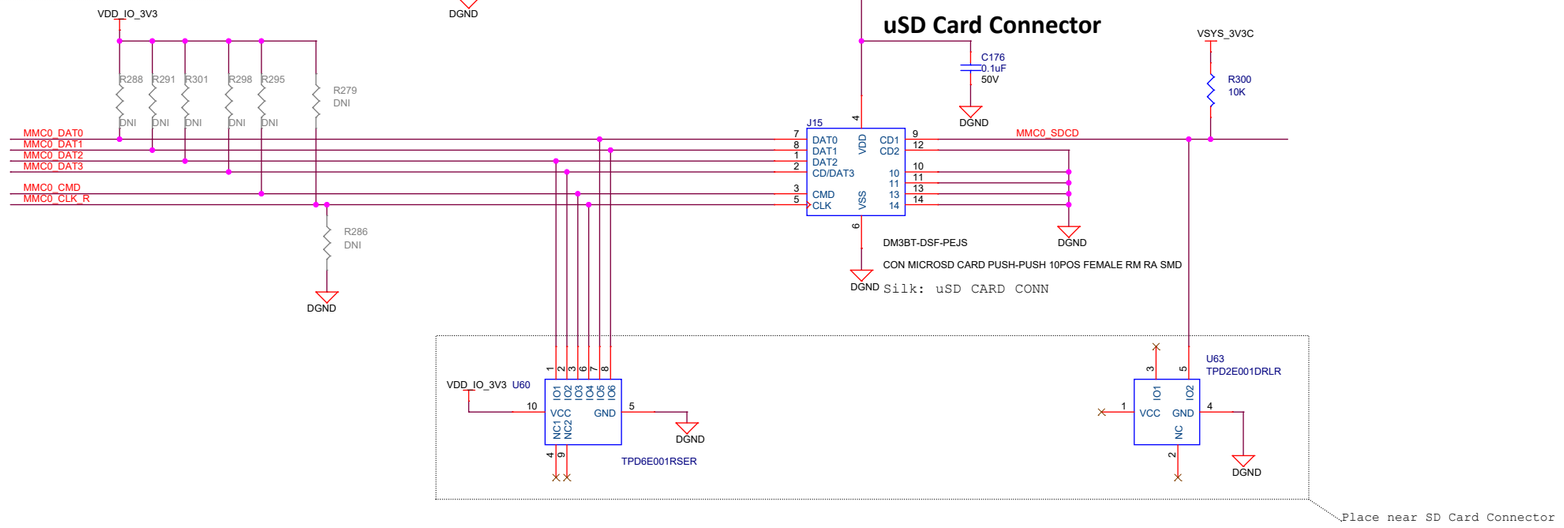
SOC- MMC0 Interface









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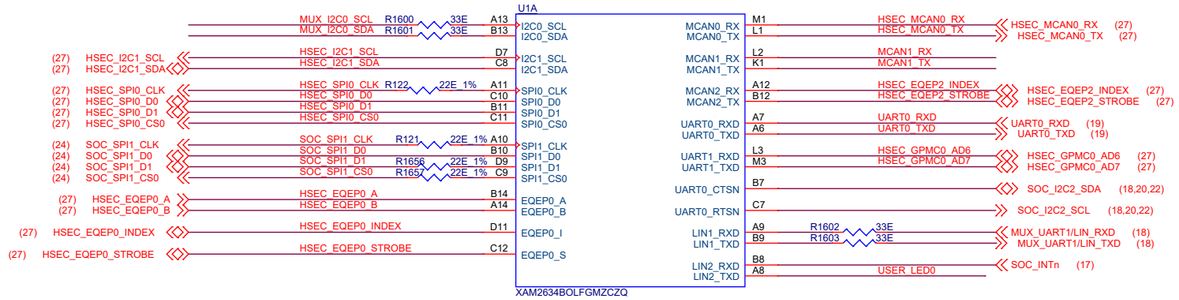
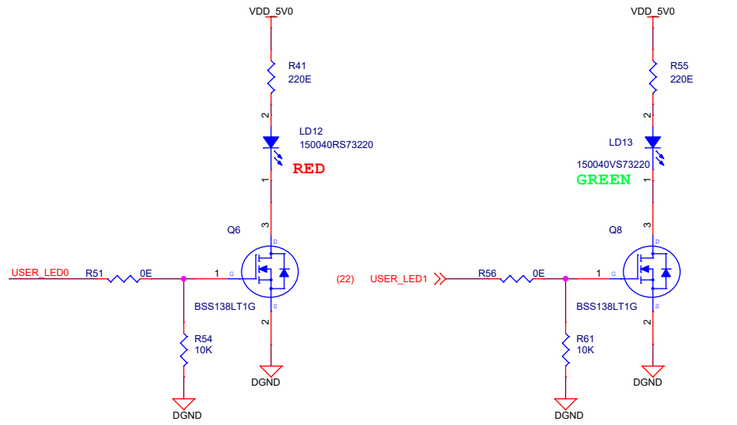
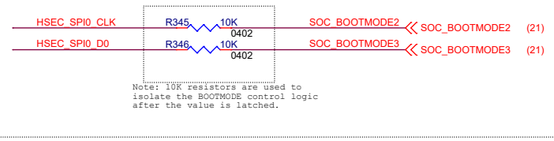
SOC-IO Interfaces



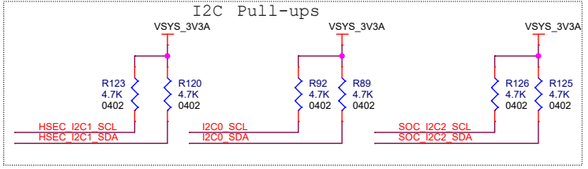
USER LED



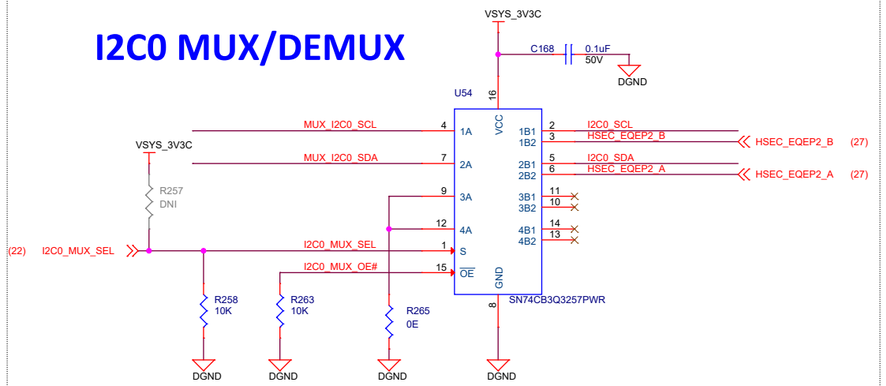
BOOTMODES



I2C Pull-ups



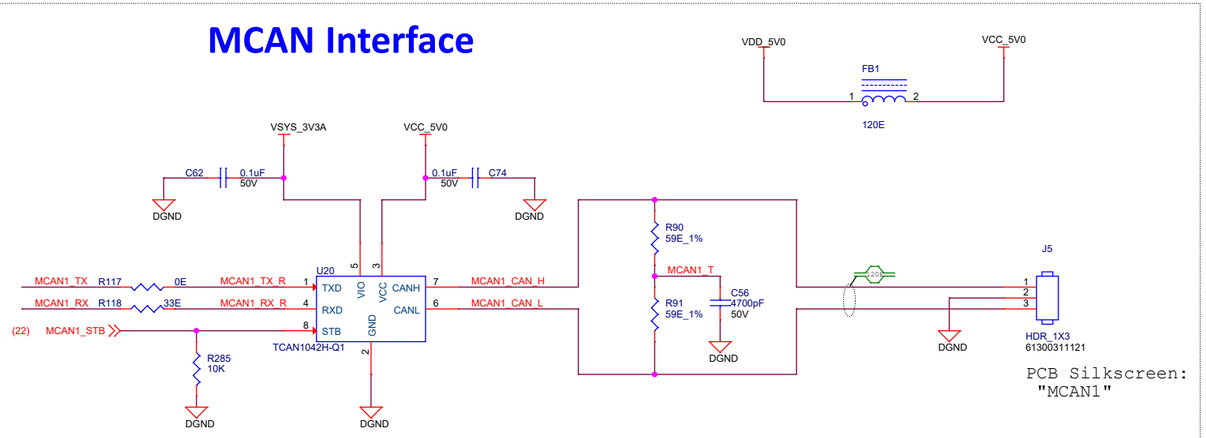
I2C0 MUX/DEMUX



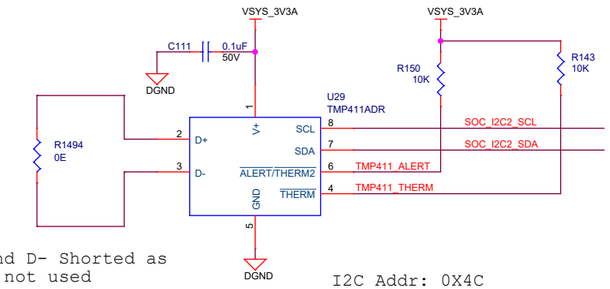
I2C0 - 1:2 MUX

SEL	CONDITION	FUNCTION
LOW	I2C0 SELECTED	A-->B1 port
HIGH	HSEC EQEP selected	A-->B2 port

MCAN Interface



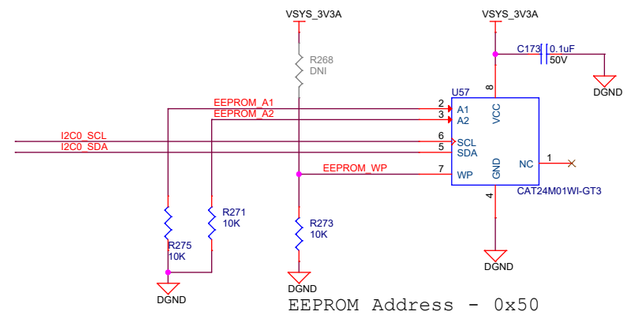
Temperature Sensor



Note: D+ and D- Shorted as TEMPCAL is not used

I2C Addr: 0X4C
PCB Note: Place Close To SOC

Board ID EEPROM



EEPROM Address - 0x50

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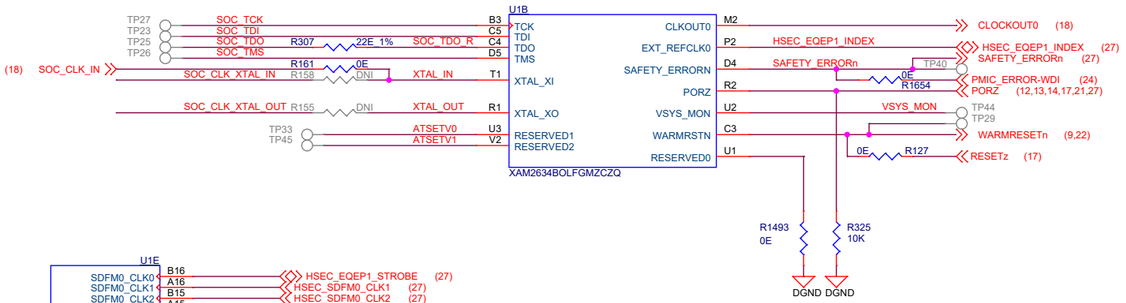
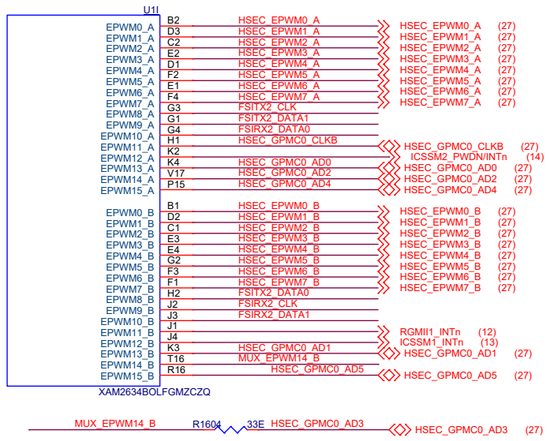
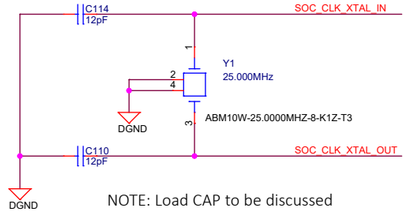
SOC JTAG, RESET and CLKS



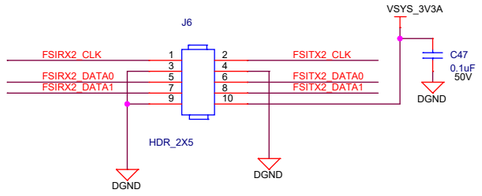


SOC Clock

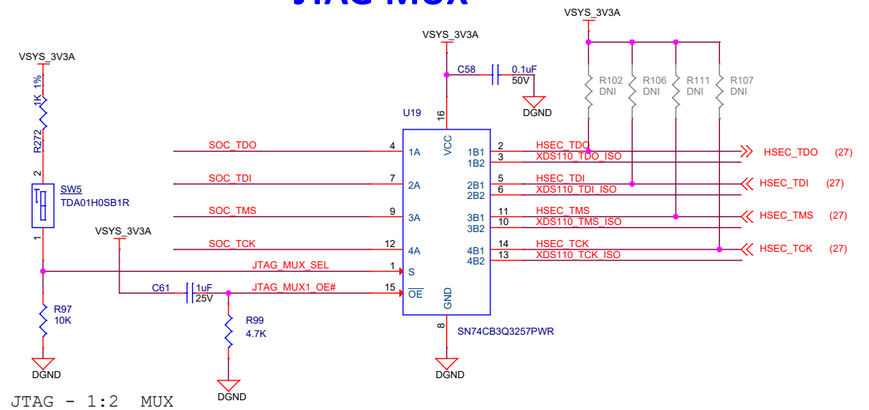


NOTE: Load CAP to be discussed

FSI Header



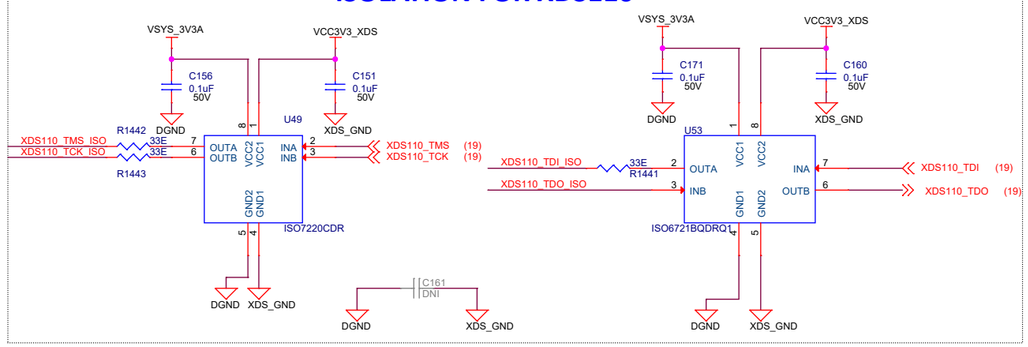
JTAG MUX



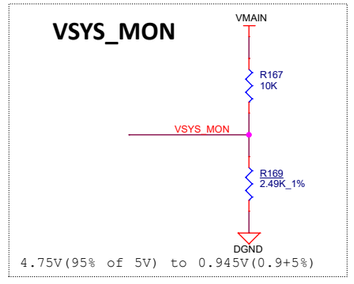
JTAG - 1:2 MUX

SW1.1	CONDITION	FUNCTION
LOW	HSEC EMU selected	A-->B1 port [ON Board EMU]
HIGH	XDS110 selected	A-->B2 port [EXTERNAL EMU]

ISOLATION FOR XDS110

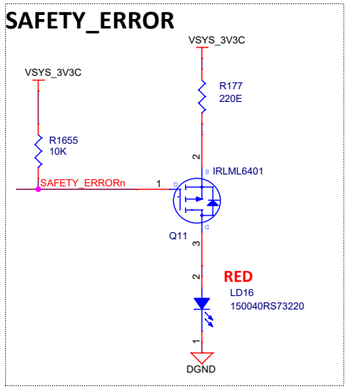


VSYS_MON



4.75V(95% of 5V) to 0.945V(0.9+5%)

SAFETY_ERROR



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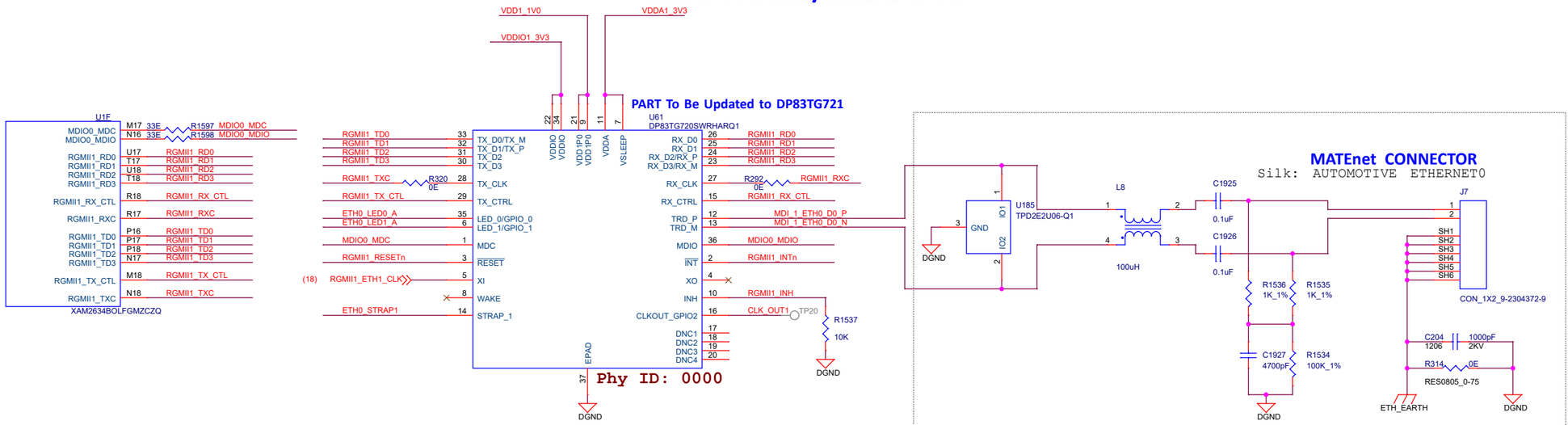
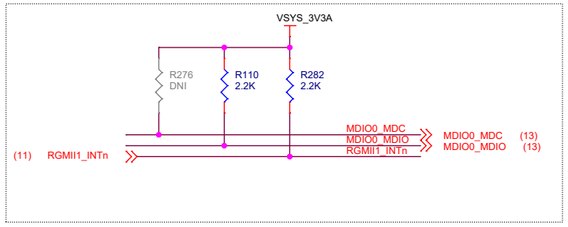
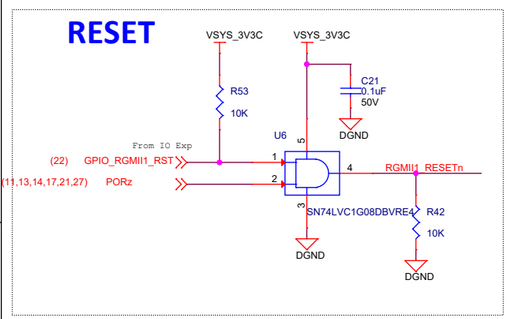
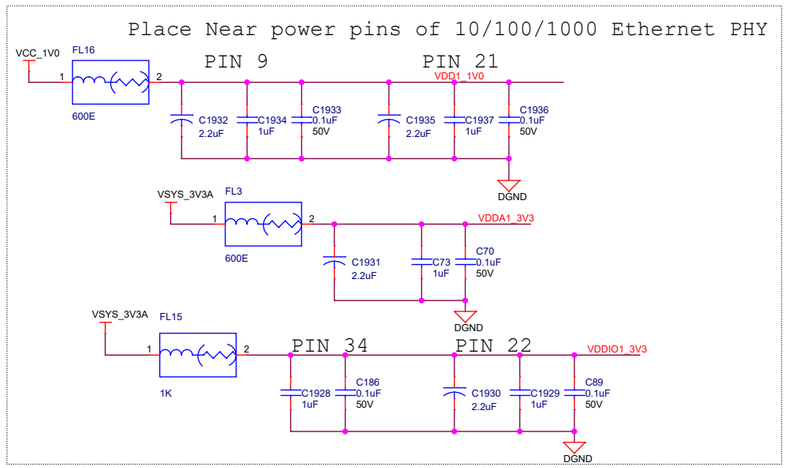
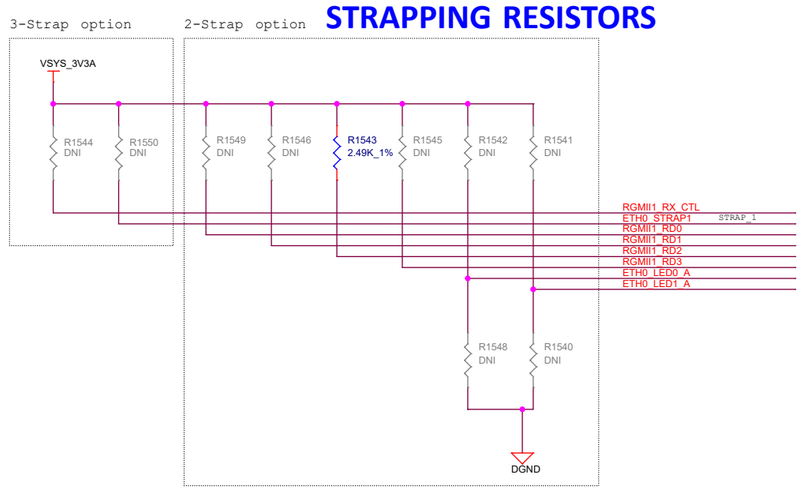
CPSW RGMII1/MII1 Ethernet

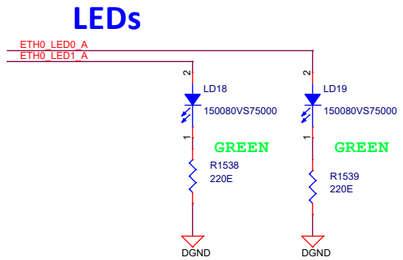












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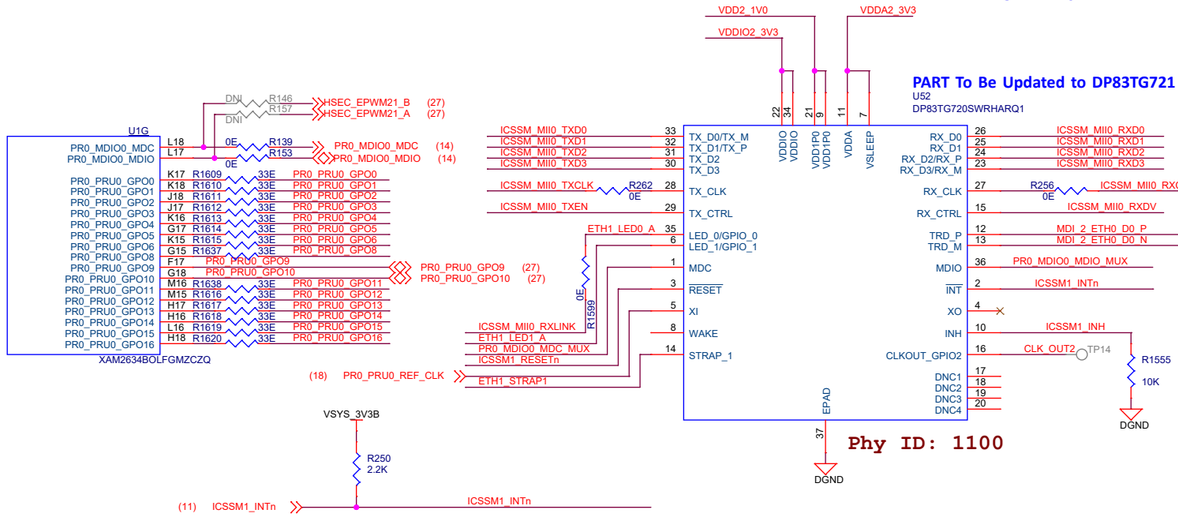
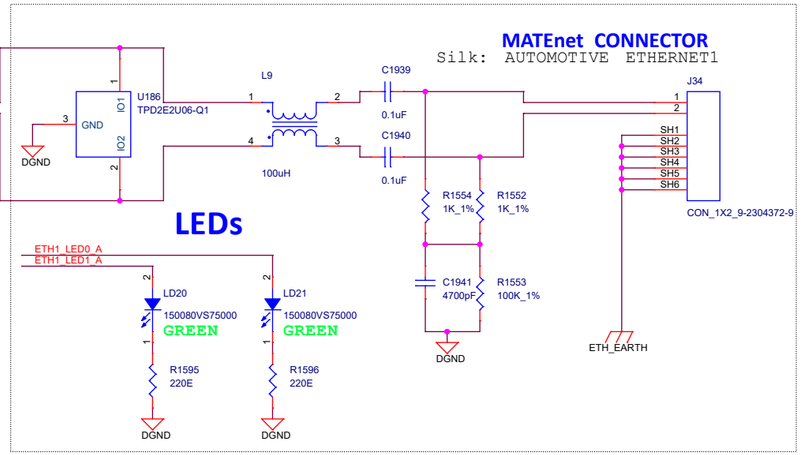
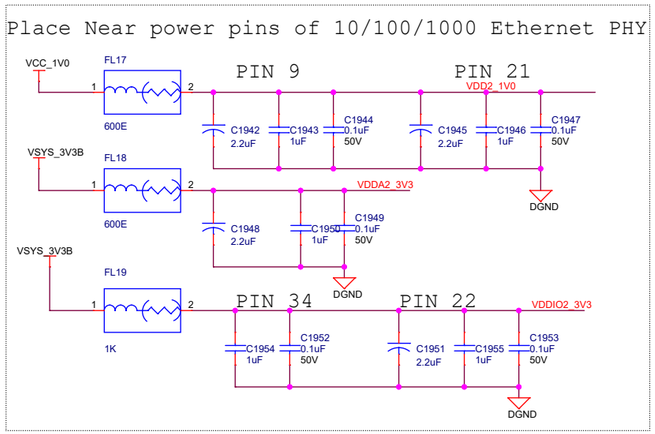
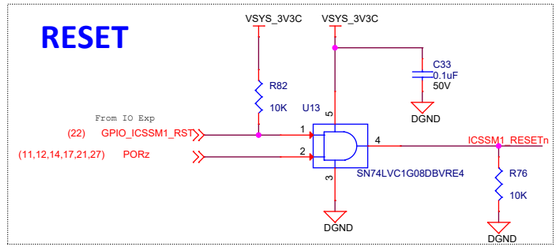
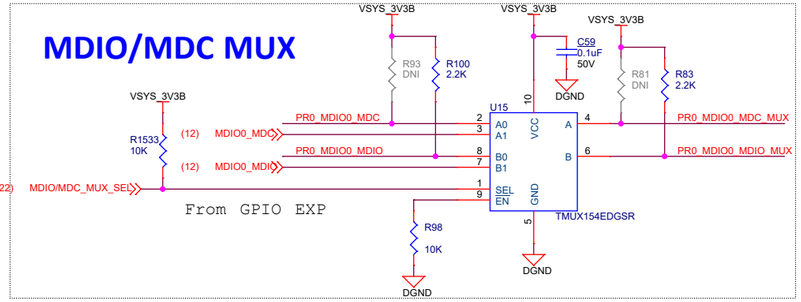
PRU0 ICSSM RGMII/MII, CPSW RGMII2/MII2 Ethernet



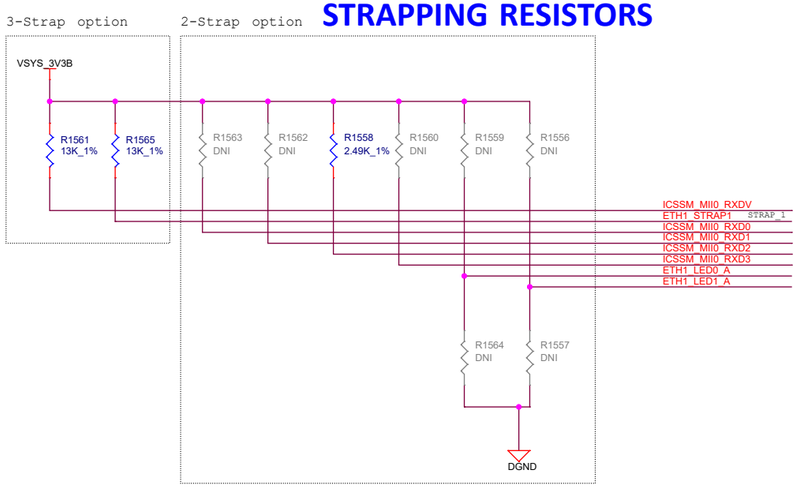






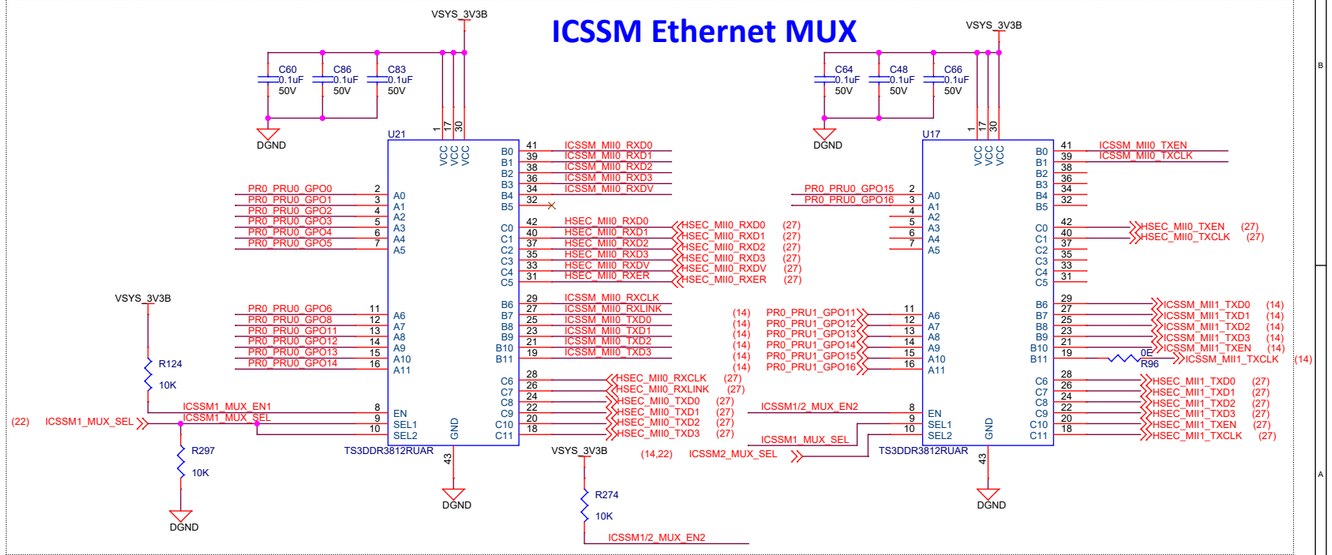


STRAPPING RESISTORS



PHY ADDRESS = 01100
MS = 0 Slave,AUTO = 0 Autonomous
RGMII (Align Mode)

ICSSM Ethernet MUX



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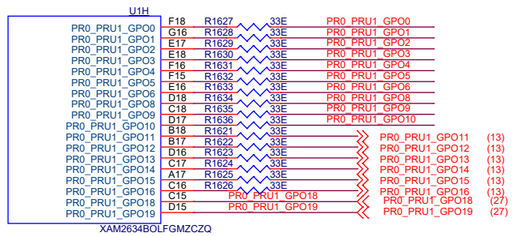
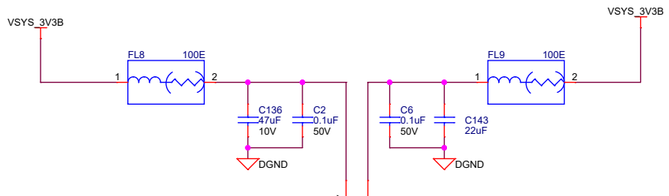
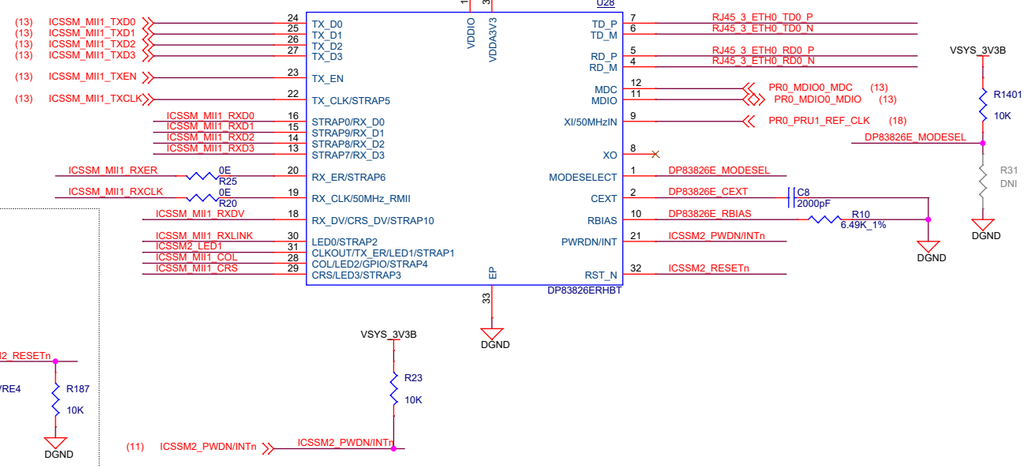
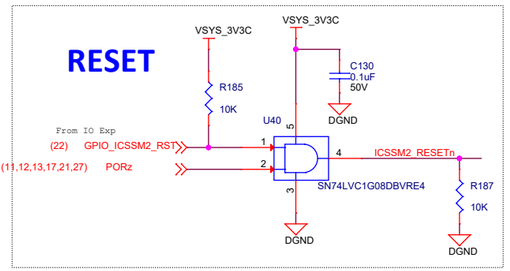
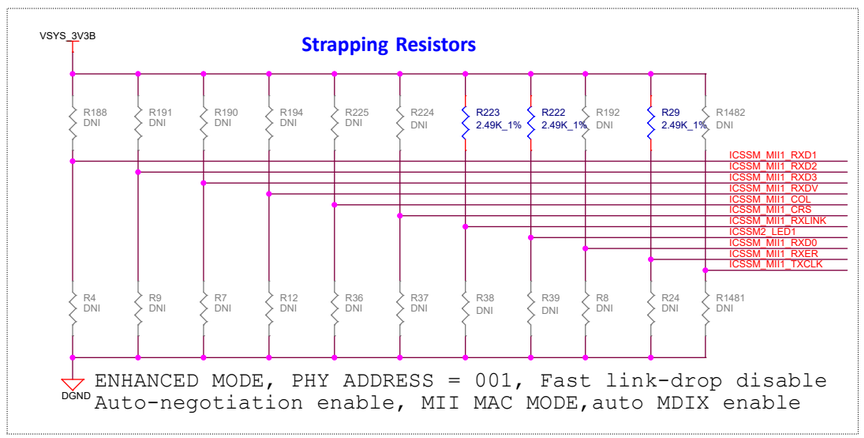
PRU1 ICSSM RGMII/MII Ethernet



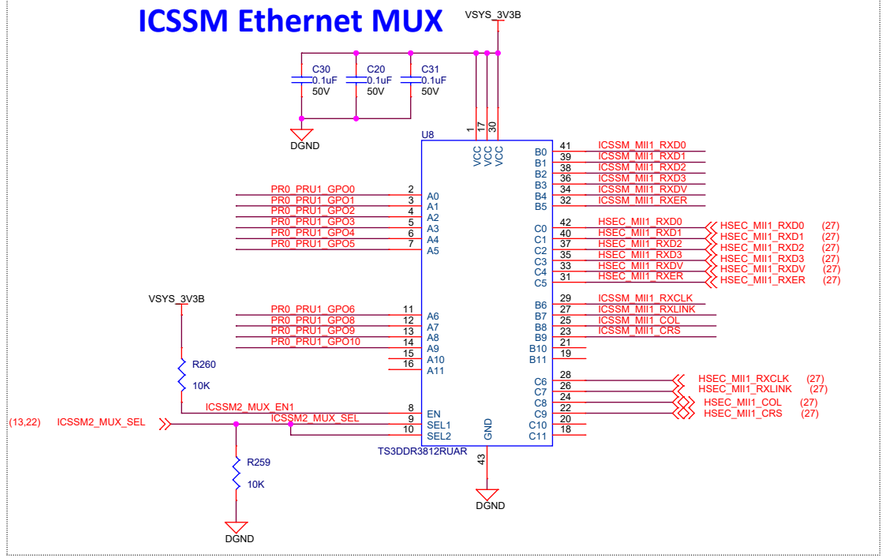




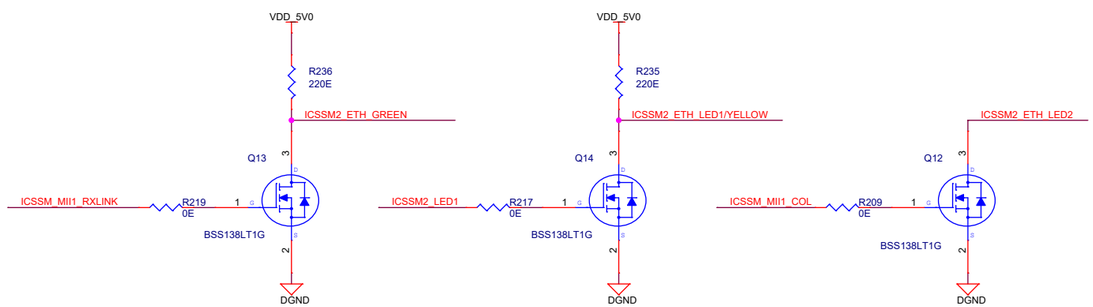




ICSSM Ethernet MUX



LED Driver MOSFETS



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Title	REVISION HISTORY	
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ADC and DAC Interfaces

VSYS_3V3C — FL4 — VDDA_IO_3V3

100E

CAD NOTE: Place the ESDs close to connector

VDDA_IO_3V3

U35, U36, U37, U38, U39, U34 — TPD4E001DBVR — DGND

C252 0.1uF, C253 0.1uF, C254 0.1uF

HSEC_ADC4_AIN0/ADC_CAL0 (27)
HSEC_ADC4_AIN1/ADC_CAL1 (27)
HSEC_ADC0_AIN0/DAC_OUT (27)
HSEC_ADC0_AIN1/DAC_OUT (27)

HSEC_ADC1_AIN2
HSEC_ADC1_AIN3
HSEC_ADC1_AIN4
HSEC_ADC1_AIN5

U1J — XAM2634BOLFGMZCZQ

ADC0_AIN0	V15	HSEC_ADC0_AIN0 (27)
ADC0_AIN1	U15	HSEC_ADC0_AIN1 (27)
ADC0_AIN2	T14	HSEC_ADC0_AIN2 (27)
ADC0_AIN3	U14	HSEC_ADC0_AIN3 (27)
ADC0_AIN4	U13	HSEC_ADC0_AIN4 (27)
ADC0_AIN5	R14	HSEC_ADC0_AIN5 (27)
ADC1_AIN0	T11	HSEC_ADC1_AIN0 (27)
ADC1_AIN1	U11	HSEC_ADC1_AIN1 (27)
ADC1_AIN2	T12	HSEC_ADC1_AIN2 (27)
ADC1_AIN3	V12	HSEC_ADC1_AIN3 (27)
ADC1_AIN4	U12	HSEC_ADC1_AIN4 (27)
ADC1_AIN5	R12	HSEC_ADC1_AIN5 (27)
ADC2_AIN0	R10	HSEC_ADC2_AIN0 (27)
ADC2_AIN1	T10	HSEC_ADC2_AIN1 (27)
ADC2_AIN2	U10	HSEC_ADC2_AIN2 (27)
ADC2_AIN3	T9	HSEC_ADC2_AIN3 (27)
ADC2_AIN4	V9	
ADC2_AIN5	T8	
ADC3_AIN0	U7	HSEC_ADC3_AIN0 (27)
ADC3_AIN1	U8	HSEC_ADC3_AIN1 (27)
ADC3_AIN2	T7	HSEC_ADC3_AIN2 (27)
ADC3_AIN3	R7	HSEC_ADC3_AIN3 (27)
ADC3_AIN4	V8	HSEC_ADC3_AIN4 (27)
ADC3_AIN5	U9	HSEC_ADC3_AIN5 (27)
ADC4_AIN0	U6	HSEC_ADC4_AIN0 (27)
ADC4_AIN1	V5	HSEC_ADC4_AIN1 (27)
ADC4_AIN2	V4	PMIC_DIAG_OUT (8,24)
ADC4_AIN3	U5	
ADC4_AIN4	V3	
ADC4_AIN5	U4	
ADC_CAL0	U16	ADC_CAL0
ADC_CAL1	T15	ADC_CAL1
ADC_VREFHI_G0	V14	
ADC_VREFHI_G1	V10	
ADC_VREFHI_G2	V6	
ADC_VREFLO_G0	V13	AM263_ADC_VREFLO_1
ADC_VREFLO_G1	V11	AM263_ADC_VREFLO_2
ADC_VREFLO_G2	V7	
DAC_OUT	T5	
DAC_VREF0	T13	
DAC_VREF1	T6	

R181 1K 1%, R171 1K 1%

R1425 1K 1%, R329 1K 1%, R333 1K 1%

DIAG_OUT - PMIC Analog/Digital Diagnostic Output to MCU

ADC_CAL0 (27), ADC_CAL1 (27)

HSEC_ADC3_AIN4
HSEC_ADC3_AIN5
HSEC_ADC4_AIN0/ADC_CAL0
HSEC_ADC4_AIN1/ADC_CAL1
HSEC_ADC2_AIN2
HSEC_ADC2_AIN3

HSEC_DAC_OUT (27)

R168 0E, R175 0E

AM263_DAC_VREF0

C125 4.7uF, C121 0.1uF

DGND DGND

DGNDGNDGNDGNDGNDGNDGNDGNDGNDGNDGNDGNDGNDGNDGNDGNDGNDGNDGNDGNDGNDGND

CAD NOTE: Place the CAPs close to connector

C278 DNI, C276 DNI, C271 DNI, C270 DNI, C285 DNI, C282 DNI, C269 DNI, C268 DNI, C281 DNI, C280 DNI, C267 DNI, C266 DNI, C276 DNI, C275 DNI, C265 DNI, C264 DNI, C284 DNI, C277 DNI, C283 DNI, C262 DNI

C1659 DNI, C1660 DNI, C1661 DNI, C1662 DNI

DGND

C258 4.7uF, C257 0.1uF, C288 0.1uF, C273 4.7uF, C272 0.1uF

AM263_ADC_VREFLO_2
AM263_ADC_VREFLO_1

CAD NOTE: - Place decoupling at BGA between VREF and GND
Place GND short as close as possible to BGA and decoupling

R178 DNI ADC_VREFHI_G0_G1
R159 DNI ADC_VREFHI_G2

ADC_VREFHI_G0_G1_R
ADC_VREFHI_G2_R

ADC_VREF1

VDDA_IO_3V3, C93 0.1uF, DGND

U24A — OPA4350EA/250

ADC_DAC_VREF

SW7 — CAS-D20TA

ADC_VREFHI_G2
ADC_VREF2

SILK "ADC VREF"

U24B — OPA4350EA/250

ADC_DAC_VREF

U24D — OPA4350EA/250

REF Voltage Generation

VDDA_IO_3V3

U22 — REF3318AIDBZT

C75 2.2uF, C72 0.1uF, C71 0.1uF

REF3318_ADC_DAC_REF

TP28

DGND

HSEC_ADC-VREFHI

SW8 — CAS-120TA

ADC_DAC-VREF

SILK "VREF"

REF VOLTAGE SELECTION

SW POSITION	SUPPLY SELECTION
PIN 1-2	ON BOARD REF IS SELECTED
PIN 2-3	HSEC SUPPLY IS SELECTED

VDDA_IO_1V8

U24C — OPA4350EA/250

AM263_DAC_VREF

SW6 — CAS-120TA

AM263_DAC_VREF0

SILK "DAC VREF"

DAC REF VOLTAGE SELECTION

SW POSITION	SUPPLY SELECTION
PIN 1-2	Allows AM263x on-die LDO reference (Routed n PCB)
PIN 2-3	selects output of VREF switch

ADC REF VOLTAGE SELECTION

SW POSITION	SUPPLY SELECTION
PIN 1-2	OPEN - Allows AM263x on-die LDO reference (routed on-die)
PIN 2-3	selects output of VREF switch
PIN 4-5	OPEN - Allows AM263x on-die LDO reference (routed on-die)
PIN 5-6	selects output of VREF switch

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TEXAS INSTRUMENTS — MISTRAL

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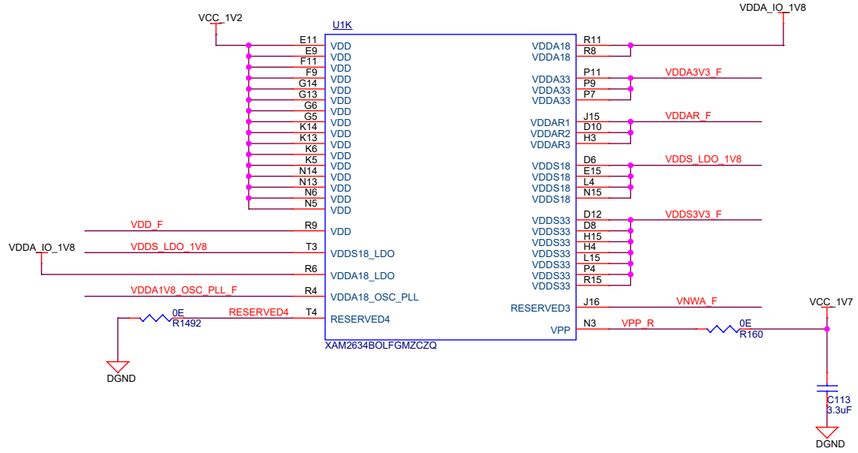
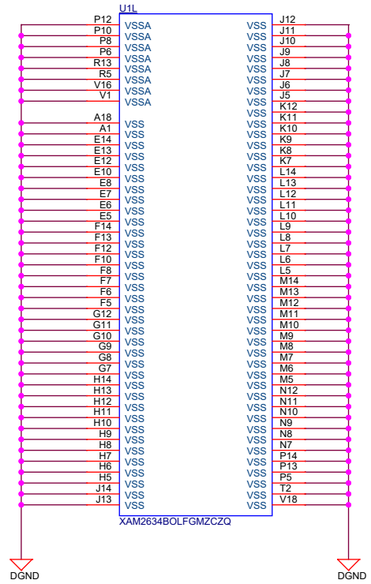
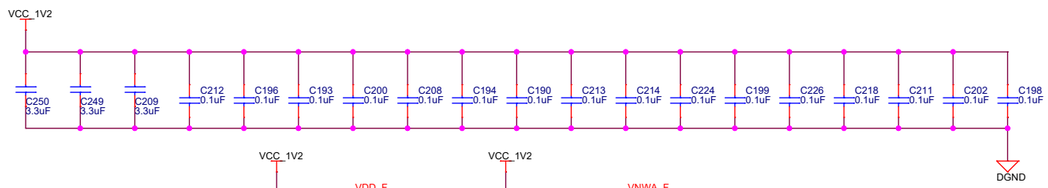
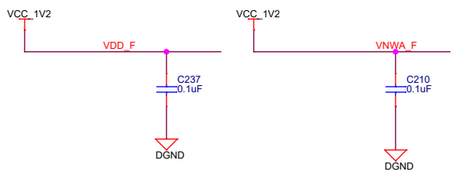
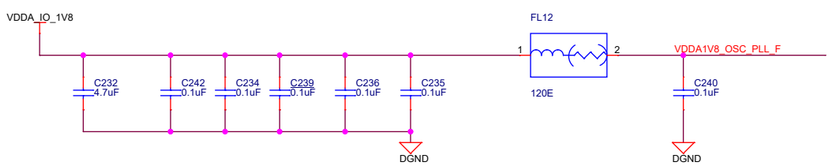
SOC-POWER and GND

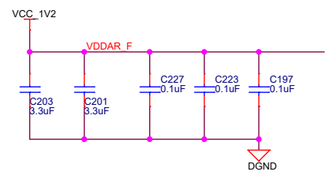


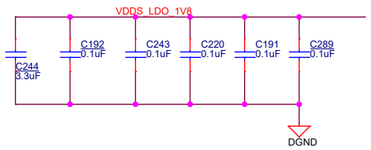


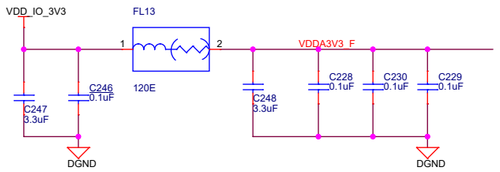


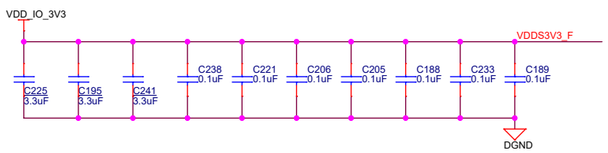












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Title	REVISION HISTORY	
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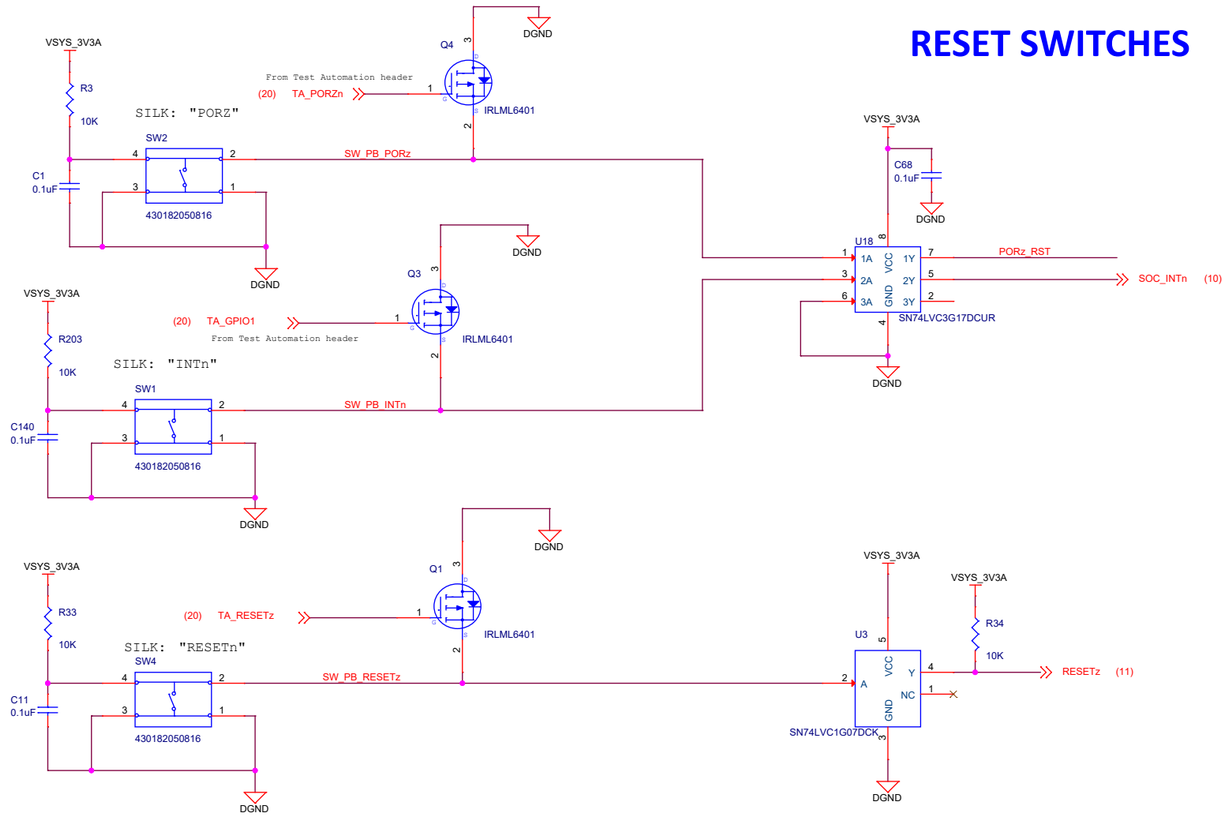
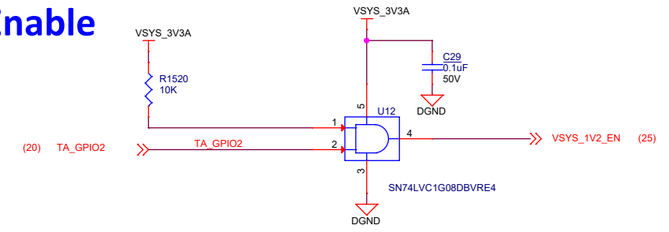
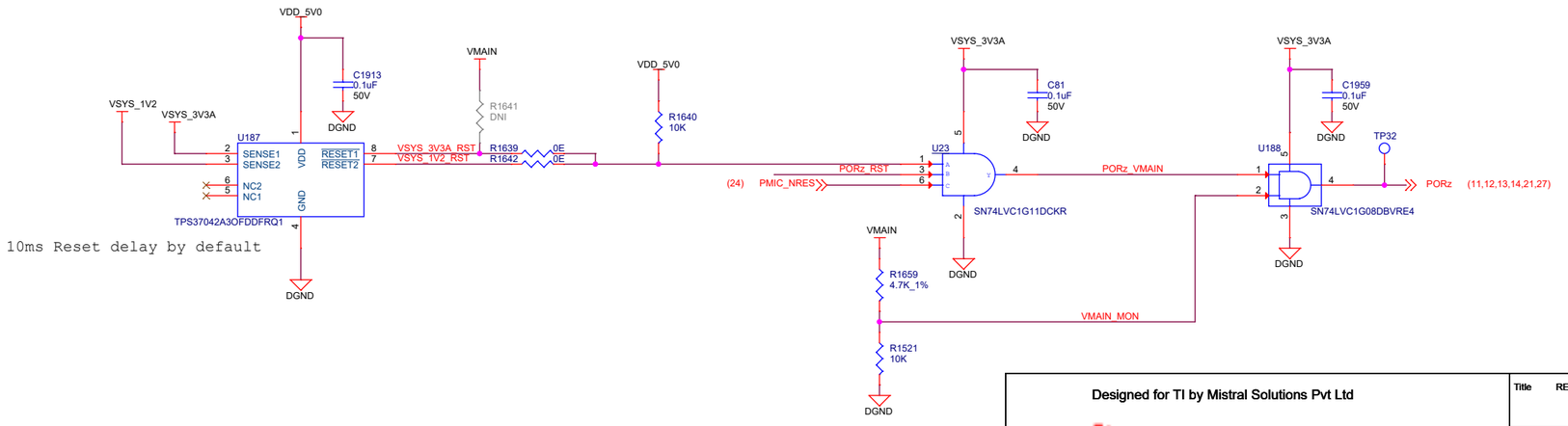
RESET SWITCHES



1.2V Enable



PORz



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Title	REVISION HISTORY	
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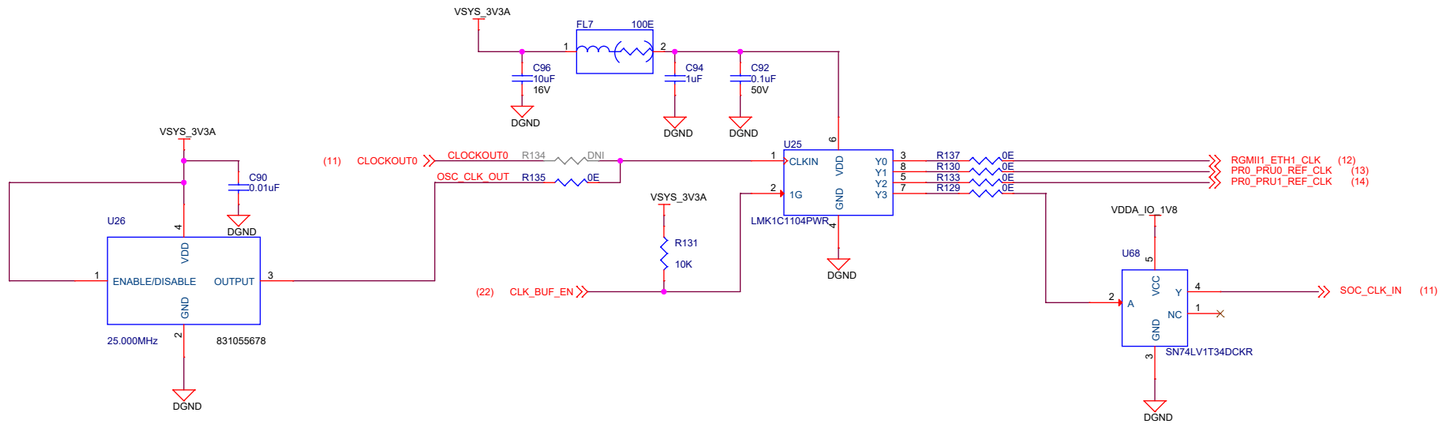
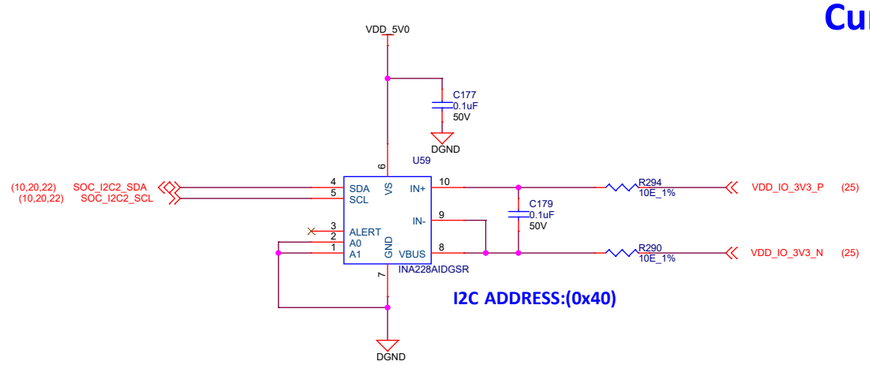
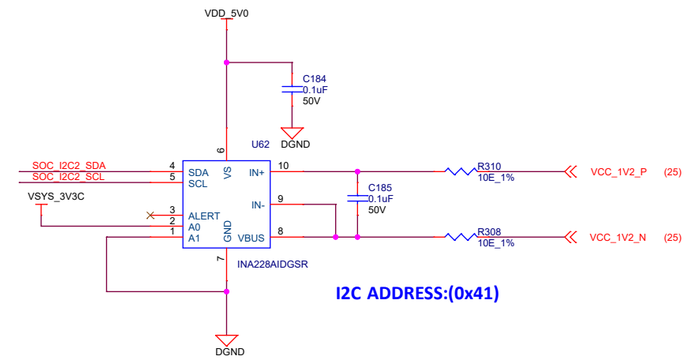
CLOCKS

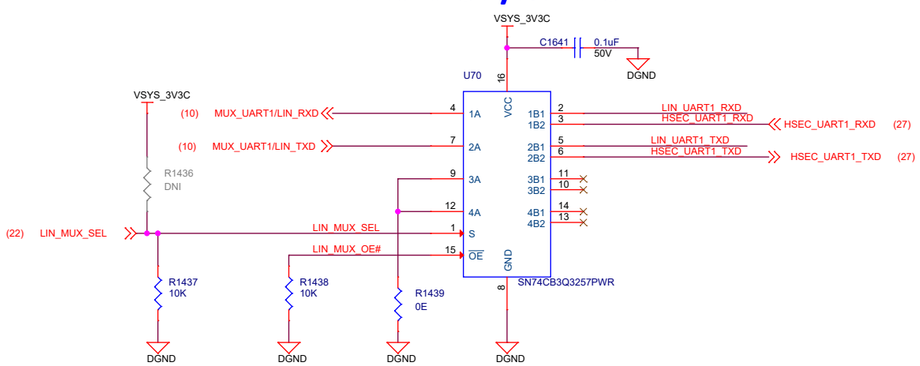


Current Monitors





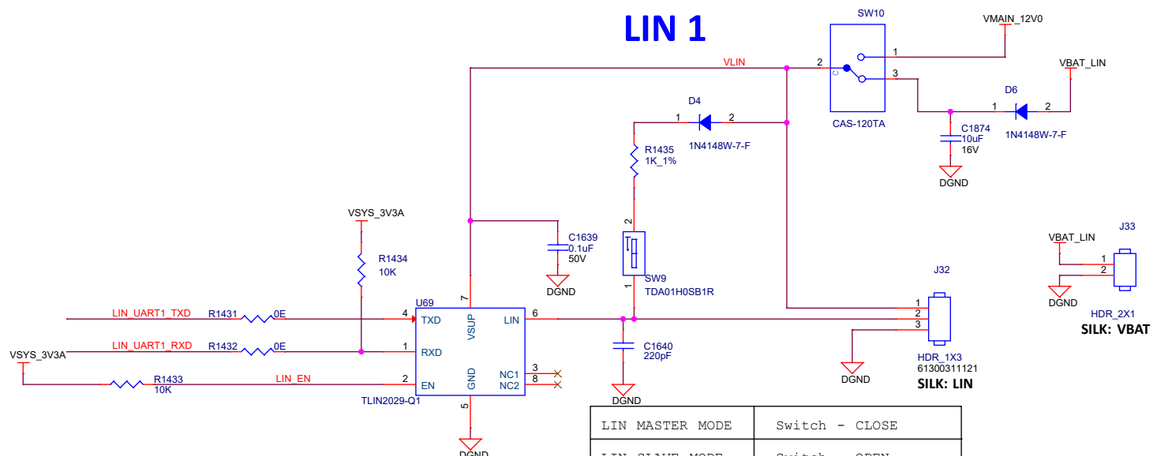
LIN MUX/DEMUX



I2C0 - 1:2 MUX

SEL	CONDITION	FUNCTION
LOW	LIN SELECTED	A-->B1 port
HIGH	HSEC UART selected	A-->B2 port

LIN 1



LIN MASTER MODE	Switch - CLOSE
LIN SLAVE MODE	Switch - OPEN

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Title REVISION HISTORY

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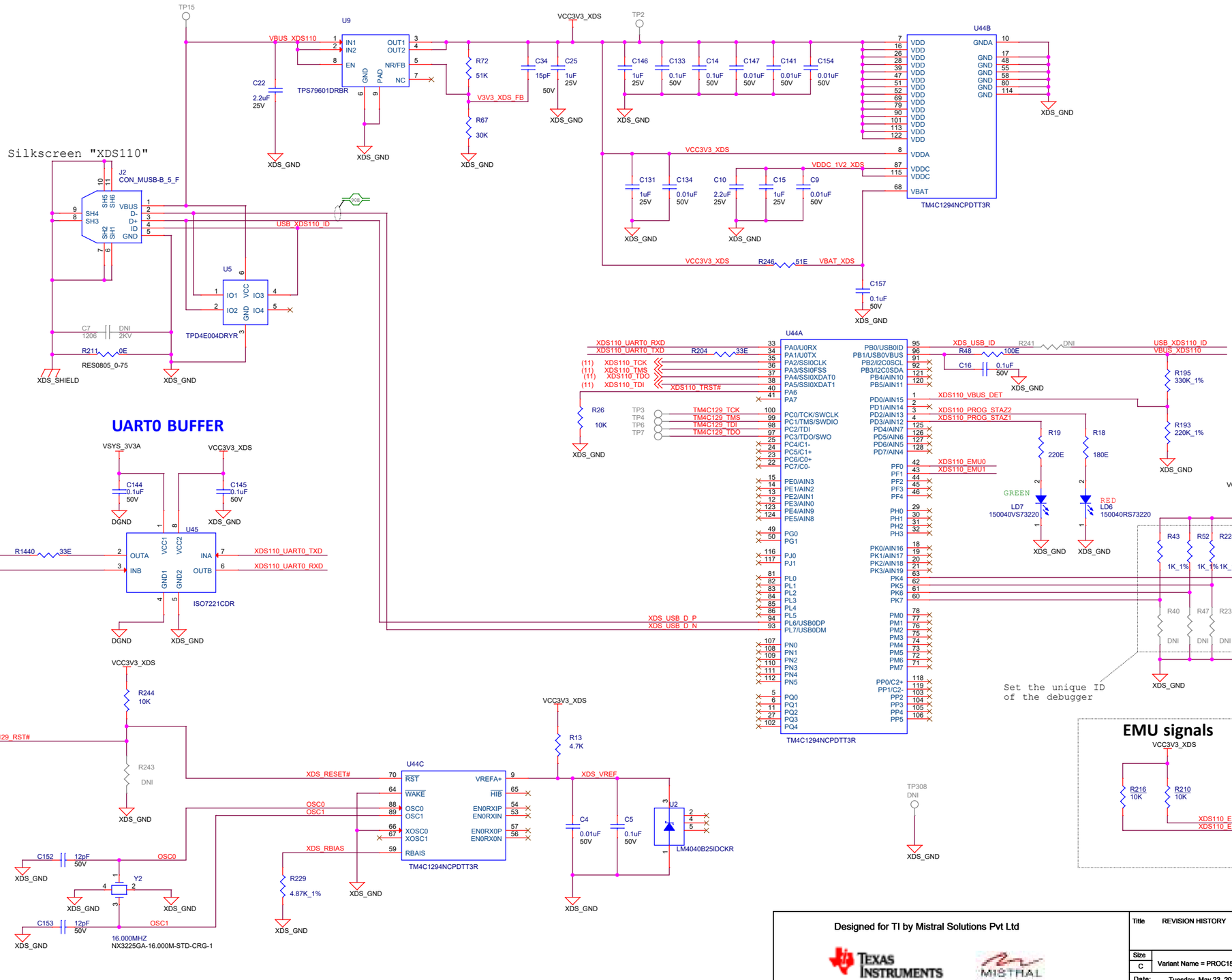
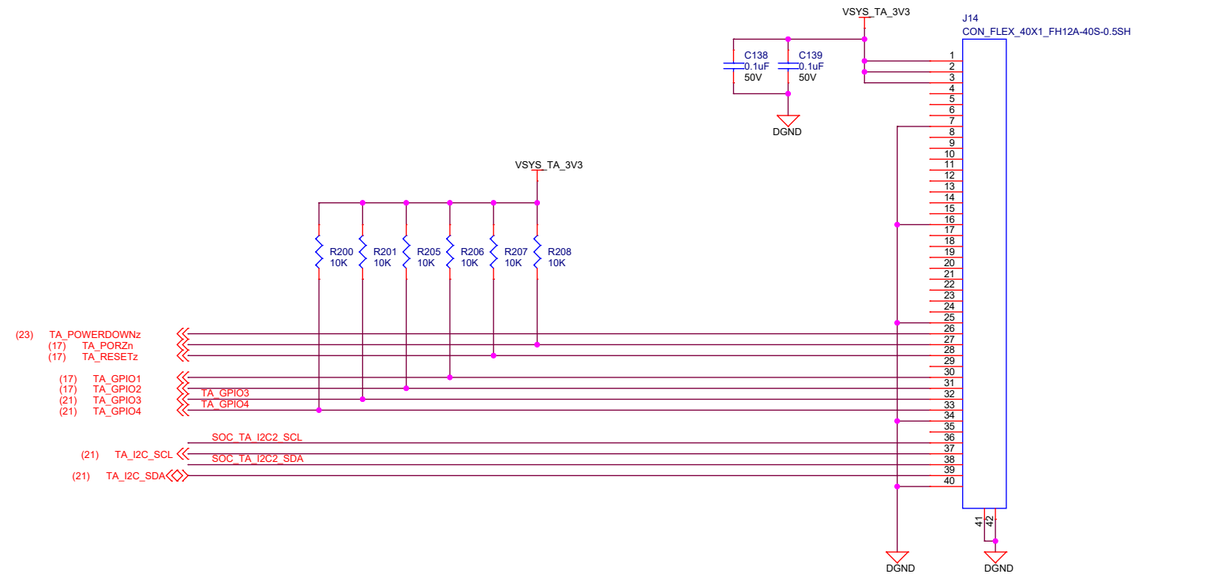
XDS110 DEBUGGER

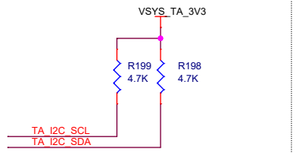


TEST AUTOMATION HEADER

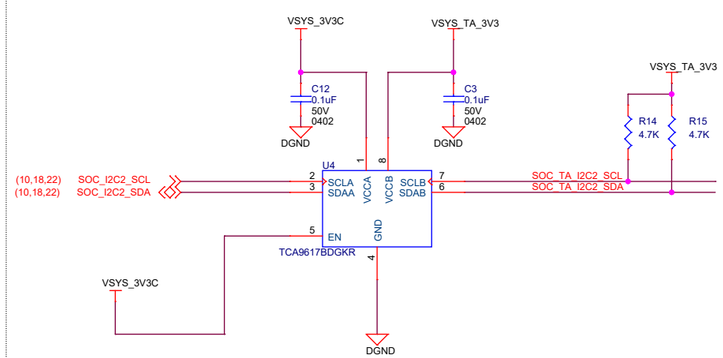
AUTOMATION INTERFACE
Cable : Parlex-050R40-76B, .5mm 3"



I2C Pull Ups



I2C BUFFER



TEST AUTOMATION GPIO MAPPING

SIGNAL NAME	DESCRIPTION	Direction WRT CTRL	Internal/ External PU/PD states
TA_POWERDOWN	Used to Power down the system	OUTPUT	External Pullup
TA_PORZn	Used to Reset the SoC PORz	OUTPUT	External Pullup
TA_RESETz	SoC Warmreset	OUTPUT	External Pullup
TA_GPIO1	Interrupt to SOC	OUTPUT	External Pullup
TA_GPIO2	Used to Enable or Disable 1.2V Regulator	OUTPUT	External Pullup
TA_GPIO3	Used to Enable the BOOTMODE Buffer	OUTPUT	External Pullup
TA_GPIO4	Used Reset Bootmode IO Exp	OUTPUT	External Pullup

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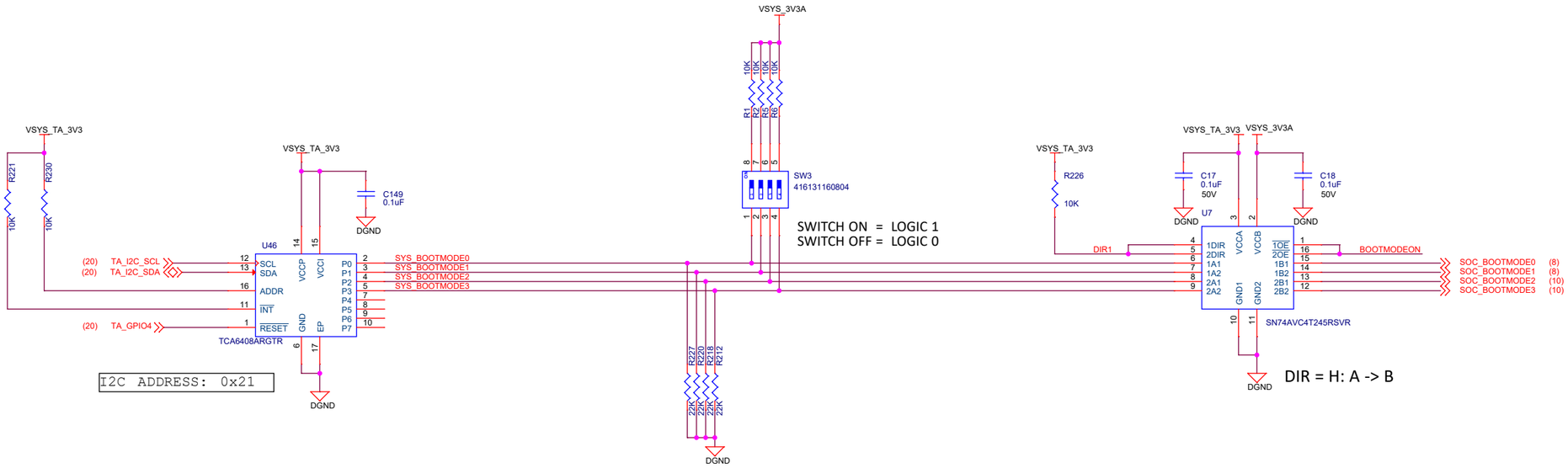
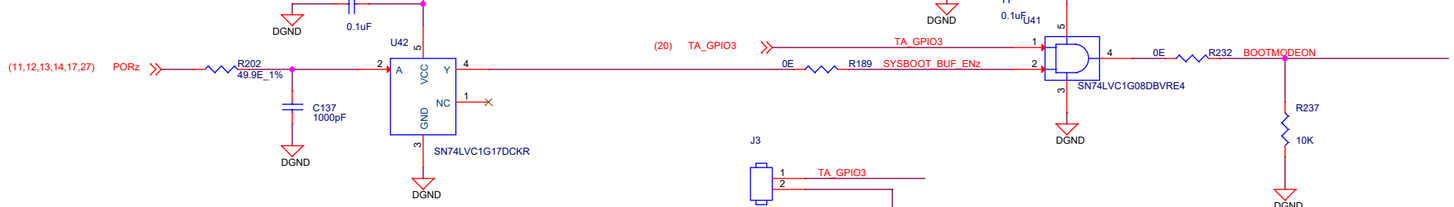
BOOTMODE BUFFER AND SWITCH





PORZ	TA_GPIO3	BOOTMODE Control from Test Automation HDR
HIGH	LOW	Enabled
HIGH	HIGH	Disabled

SH-J1

DNI

SH-J1 Shall be mounted to enable the bootmode buffer

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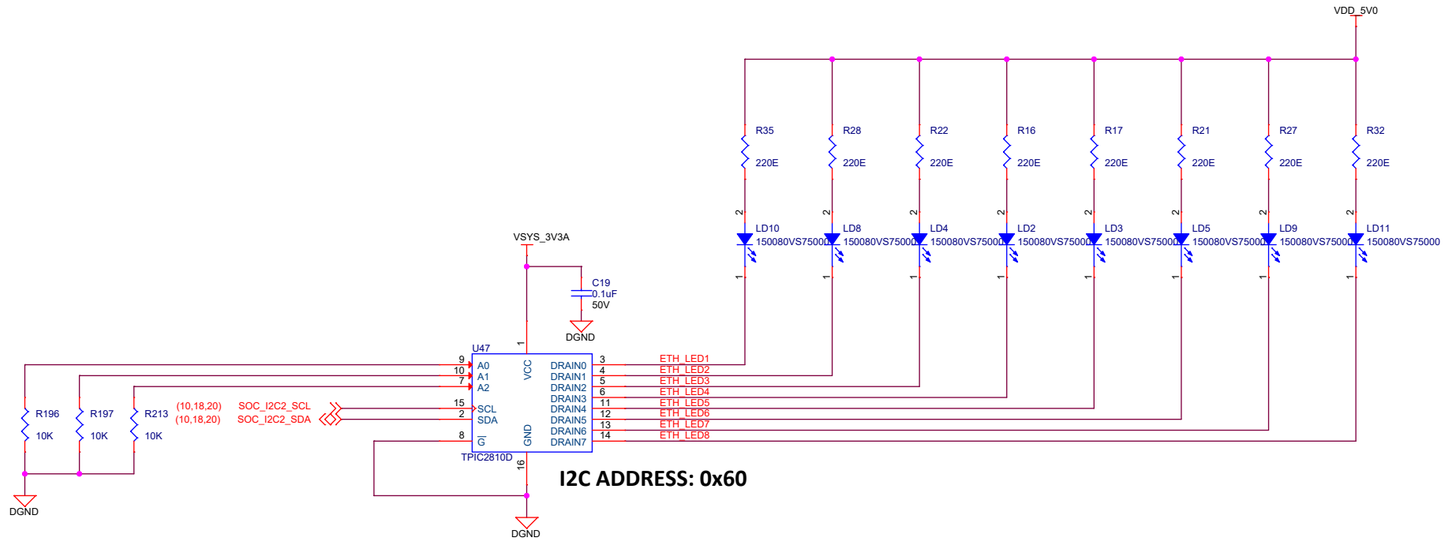
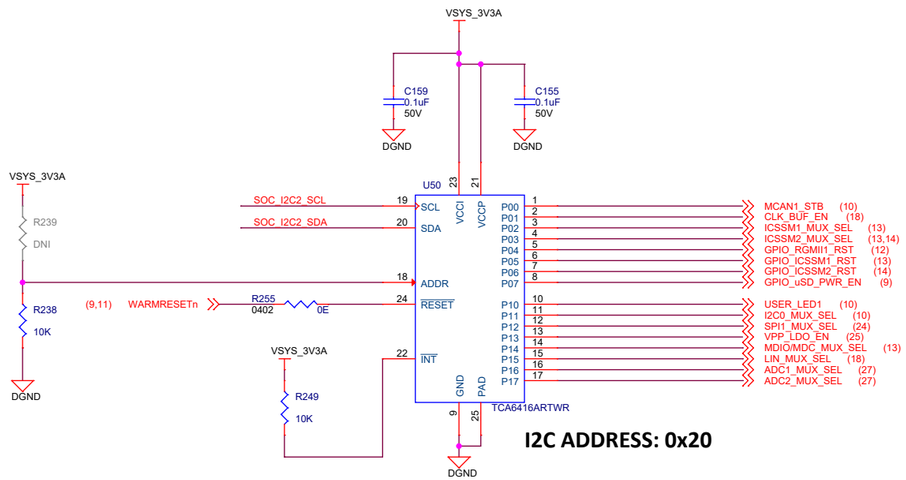
LED Driver



IO Expander



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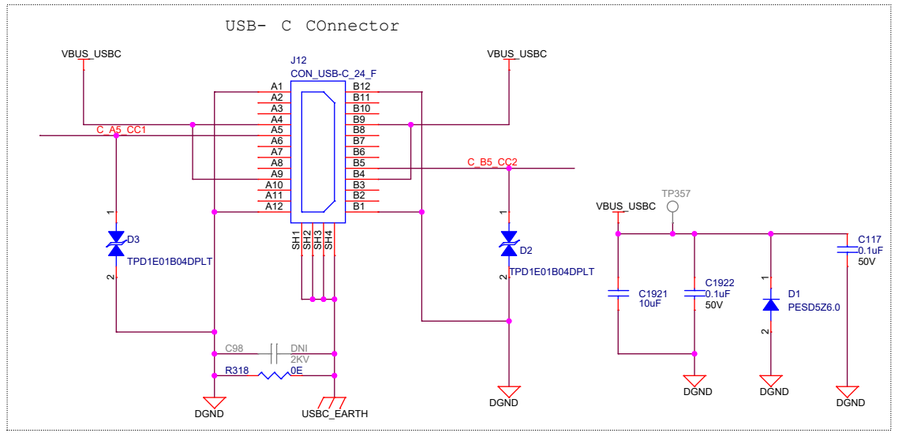
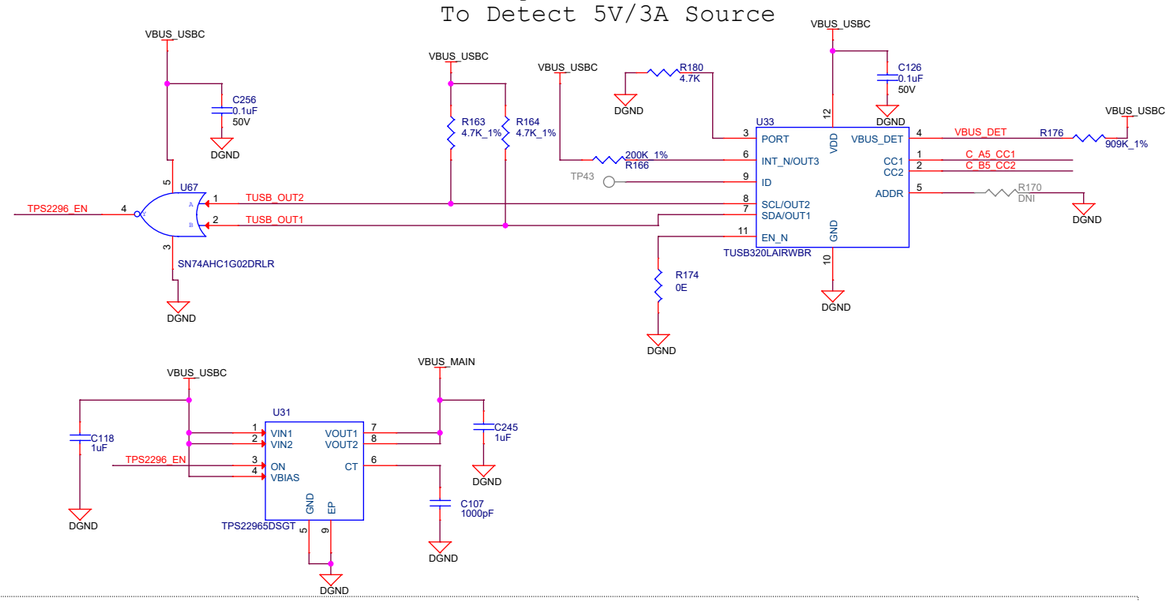
USB-C Power

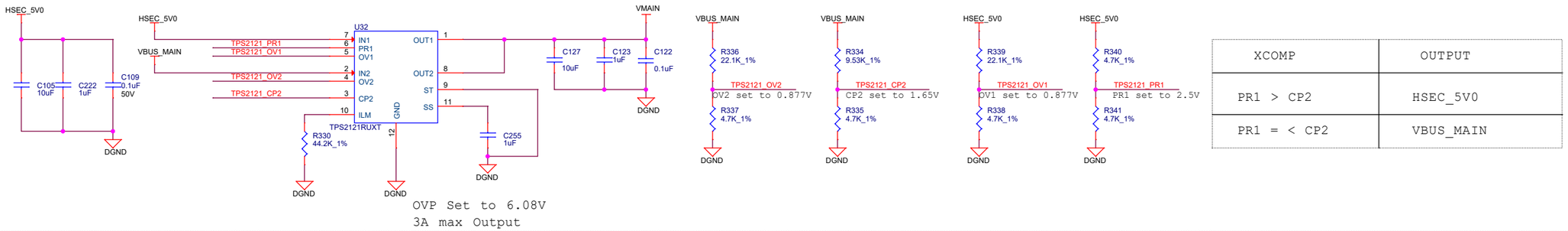
USB- C COnnector



Configured as UFP MODE To Detect 5V/3A Source



Power MUX

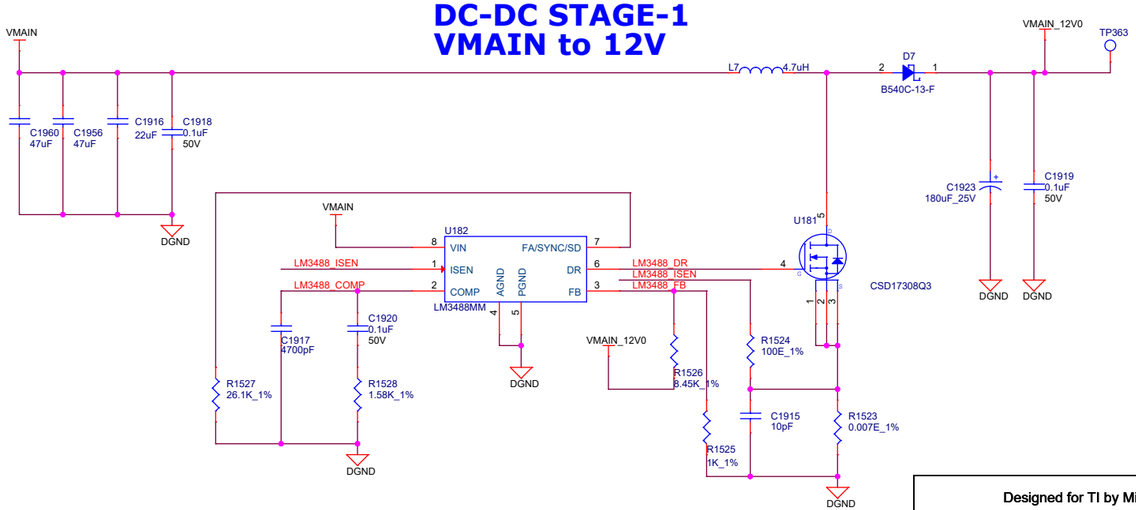


XCOMP	OUTPUT
PR1 > CP2	HSEC_5V0
PR1 = < CP2	VBUS_MAIN

OVP Set to 6.08V
3A max Output

Designed as per reference sch

DC-DC STAGE-1 VMAIN to 12V



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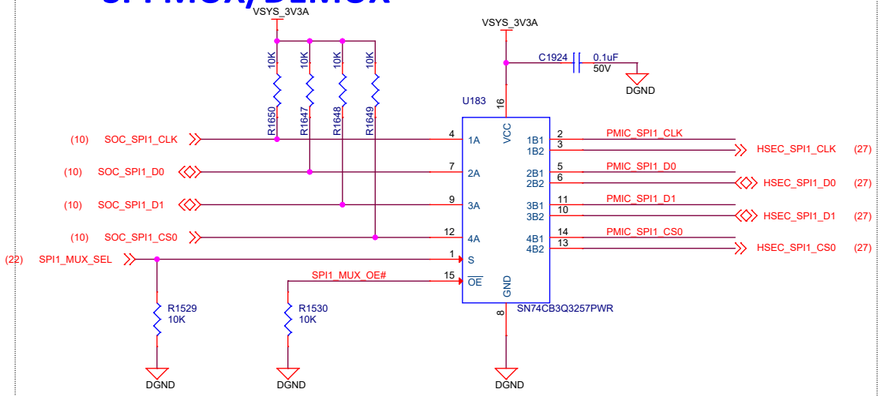
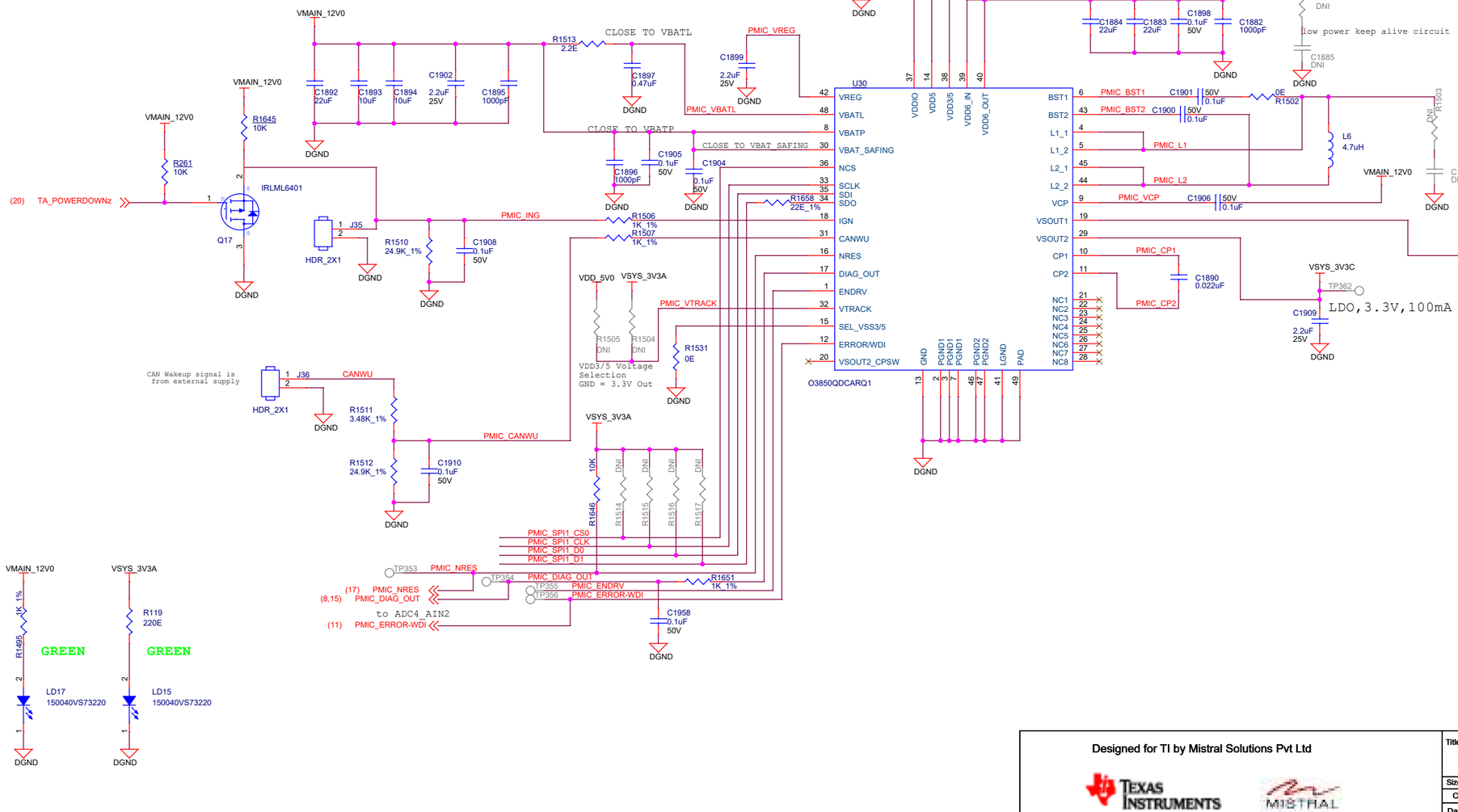
SPI MUX/DEMUX



SPI1 - 1:2 MUX

SEL	CONDITION	FUNCTION
LOW	PMIC SELECTED	A-->B1 port
HIGH	HSEC SPI1 selected	A-->B2 port

MAIN Power and PMIC



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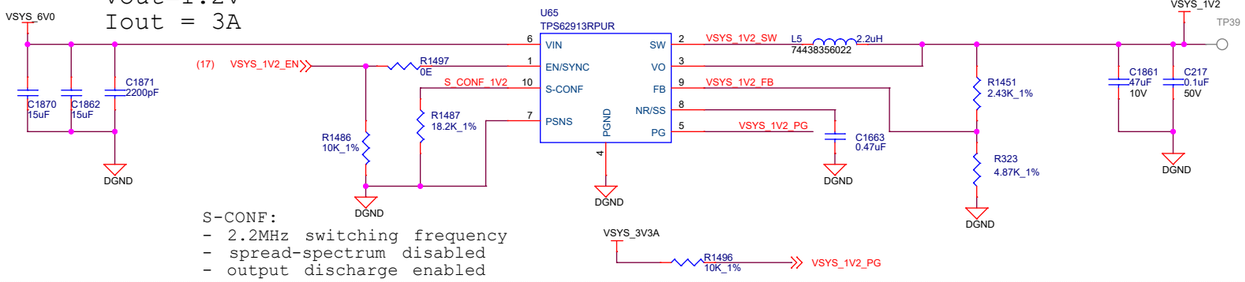
Power Supply #1

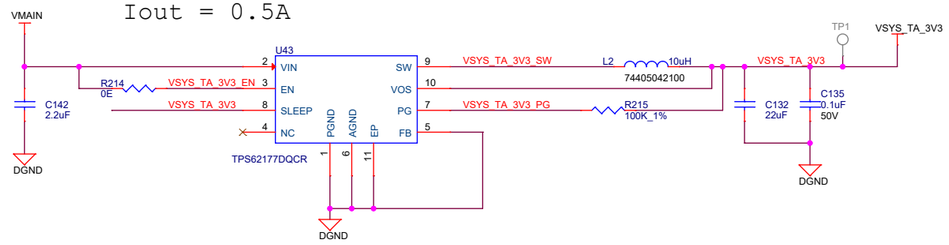
1.2V GENERATION

TPS62913
Vout=1.2V
Iout = 3A



Test Automation Header Supply

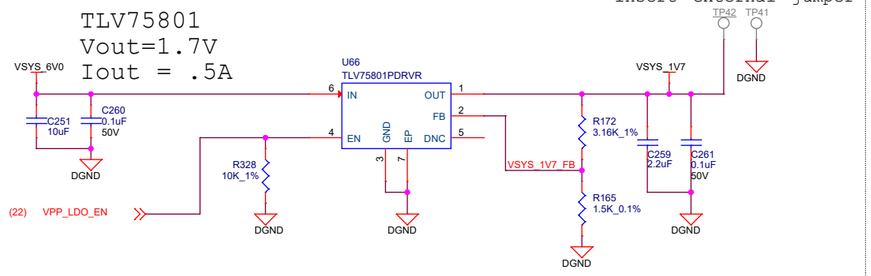
TPS62177 3.3V BUCK REGULATOR
Vout = 3.3V
Iout = 0.5A



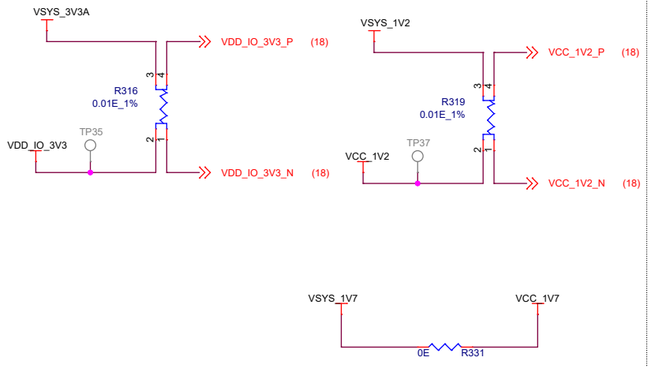
1.7V VPP Generation

Place testpoints with 100mils spacing to insert external jumper

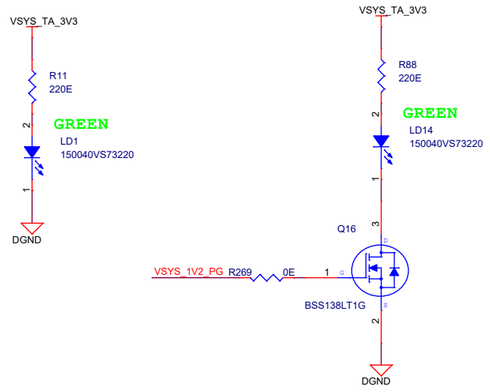
TLV75801
Vout=1.7V
Iout = .5A



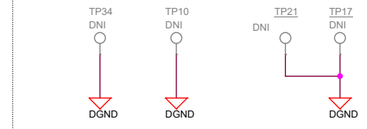
Voltage In-Line Resistors



Power LED



Ground Test Points



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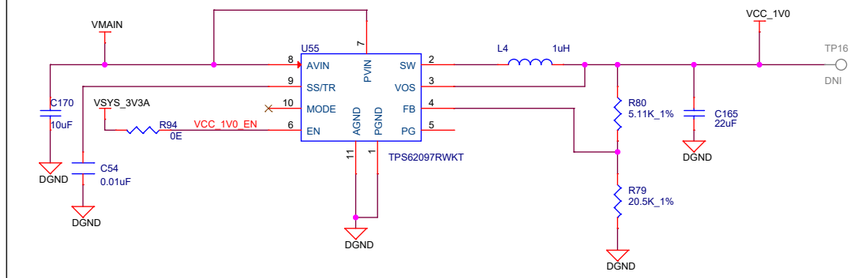
Ethernet Powers

1.0V ETHERNET PHY POWER SUPPLY



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Size: C	Variant Name = PROC153 001	Rev: E2
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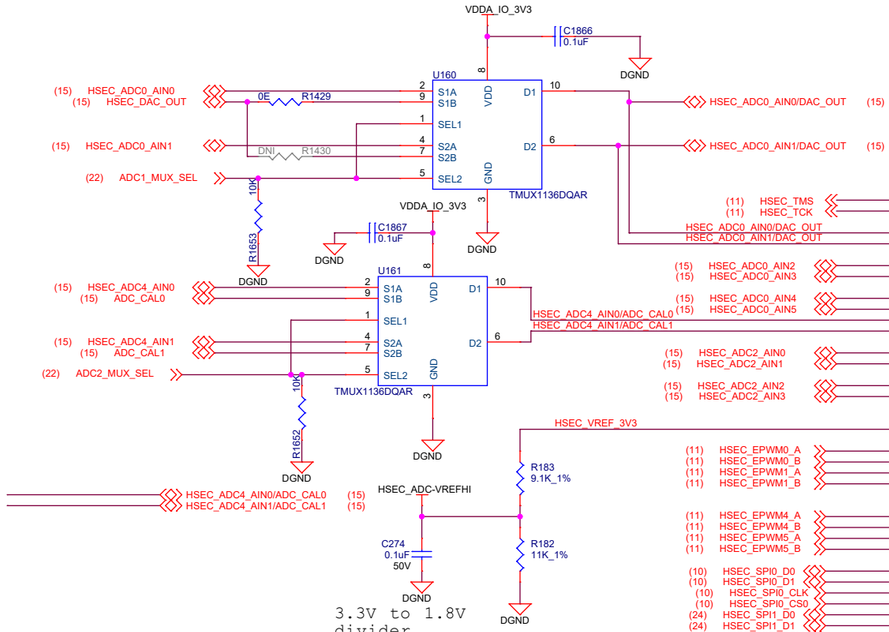
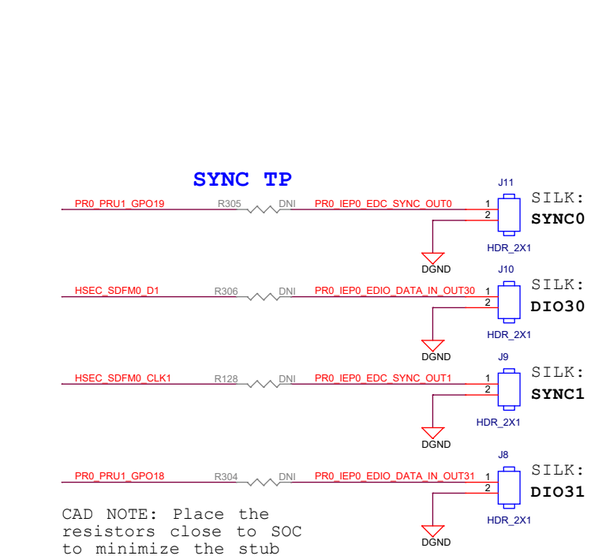
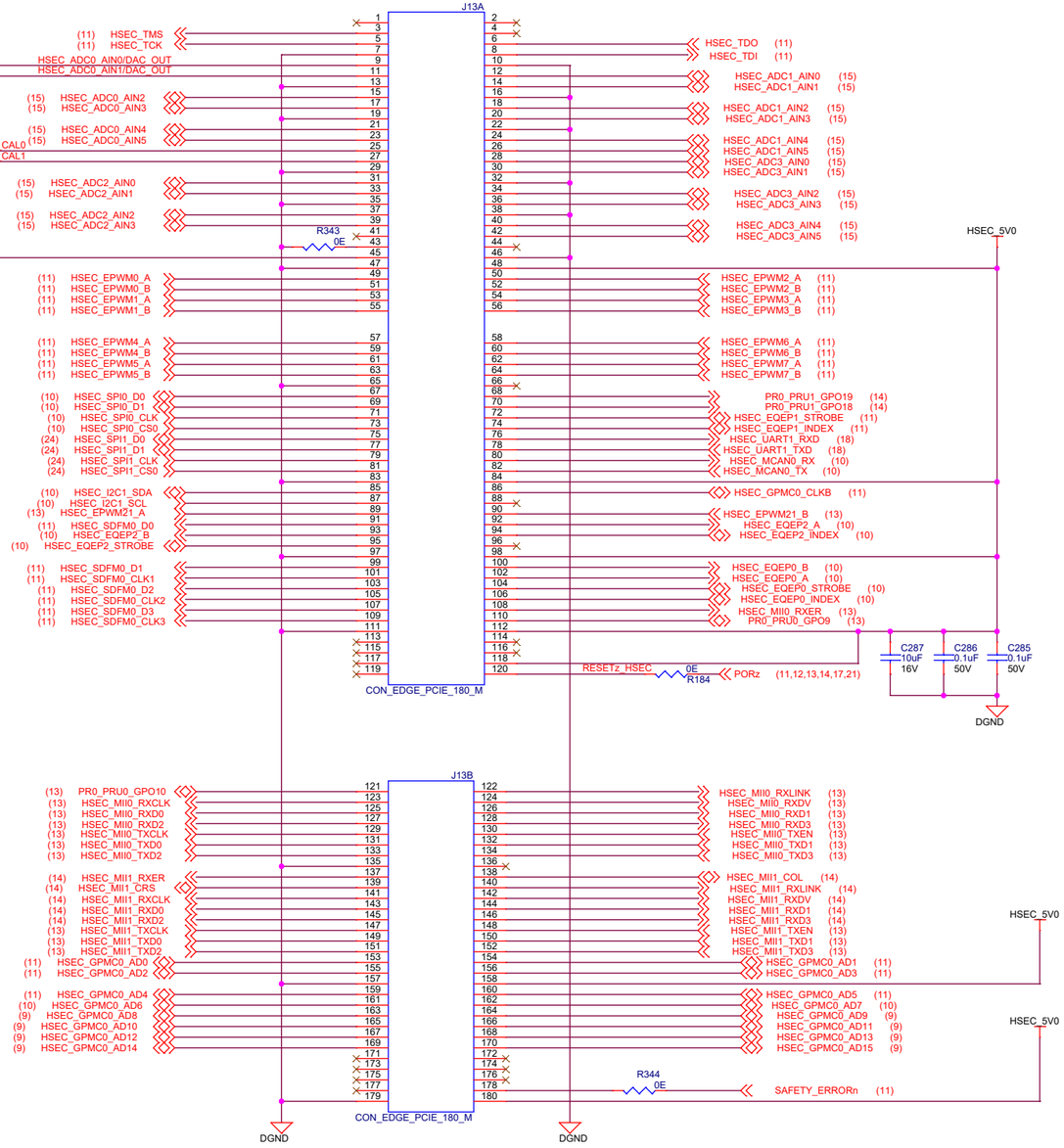
HSEC Connector







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EVM Development & Evaluation test circuitry

(TI EVM Only)

NOTES, HW & LABELS

ASSEMBLY NOTES

1. All MSL components should be baked as per JEDEC standard.

2. PCB should be baked at 120 degree for 8 hours.

3. Board assembly must comply with workmanship standards. IPC-A-610 Class 2, unless otherwise specified.

4. These assemblies are ESD sensitive, ESD precautions shall be observed.

5. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

6. Provide serial numbers to the assembled boards for identification.

7. The assembled board are wrapped in ESD Covers(individual) and
packed securely before shipment.

STANDOFFs

MH5 MH6 MH7 MH8

DNI
DNI

WASHER's

ACC1 ACC2 ACC3 ACC4

DNI
DNI

SCREWS

MH4 MH3 MH2 MH1

MH12 MH11 MH9 MH10

DNI
DNI

RUBBER FEET

ACC5 ACC6 ACC7 ACC8

DNI

FIDUCIALS

FID1 FID2 FID3
FID4 FID5 FID6
DNI

BARE PCB

PCB1

PROC153E2

LABELS

Board Serial No.

LBL1

PCB LABEL

AM6-COMPROCEVM

Assembly Revision.

LBL3

PCB LABEL

AM6-COMPROCEVM

EVM Orderable No.

LBL2

PCB LABEL

AM6-COMPROCEVM

Orderable Part Numbers	
Variant	**Label Text**
001	TMDSCNCD263AUTO

LOGOs

PCB LOGO DNI — Texas Intruments

PCB LOGO DNI — For Evaluation only; not FCC approved for resale

PCB LOGO DNI — WEEE Mark

PCB LOGO DNI — CE Mark

PCB LOGO DNI — High Temperature

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